

To our customers,

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## Old Company Name in Catalogs and Other Documents

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April 1<sup>st</sup>, 2010  
Renesas Electronics Corporation

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# HD74ALVCH16269

## 12-bit to 24-bit Registered Bus Transceivers with 3-state Outputs

REJ03D0046-0200Z  
(Previous ADE-205-136(Z))  
Rev.2.00  
Oct.02.2003

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### Description

The HD74ALVCH16269 is used in applications where two separate ports must be multiplexed onto, or demultiplexed from, a single port. The device is particularly suitable as an interface between synchronous DRAMs and high speed microprocessors. Data is stored in the internal B port registers on the low to high transition of the clock (CLK) input when the appropriate clock enable (CLKENA) inputs are low. Proper control of these inputs allows two sequential 12-bit words to be presented as a 24-bit word on the B port. For data transfer in the B to A direction, a single storage register is provided. The select ( $\overline{SEL}$ ) line selects 1B or 2B data for the A outputs. The register on the A output permits the fastest possible data transfer, thus extending the period that the data is valid on the bus. The control terminals are registered so that all transactions are synchronous with CLK. Data flow is controlled by the active low output enables ( $\overline{OEA}$ ,  $\overline{OEB1}$ ,  $\overline{OEB2}$ ). Active bus hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

### Features

- $V_{CC} = 2.3\text{ V to }3.6\text{ V}$
- Typical  $V_{OL}$  ground bounce  $< 0.8\text{ V}$  ( $@V_{CC} = 3.3\text{ V, }T_a = 25^\circ\text{C}$ )
- Typical  $V_{OH}$  undershoot  $> 2.0\text{ V}$  ( $@V_{CC} = 3.3\text{ V, }T_a = 25^\circ\text{C}$ )
- High output current  $\pm 24\text{ mA}$  ( $@V_{CC} = 3.0\text{ V}$ )
- Bus hold on data inputs eliminates the need for external pullup / pulldown resistors

**Function Table**

Inputs			Outputs	
CLK	$\overline{OEA}$	$\overline{OEB}$	A	1B, 2B
↑	H	H	Z	Z
↑	H	L	Z	Active
↑	L	H	Active	Z
↑	L	L	Active	Active

**Output enable**

Inputs			Outputs		
CLKENA1	$\overline{CLKENA2}$	CLK	A	1B	2B
H	H	X	X	1B <sub>0</sub> <sup>*1</sup>	2B <sub>0</sub> <sup>*1</sup>
L	X	↑	L	L	X
L	X	↑	H	H	X
X	L	↑	L	X	L
X	L	↑	H	X	H

**A-to-B storage ( $\overline{OEB} = L$ )**

Inputs				Output A
CLK	$\overline{SEL}$	1B	2B	
X	H	X	X	A <sub>0</sub> <sup>*1</sup>
X	L	X	X	A <sub>0</sub> <sup>*1</sup>
↑	H	L	X	L
↑	H	H	X	H
↑	L	X	L	L
↑	L	X	H	H

**B-to-A storage ( $\overline{OEA} = L$ )**

H : High level

L : Low level

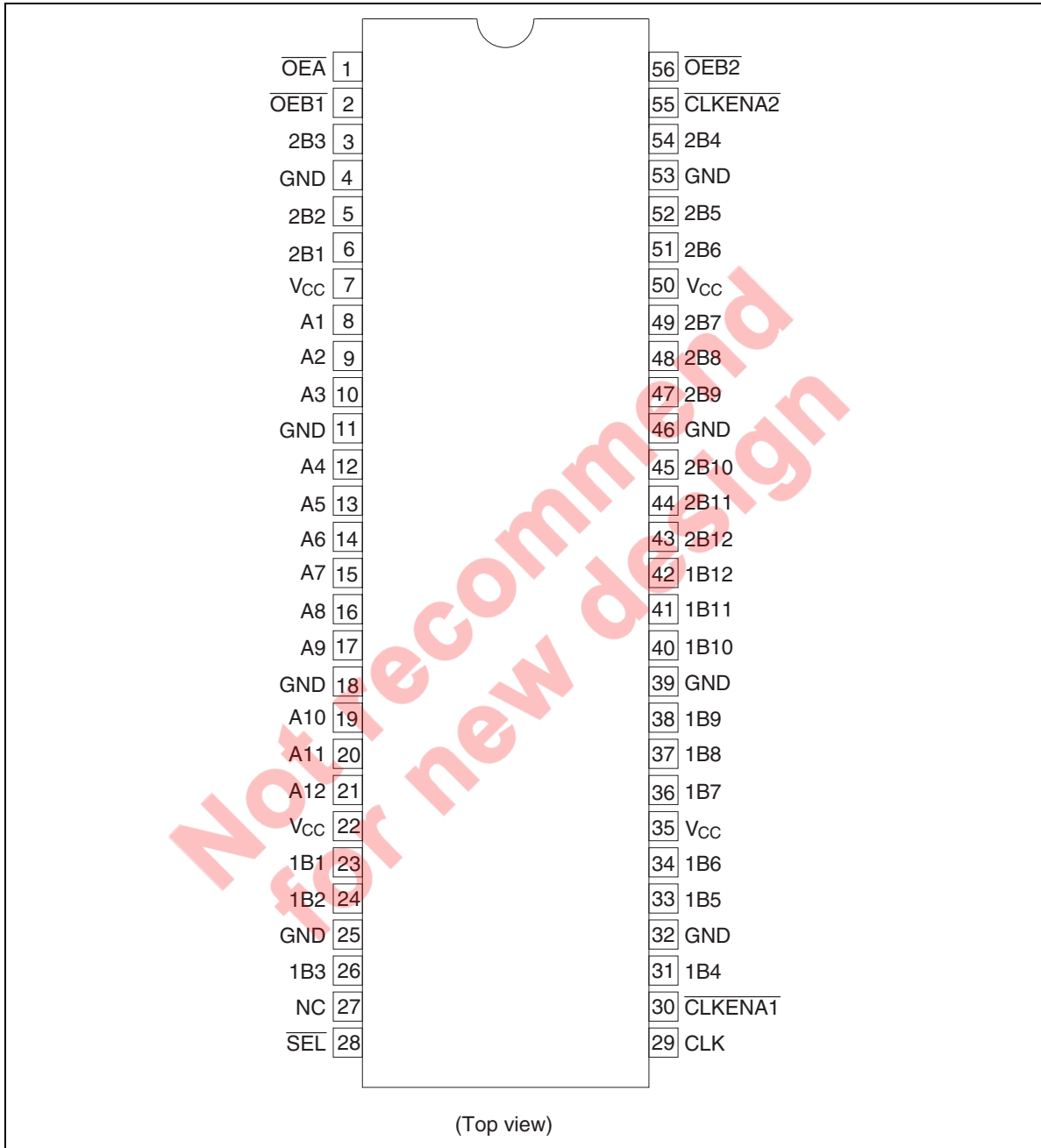
X : Immaterial

Z : High impedance

↑ : Low to high transition

Note: 1. Output level before the indicated steady state input conditions were established.

Pin Arrangement



**Absolute Maximum Ratings**

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	$V_{CC}$	-0.5 to 4.6	V	
Input voltage <sup>*1,2</sup>	$V_I$	-0.5 to 4.6 -0.5 to $V_{CC} + 0.5$	V	Except I/O ports I/O ports
Output voltage <sup>*1,2</sup>	$V_O$	-0.5 to $V_{CC} + 0.5$	V	
Input clamp current	$I_{IK}$	-50	mA	$V_I < 0$
Output clamp current	$I_{OK}$	±50	mA	$V_O < 0$ or $V_O > V_{CC}$
Continuous output current	$I_O$	±50 ±100	mA	$V_O = 0$ to $V_{CC}$
Maximum power dissipation at $T_a = 55^\circ\text{C}$ (in still air) <sup>*3</sup>	$P_T$	1	W	TSSOP
Storage temperature	$T_{stg}$	-65 to 150	°C	

Notes: Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

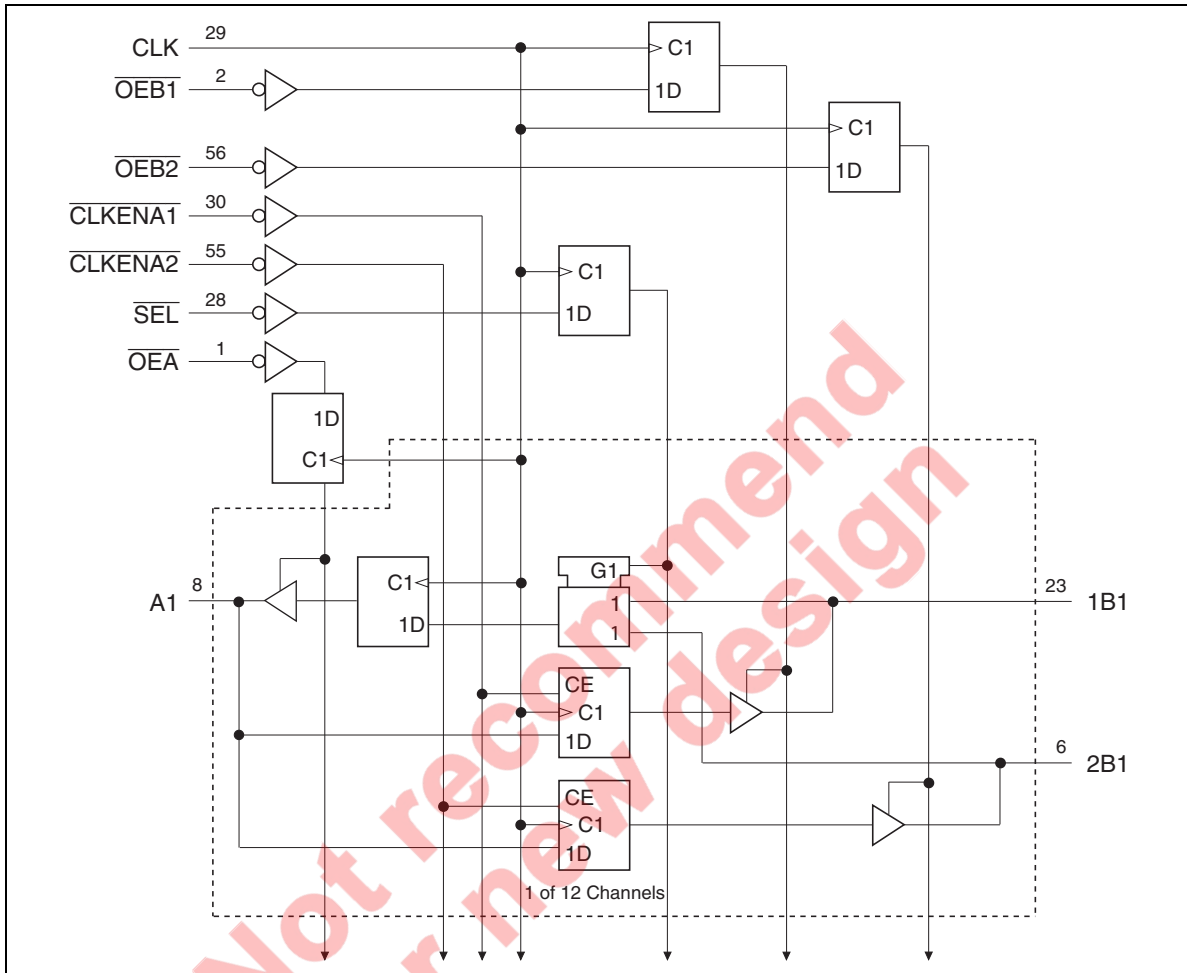
1. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

**Recommended Operating Conditions**

Item	Symbol	Min	Max	Unit	Conditions
Supply voltage	$V_{CC}$	2.3	3.6	V	
Input voltage	$V_I$	0	$V_{CC}$	V	
Output voltage	$V_O$	0	$V_{CC}$	V	
High level output current	$I_{OH}$	—	-12 -12 -24	mA	$V_{CC} = 2.3\text{ V}$ $V_{CC} = 2.7\text{ V}$ $V_{CC} = 3.0\text{ V}$
Low level output current	$I_{OL}$	—	12 12 24	mA	$V_{CC} = 2.3\text{ V}$ $V_{CC} = 2.7\text{ V}$ $V_{CC} = 3.0\text{ V}$
Input transition rise or fall rate	$\Delta t / \Delta v$	0	10	ns / V	
Operating temperature	$T_a$	-40	85	°C	

Note: Unused control inputs must be held high or low to prevent them from floating.

Logic Diagram



**Electrical Characteristics**

(Ta = -40 to 85°C)

Item	Symbol	V <sub>CC</sub> (V) <sup>*1</sup>	Min	Max	Unit	Test Conditions
Input voltage	V <sub>IH</sub>	2.3 to 2.7	1.7	—	V	
		2.7 to 3.6	2.0	—		
	V <sub>IL</sub>	2.3 to 2.7	—	0.7		
		2.7 to 3.6	—	0.8		
Output voltage	V <sub>OH</sub>	Min to Max	V <sub>CC</sub> -0.2	—	V	I <sub>OH</sub> = -100 μA
		2.3	2.0	—		I <sub>OH</sub> = -6 mA, V <sub>IH</sub> = 1.7 V
		2.3	1.7	—		I <sub>OH</sub> = -12 mA, V <sub>IH</sub> = 1.7 V
		2.7	2.2	—		I <sub>OH</sub> = -12 mA, V <sub>IH</sub> = 2.0 V
		3.0	2.4	—		I <sub>OH</sub> = -12 mA, V <sub>IH</sub> = 2.0 V
		3.0	2.0	—		I <sub>OH</sub> = -24 mA, V <sub>IH</sub> = 2.0 V
	V <sub>OL</sub>	Min to Max	—	0.2		I <sub>OL</sub> = 100 μA
		2.3	—	0.4		I <sub>OL</sub> = 6 mA, V <sub>IL</sub> = 0.7 V
		2.3	—	0.7		I <sub>OL</sub> = 12 mA, V <sub>IL</sub> = 0.7 V
		2.7	—	0.4		I <sub>OL</sub> = 12 mA, V <sub>IL</sub> = 0.8 V
		3.0	—	0.55		I <sub>OL</sub> = 24 mA, V <sub>IL</sub> = 0.8 V
		3.0	—	0.55		I <sub>OL</sub> = 24 mA, V <sub>IL</sub> = 0.8 V
Input current	I <sub>IN</sub>	3.6	—	±5	μA	V <sub>IN</sub> = V <sub>CC</sub> or GND
	I <sub>IN (hold)</sub>	2.3	45	—		V <sub>IN</sub> = 0.7 V
		2.3	-45	—		V <sub>IN</sub> = 1.7 V
		3.0	75	—		V <sub>IN</sub> = 0.8 V
		3.0	-75	—		V <sub>IN</sub> = 2.0 V
		3.6	—	±500		V <sub>IN</sub> = 0 to 3.6 V
		3.6	—	±500		V <sub>IN</sub> = 0 to 3.6 V
3.6	—	±500	V <sub>IN</sub> = 0 to 3.6 V			
Off state output current <sup>*2</sup>	I <sub>OZ</sub>	3.6	—	±10	μA	V <sub>OUT</sub> = V <sub>CC</sub> or GND
Quiescent supply current	I <sub>CC</sub>	3.6	—	40	μA	V <sub>IN</sub> = V <sub>CC</sub> or GND
	ΔI <sub>CC</sub>	3.0 to 3.6	—	750	μA	V <sub>IN</sub> = one input at (V <sub>CC</sub> -0.6) , other inputs at V <sub>CC</sub> or GND

- Notes: 1. For conditions shown as Min or Max, use the appropriate values under recommended operating conditions.  
 2. For I/O ports, the parameter I<sub>OZ</sub> includes the input leakage current.



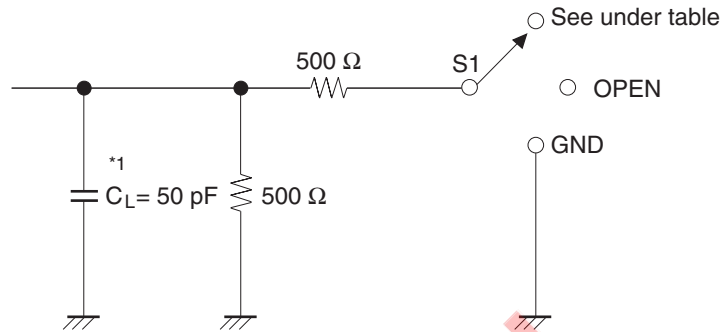
Switching Characteristics

Item	Symbol	V <sub>CC</sub> (V)	Min	Typ	Max	Unit	FROM (Input)	TO (Output)
Maximum clock frequency	f <sub>max</sub>	2.5±0.2	135	—	—	MHz		
		2.7	135	—	—			
		3.3±0.3	135	—	—			
Propagation delay time	t <sub>PLH</sub>	2.5±0.2	1.0	—	8.8	ns	CLK	B
		2.7	—	—	7.3			
	3.3±0.3	1.0	—	6.2				
	2.5±0.2	1.0	—	7.0	A			
	2.7	—	—	5.8				
	3.3±0.3	1.0	—	5.0				
Output enable time	t <sub>ZH</sub>	2.5±0.2	1.0	—	8.4	ns	CLK	B
		2.7	—	—	6.7			
	3.3±0.3	1.0	—	6.1				
	2.5±0.2	1.0	—	8.1	A			
	2.7	—	—	6.2				
	3.3±0.3	1.0	—	5.9				
Output disable time	t <sub>HZ</sub>	2.5±0.2	1.4	—	8.3	ns	CLK	B
		2.7	—	—	6.9			
	3.3±0.3	1.0	—	6.1				
	2.5±0.2	1.5	—	7.7	A			
	2.7	—	—	6.8				
	3.3±0.3	1.0	—	5.6				
Input capacitance	C <sub>IN</sub>	3.3	—	3.5	—	pF	Control inputs	
Output capacitance	C <sub>IN/O</sub>	3.3	—	9.0	—	pF	A or B ports	

Switching Characteristics (cont.)

Item	Symbol	V <sub>CC</sub> (V)	Min	Typ	Max	Unit	FROM (Input)
Setup time	t <sub>su</sub>	2.5±0.2	2.0	—	—	ns	A data before CLK↑
		2.7	2.0	—	—		
		3.3±0.3	1.7	—	—		
		2.5±0.2	2.2	—	—		B data before CLK↑
		2.7	2.1	—	—		
		3.3±0.3	1.8	—	—		
		2.5±0.2	1.6	—	—		SEL before CLK↑
		2.7	1.6	—	—		
		3.3±0.3	1.3	—	—		
		2.5±0.2	1.0	—	—		CLKENA1 or
		2.7	1.2	—	—		CLKENA2 before LK↑
		3.3±0.3	0.9	—	—		
		2.5±0.2	1.5	—	—		OE before CLK↑
		2.7	1.6	—	—		
		3.3±0.3	1.3	—	—		
Hold time	t <sub>h</sub>	2.5±0.2	0.7	—	—	ns	A data after CLK↑
		2.7	0.6	—	—		
		3.3±0.3	0.6	—	—		
		2.5±0.2	0.7	—	—		B data after CLK↑
		2.7	0.6	—	—		
		3.3±0.3	0.6	—	—		
		2.5±0.2	1.1	—	—		SEL after CLK↑
		2.7	0.7	—	—		
		3.3±0.3	0.7	—	—		
		2.5±0.2	1.0	—	—		CLKENA1 or
		2.7	0.8	—	—		CLKENA2 after CLK↑
		3.3±0.3	1.1	—	—		
		2.5±0.2	0.8	—	—		OE after CLK↑
		2.7	0.8	—	—		
		3.3±0.3	0.8	—	—		
Pulse width	t <sub>w</sub>	2.5±0.2	3.3	—	—	ns	CLK "H" or "L"
		2.7	3.3	—	—		
		3.3±0.3	3.3	—	—		

• Test Circuit

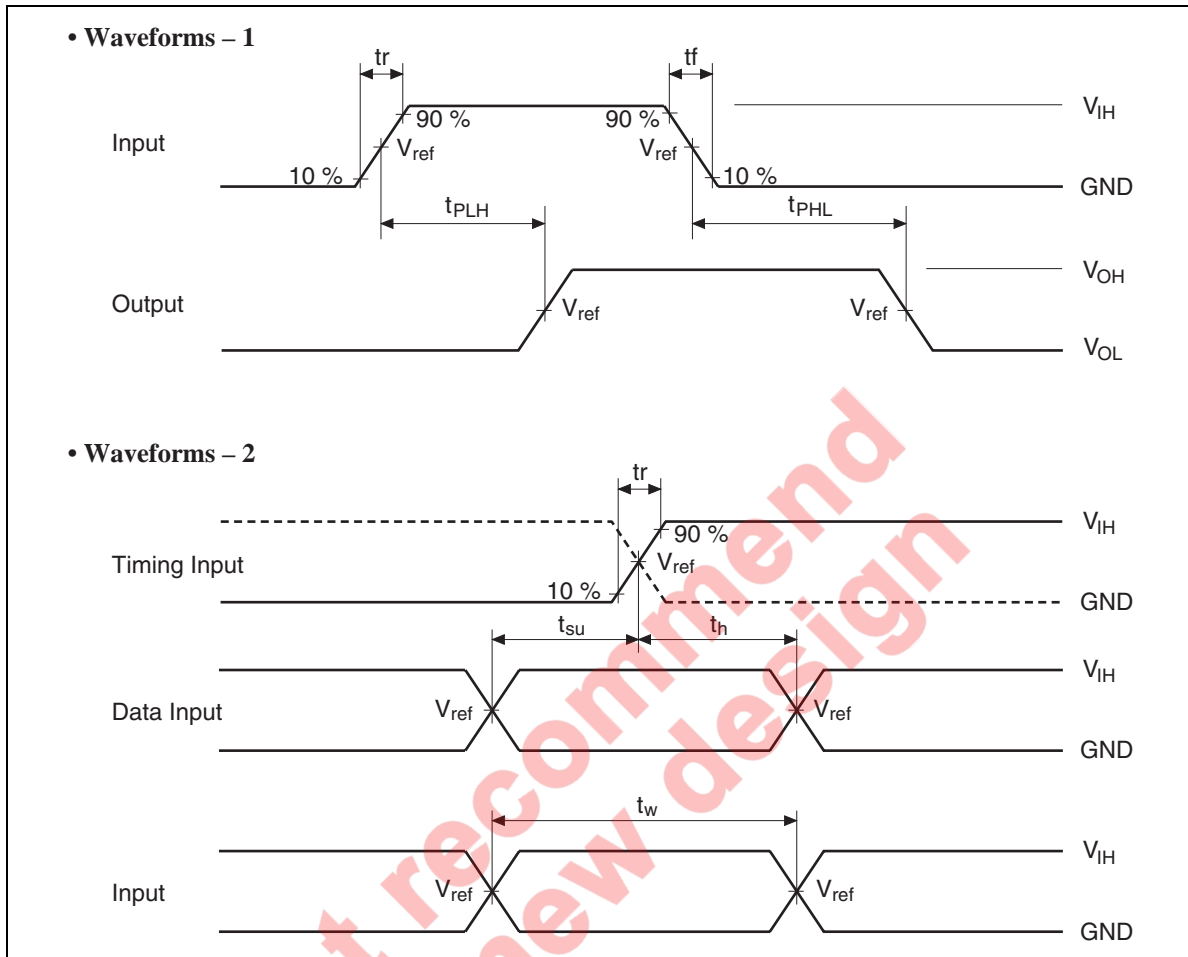


Load Circuit for Outputs

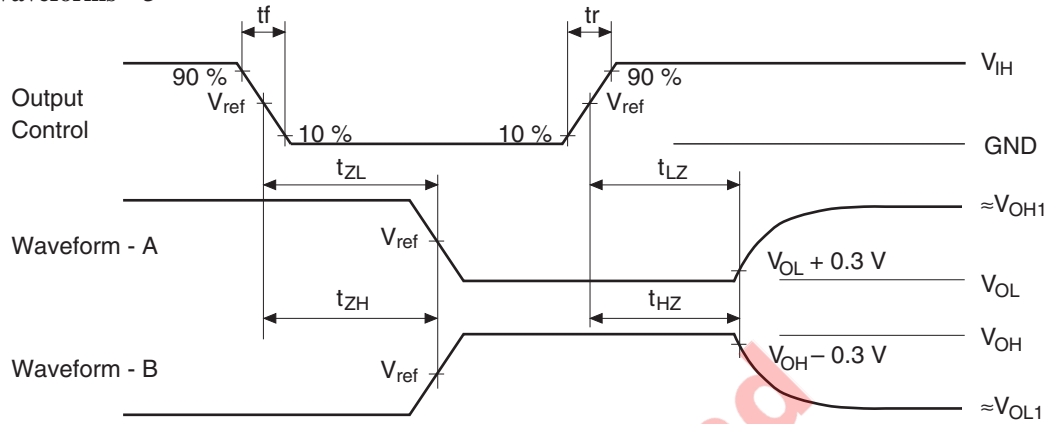
Symbol	V <sub>CC</sub> =2.5±0.2V	V <sub>CC</sub> =2.7V, 3.3±0.3V
t <sub>PLH</sub> /t <sub>PHL</sub>	OPEN	OPEN
t <sub>su</sub> /t <sub>h</sub> /t <sub>w</sub>	OPEN	OPEN
t <sub>ZH</sub> /t <sub>HZ</sub>	GND	GND
t <sub>ZL</sub> /t <sub>LZ</sub>	4.6 V	6.0 V

Note: 1. C<sub>L</sub> includes probe and jig capacitance.

Not recommended for new design



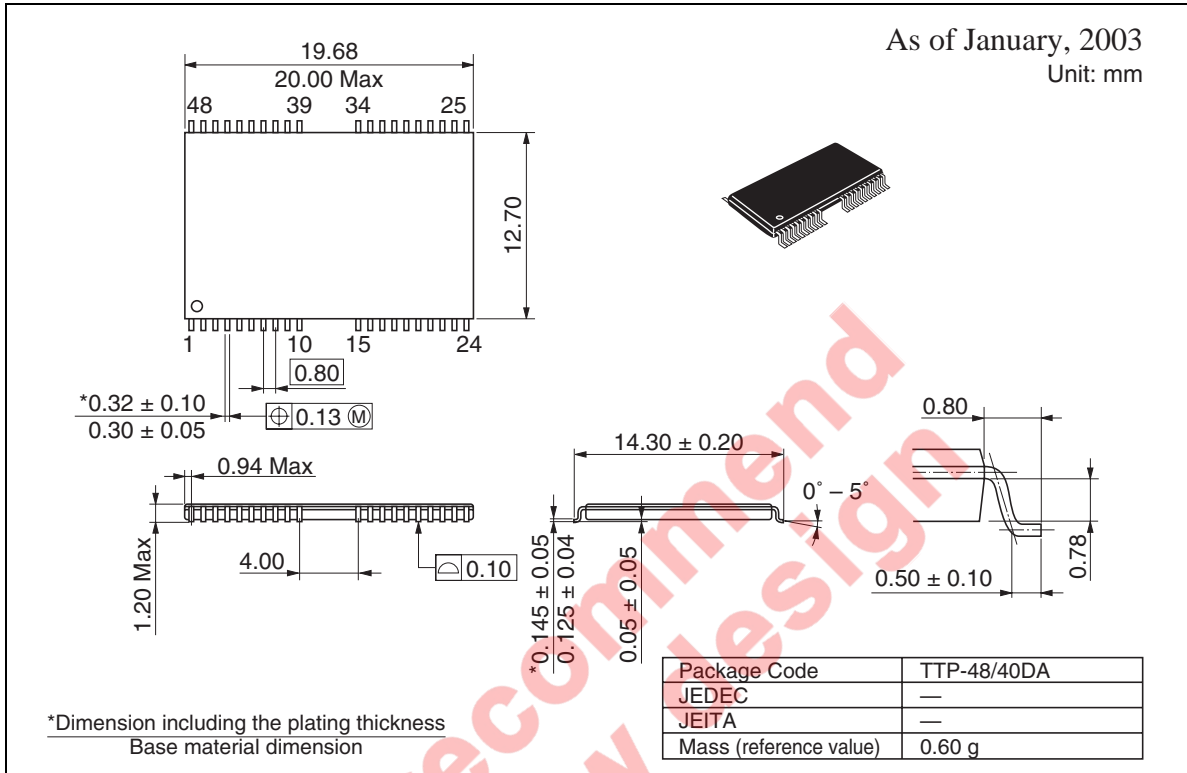
• Waveforms – 3



TEST	$V_{CC}=2.5\pm 0.2V$	$V_{CC}=2.7V, 3.3\pm 0.3V$
$V_{IH}$	2.3 V	2.7 V
$V_{ref}$	1.2 V	1.5 V
$V_{OH1}$	2.3 V	3.0 V
$V_{OL1}$	GND	GND

- Notes:
1. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_o = 50 \Omega$ ,  $t_r \leq 2.5$  ns,  $t_f \leq 2.5$  ns.
  2. Waveform – A is for an output with internal conditions such that the output is low except when disabled by the output control.
  3. Waveform – B is for an output with internal conditions such that the output is high except when disabled by the output control.
  4. The output are measured one at a time with one transition per measurement.

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