SN74ALVCH162373 16-BIT TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS

SCES583A-JULY 2004-REVISED OCTOBER 2004

FEATURES

- Member of the Texas Instruments Widebus™
 Family
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Output Ports Have Equivalent 26-Ω Series Resistors, So No External Resistors Are Required
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)

DESCRIPTION/ORDERING INFORMATION

This 16-bit transparent D-type latch is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74ALVCH162373 is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers. This device can be used as two 8-bit latches or one 16-bit latch. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the levels set up at the D inputs.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components. \overline{OE} does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

1 <u>0E</u> [₁ ∪	48	l 1 1LE
1Q1 [2	47	1 1D1
1Q2 [3	46	1D2
GND [4	45	GND
1Q3 [1	44	1 1D3
1Q3 [1Q4 [6	43	1 1D3
	o	-	E
V _{CC} [7	42	V_{CC}
1Q5 [8	41] 1D5
1Q6 [9	40] 1D6
GND [10	39	GND
1Q7 [11	38	1D7
1Q8 [12	37	1D8
2Q1 [13	36	2D1
2Q2 [14	35	2D2
GND [15	34	GND
2Q3 [16	33] 2D3
2Q4 [17	32] 2D4
v _{cc} [18	31] v _{cc}
2Q5 [19	30] 2D5
2Q6 [20	29] 2D6
GND [21	28	GND

27 2D7

26 T 2D8

25 **∏** 2LE

2Q7 **1**22

2Q8 **∏**23

20E **1**24

DGG OR DL PACKAGE

(TOP VIEW)

The outputs, which are designed to sink up to 12 mA, include equivalent 26- Ω resistors to reduce overshoot and undershoot.

ORDERING INFORMATION

T _A	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING	
	SSOP - DL	Tube	SN74ALVCH162373DL	ALVCH162373	
4000 +- 0500	330P - DL	Tape and reel	SN74ALVCH162373LR		
-40°C to 85°C	TSSOP - DGG	Tape and reel	SN74ALVCH162373GR	ALVCH162373	
	VFBGA - GQL	Tape and reel	SN74ALVCH162373KR	VH2373	

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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DESCRIPTION/ORDERING INFORMATION (CONTINUED)

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry holds unused or undriven data inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

(TOP VIEW) 2 3 4 5 6 000000 Α В 000000 000000 С 000000 D Ε \bigcirc \bigcirc F \circ \circ 000000 G 000000 Н 000000 J 000000 Κ

GQL PACKAGE

TERMINAL ASSIGNMENTS(1)

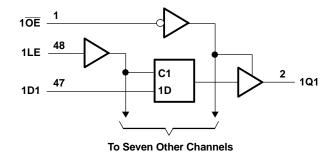
	1	2	3	4	5	6
Α	1 OE	NC	NC	NC	NC	1LE
В	1Q2	1Q1	GND	GND	1D1	1D2
С	1Q4	1Q3	V _{CC}	V _{CC}	1D3	1D4
D	1Q6	1Q5	GND	GND	1D5	1D6
Е	1Q8	1Q7			1D7	1D8
F	2Q1	2Q2			2D2	2D1
G	2Q3	2Q4	GND	GND	2D4	2D3
Н	2Q5	2Q6	V _{CC}	V _{CC}	2D6	2D5
J	2Q7	2Q8	GND GND		2D8	2D7
K	2 OE	NC	NC	NC	NC	2LE

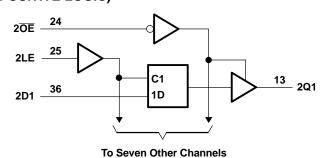
(1) NC - No internal connection

FUNCTION TABLE (each 8-bit section)

	INPUTS	OUTPUT	
ŌĒ	LE	D	Q
L	Н	Н	Н
L	Н	L	L
L	L	X	Q_0
Н	X	Χ	Z

LOGIC DIAGRAM (POSITIVE LOGIC)





Pin numbers shown are for the DGG and DL packages.



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ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		-0.5	4.6	V
V_{I}	Input voltage range ⁽²⁾		-0.5	4.6	V
Vo	Output voltage range (2)(3)		-0.5	$V_{CC} + 0.5$	V
I _{IK}	Input clamp current	V _I < 0		-50	mA
I _{OK}	Output clamp current	V _O < 0		-50	mA
Io	Continuous output current			±50	mA
	Continuous current through each V _{CC} or GN	ID		±100	mA
		DGG package		70	
θ_{JA}	Package thermal impedance (4)	DL package		63	°C/W
		GQL package		42	
T _{stg}	Storage temperature range		-65	150	°C

⁽¹⁾ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS(1)

			MIN	MAX	UNIT
V _{CC}	Supply voltage		1.65	3.6	V
		V _{CC} = 1.65 V to 1.95 V	$0.65 \times V_{CC}$	V _{CC}	
V_{IH}	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7	V _{CC}	V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2	V_{CC}	
		V _{CC} = 1.65 V to 1.95 V	0	$0.35 \times V_{CC}$	
V_{IL}	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	0	0.7	V
		V _{CC} = 2.7 V to 3.6 V	0	0.8	
Vo	Output voltage		0	V_{CC}	V
		V _{CC} = 1.65 V		-2	
	High lovel output ourrant	V _{CC} = 2.3 V			mA
I _{OH}	High-level output current	V _{CC} = 2.7 V		-8	IIIA
		V _{CC} = 3 V		-12	
		V _{CC} = 1.65 V		2	
	Low lovel output ourrent	V _{CC} = 2.3 V		6	mA
l _{OL}	Low-level output current	V _{CC} = 2.7 V		8	
		V _{CC} = 3 V		12	
Δt/Δν	Input transition rise or fall rate			10	ns/V
T _A	Operating free-air temperature		-40	85	°C

⁽¹⁾ All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

⁽²⁾ The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

³⁾ This value is limited to 4.6 V maximum.

⁽⁴⁾ The package thermal impedance is calculated in accordance with JESD 51-7.

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ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

F	PARAMETER	TEST CONDITIONS	V _{cc}	MIN	TYP ⁽¹⁾ MAX	UNIT		
		$I_{OH} = -100 \mu\text{A}$	1.65 V to 3.6 V	V _{CC} - 0.2				
		$I_{OH} = -2 \text{ mA}$	1.65 V	1.2				
		$I_{OH} = -4 \text{ mA}$	2.3 V	1.9				
V _{OH}			2.3 V	1.7		V		
		I _{OH} = -6 mA	3 V	2.4				
		$I_{OH} = -8 \text{ mA}$	2.7 V	2				
		I _{OH} = -12 mA	3 V	2				
		$I_{OL} = 100 \mu A$	1.65 V to 3.6 V		0.2			
		I _{OL} = 2 mA	1.65 V		0.45			
		I _{OL} = 4 mA	2.3 V		0.4			
V _{OL}		L C A	2.3 V		0.55	V		
		I _{OL} = 6 mA	3 V		0.55			
		I _{OL} = 8 mA	2.7 V		0.6			
		I _{OL} = 12 mA	3 V		0.8			
I _I		$V_I = V_{CC}$ or GND	3.6 V		±5	μΑ		
		V _I = 0.58 V	1.65 V	25				
		V _I = 1.07 V	1.65 V	-25				
		V _I = 0.7 V	2.3 V	45				
I _{I(hold)}		V _I = 1.7 V	2.3 V	-45		μΑ		
, ,		V _I = 0.8 V	3 V	75				
		V _I = 2 V	3 V	-75				
		$V_1 = 0$ to 3.6 $V^{(2)}$	3.6 V		±500			
l _{OZ}		$V_O = V_{CC}$ or GND	3.6 V		±10	μΑ		
I _{CC}		$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		40	μΑ		
ΔI_{CC}		One input at V_{CC} - 0.6 V, Other inputs at V_{CC} or GND	3 V to 3.6 V		750	μΑ		
0	Control inputs	V V or CND	221/		3	~ F		
C _i	Data inputs	$V_{I} = V_{CC}$ or GND	3.3 V		6	pF		
Co	Outputs	$V_O = V_{CC}$ or GND	3.3 V		7	pF		

TIMING REQUIREMENTS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		$V_{CC} = 1.8 \text{ V} $ $V_{CC} = 2.5 \text{ V} $ $\pm 0.15 \text{ V} $ $0.2 \text{ V} $		V _{CC} = 2.7 V	V_{CC} = 3.3 V \pm 0.3 V	UNIT
		MIN MAX	MIN MAX	MIN MAX	MIN MAX	
t _w	Pulse duration, LE high or low	3.3	3.3	3.3	3.3	ns
t _{su}	Setup time, data before LE↓	1.1	1.1	1.1	1.1	ns
t _h	Hold time, data after LE↓	1.1	1.1	1.1	1.1	ns

⁽¹⁾ All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$. (2) This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.







SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTBUT)	V _{CC} = ± 0.1	1.8 V I5 V	V _{CC} = 1 ± 0.2	2.5 V 2 V	V _{CC} =	2.7 V	V _{CC} = ± 0.	3.3 V 3 V	UNIT
	(INFOT)) (OUTPUT)		MAX	MIN	MAX	MIN	MAX	MIN	MAX	
	D	0	1	6.3	1	5.3	1	4.5	1.1	4	20
ι _{pd}	LE	Q	1	6.6	1	5.6	1	5	1	4.2	ns
t _{en}	ŌĒ	Q	1	7.2	1	6.5	1.5	6	1	5	ns
t _{dis}	ŌĒ	Q	1	6.5	1	5.6	1.5	5.5	1.4	4.5	ns
t _{sk(o)}				1		0.5		0.5		0.5	ns

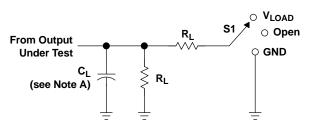
OPERATING CHARACTERISTICS

 $T_A = 25^{\circ}C$

	PARAMETER		TEST CONDITIONS	V _{CC} = 1.8 V TYP	V _{CC} = 2.5 V TYP	V _{CC} = 3.3 V TYP	UNIT
_	Dower dissipation conscitance	Outputs enabled	C ₁ = 50 pF. f = 10 MHz	20	22	26	pF
Cp	Power dissipation capacitance	Outputs disabled	$C_L = 50 \text{ pF}, f = 10 \text{ MHz}$	6	6.5	8	рг



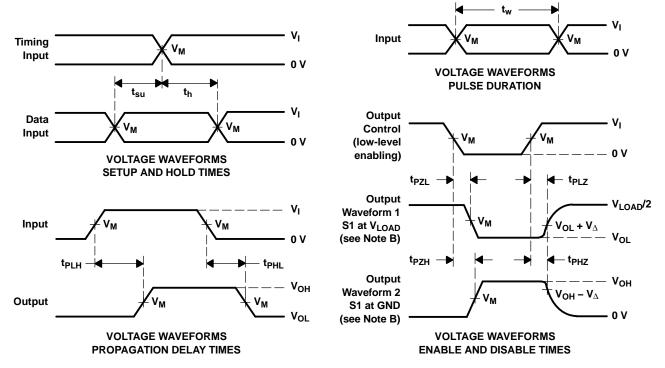
PARAMETER MEASUREMENT INFORMATION



TEST	S 1
t _{pd}	Open
t _{PLZ} /t _{PZL}	V _{LOAD}
t _{PHZ} /t _{PZH}	GND

LOAD CIRCUIT

V	INPUT			ь	V		
V _{CC}	VI	t _r /t _f	V _M	V _{LOAD}	CL	R _L	$V_{\!\scriptscriptstyle \Delta}$
1.8 V	V _{CC}	≤ 2 ns	V _{CC} /2	2×V _{CC}	30 pF	1 k Ω	0.15 V
2.5 V \pm 0.2 V	V _{CC}	≤2 ns	V _{CC} /2	2×V _{CC}	30 pF	500 Ω	0.15 V
2.7 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
3.3 V \pm 0.3 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_{O} = 50 \Omega$.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .
- H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms





11-Apr-2013

PACKAGING INFORMATION

Orderable Device	Status	Package Type	Package Drawing	Pins	Package Qty	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Top-Side Markings	Samples
74ALVCH162373DLG4	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVCH162373	Samples
74ALVCH162373GRE4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVCH162373	Samples
74ALVCH162373GRG4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVCH162373	Samples
74ALVCH162373LRG4	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVCH162373	Samples
74ALVCH162373ZQLR	ACTIVE	BGA MICROSTAR JUNIOR	ZQL	56	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	VH2373	Samples
SN74ALVCH162373DL	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVCH162373	Samples
SN74ALVCH162373GR	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVCH162373	Samples
SN74ALVCH162373KR	OBSOLETE	BGA MICROSTAR JUNIOR	GQL	56		TBD	Call TI	Call TI	-40 to 85	VH2373	
SN74ALVCH162373LR	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVCH162373	Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.



PACKAGE OPTION ADDENDUM

11-Apr-2013

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Dackage	Package	Dine	SPQ	Reel	Reel	Α0	В0	K0	P1	W	Pin1
Device	Туре	Drawing		5	Diameter	Width W1 (mm)	(mm)	(mm)	(mm)	(mm)		Quadrant
74ALVCH162373ZQLR	BGA MI CROSTA R JUNI OR	ZQL	56	1000	330.0	16.4	4.8	7.3	1.5	8.0	16.0	Q1
SN74ALVCH162373GR	TSSOP	DGG	48	2000	330.0	24.4	8.6	15.8	1.8	12.0	24.0	Q1
SN74ALVCH162373LR	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1

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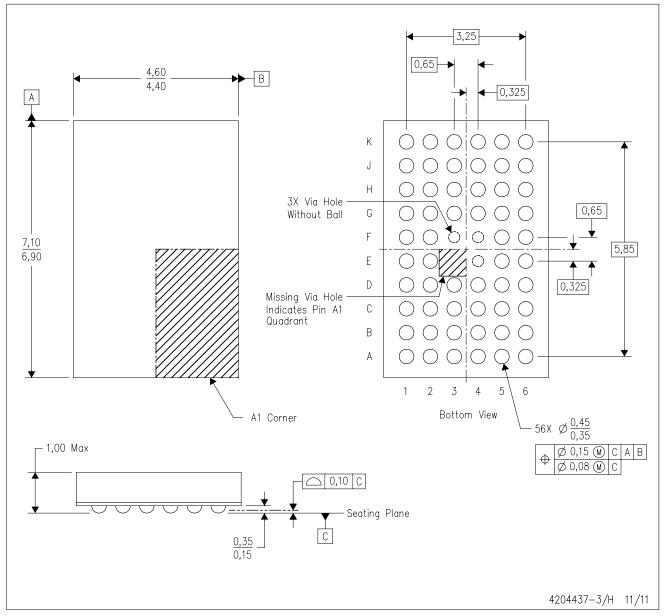


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74ALVCH162373ZQLR	BGA MICROSTAR JUNIOR	ZQL	56	1000	336.6	336.6	28.6
SN74ALVCH162373GR	TSSOP	DGG	48	2000	367.0	367.0	45.0
SN74ALVCH162373LR	SSOP	DL	48	1000	367.0	367.0	55.0

ZQL (R-PBGA-N56)

PLASTIC BALL GRID ARRAY



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MO-285 variation BA-2.
- D. This package is Pb-free. Refer to the 56 GQL package (drawing 4200583) for tin-lead (SnPb).

MicroStar Junior is a trademark of Texas Instruments



DL (R-PDSO-G48)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MO-118

PowerPAD is a trademark of Texas Instruments.



GQL (R-PBGA-N56)

PLASTIC BALL GRID ARRAY



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MO-285 variation BA-2.
- D. This package is tin-lead (SnPb). Refer to the 56 ZQL package (drawing 4204437) for lead-free.



DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold protrusion not to exceed 0,15.

D. Falls within JEDEC MO-153

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Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have *not* been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

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