National Semiconductor

ADVANCE INFORMATION

74ABT16657
16-Bit Transceiver with Parity Generators/Checkers and TRI-STATE® Outputs

General Description

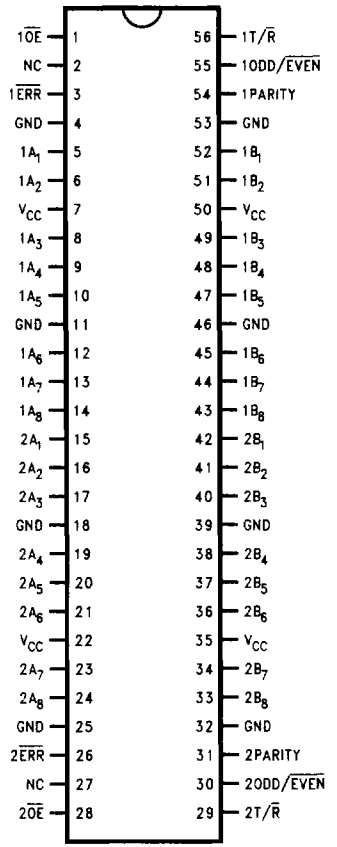
The 'ABT16657 contain two noninverting octal transceivers with separate parity generator/checker circuits and control signals. Odd or even parity is selected by a high or low level on the 1ODD/$\overline{\text{EVEN}}$ or 2ODD/$\overline{\text{EVEN}}$ inputs.

Features

- Guaranteed latch-up
- High impedance glitch free bus loading during entire power up and power down cycle
- Non-destructive hot insertion capability

Connection Diagram

Pin Assignment for SSOP



TL/F/12111–1

Function Table

Function Table (each 8-bit section)

Number of Inputs That Are High	Inputs			Input/ Output	Outputs	
	$\overline{OE}$	T/$\overline{R}$	ODD/$\overline{EVEN}$	Parity	$\overline{ERROR}$	Outputs Mode
0, 2, 4, 6, 8	L	H	H	H	Z	Transmit
	L	H	L	L	Z	Transmit
	L	L	H	H	H	Receive
	L	L	H	L	L	Receive
	L	L	L	H	L	Receive
	L	L	L	L	H	Receive
1, 3, 5, 7	L	H	H	L	Z	Transmit
	L	H	L	H	Z	Transmit
	L	L	H	H	L	Receive
	L	L	H	L	H	Receive
	L	L	L	H	H	Receive
	L	L	L	L	L	Receive
Immaterial	H	X	X	Z	Z	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Functional Description

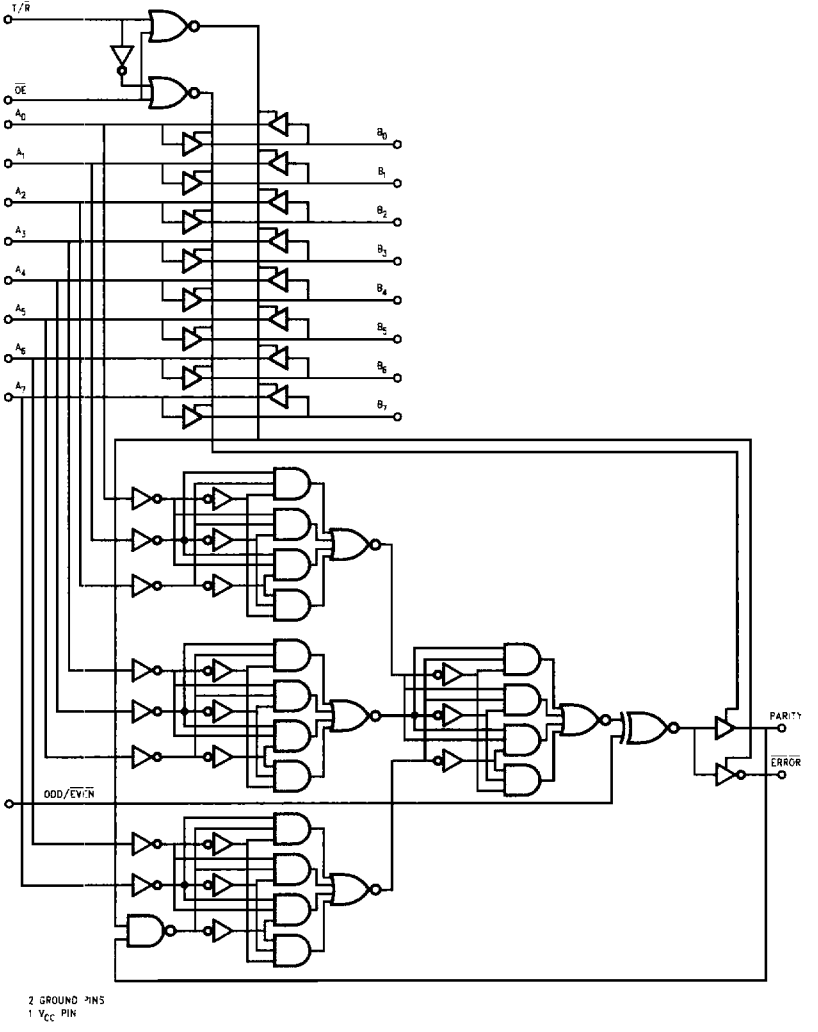
The Transmit/Receive (1T/$\overline{R}$ or 2T/$\overline{R}$) input determines the data flow through the bidirectional transceivers. When the T/$\overline{R}$ (1 or 2) input are high (transmit mode), the data flows from the 1A or 2A port tc the 1B or 2B port. When the T/$\overline{R}$ (1 or 2) inputs are low (receive mode), the data flows from the 1B or 2B port to the 1A or 2A port. When the OE (1 or 2) inputs are high, both the 1A or 2A and the 1B or 2B inputs are TRI-STATE.

Odd or even parity is selected by a high or low level on the 1ODD/$\overline{EVEN}$ or 2ODD/$\overline{EVEN}$ inputs. 1PARITY or 2PARITY carries the parity bit value, it is an output from the parity generator/checker in the transmit mode, and an input to the parity generator/checker in the receive mode.

When transmitting (1T/$\overline{R}$ or 2T/$\overline{R}$ HIGH), the parity generator detects whether an even or odd number of bits on the A port are HIGH and compares these with the condition of the parity select (1ODD/$\overline{EVEN}$ or 2ODD/$\overline{EVEN}$). If the Parity Select is HIGH and an even number of A inputs are HIGH, the Parity output is HIGH.

In receiving mode, (1T/$\overline{R}$ or 2T/$\overline{R}$ LOW), the parity select and number of HIGH inputs on port B are compared to the condition of the Parity input. If an even number of bits on the B port are HIGH, the parity select is HIGH, and the PARITY input is HIGH, then $\overline{ERROR}$ will be HIGH to indicate no error. If an odd number of bits on the B port are HIGH, the parity select is HIGH, and the PARITY input is HIGH, the $\overline{ERROR}$ will be LOW indicating an error.

Functional Block Diagram (each transceiver)



TL/F/12111–2