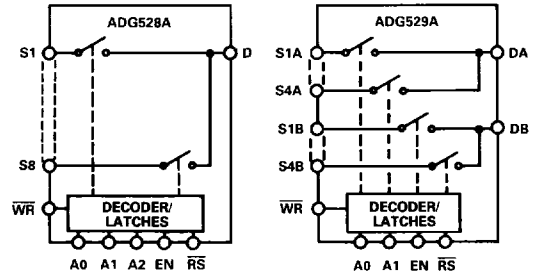


**ADG528A/ADG529A**

**FEATURES**

- 44V Supply Maximum Rating**
- V<sub>SS</sub> to V<sub>DD</sub> Analog Signal Range**
- Single/Dual Supply Specifications**
- Wide Supply Ranges (10.8V to 16.5V)**
- Microprocessor Compatible (100ns  $\overline{WR}$  Pulse)**
- Extended Plastic Temperature Range**  
(-40°C to +85°C)
- Low Leakage (20pA typ)**
- Low Power Dissipation (28mW max)**
- Superior Alternative to:**  
**DG528**  
**DG529**

**ADG528A/ADG529A FUNCTIONAL BLOCK DIAGRAMS**



**GENERAL DESCRIPTION**

The ADG528A and ADG529A are CMOS monolithic analog multiplexers with 8 channels and dual 4 channels respectively. On-chip latches facilitate microprocessor interfacing. The ADG528A switches one of 8 inputs to a common output depending on the state of three binary addresses and an enable input. The ADG529A switches one of 4 differential inputs to a common differential output depending on the state of two binary addresses and an enable input. Both devices have TTL and 5V CMOS logic compatible digital inputs.

The ADG528A and ADG529A are designed on an enhanced LC<sup>2</sup>MOS process which gives an increased signal capability of V<sub>SS</sub> to V<sub>DD</sub> and enables operation over a wide range of supply voltages. The devices can comfortably operate anywhere in the 10.8V to 16.5V single or dual supply range. These multiplexers also feature high switching speeds and low R<sub>ON</sub>.

**ORDERING INFORMATION<sup>1</sup>**

Temperature Range and Package Options <sup>2</sup>		
-40°C to +85°C	-40°C to +85°C	-55°C to +125°C
Plastic DIP (N-18) ADG528AKN ADG529AKN	Hermetic (Q-18) ADG528ABQ ADG529ABQ	Hermetic (Q-18) ADG528ATQ ADG529ATQ
PLCC <sup>3</sup> (P-20A) ADG528AKP ADG529AKP		LC <sup>4</sup> (E-20A) ADG528ATE ADG529ATE

**NOTES**

- <sup>1</sup>To order MIL-STD-883, Class B processed parts, add 883B to part number.
- Contact your local sales office for military data sheet.
- <sup>2</sup>See Section 14 for package outline information.
- <sup>3</sup>PLCC: Plastic Leaded Chip Carrier.
- <sup>4</sup>LC<sup>4</sup>: Leadless Ceramic Chip Carrier.

**PRODUCT HIGHLIGHTS**

1. **Single/Dual Supply Specifications with a Wide Tolerance:**  
The devices are specified in the 10.8V to 16.5V range for both single and dual supplies.
2. **Easily Interfaced:**  
The ADG528A and ADG529A can be easily interfaced with microprocessors. The  $\overline{WR}$  signal latches the state of the address control lines and the enable line. The  $\overline{RS}$  signal clears both the address and enable data in the latches resulting in no output (all switches off).  $\overline{RS}$  can be tied to the microprocessor reset pin.
3. **Extended Signal Range:**  
The enhanced LC<sup>2</sup>MOS processing results in a high breakdown and an increased analog signal range of V<sub>SS</sub> to V<sub>DD</sub>.
4. **Break-Before-Make Switching:**  
Switches are guaranteed break-before-make so that input signals are protected against momentary shorting.
5. **Low Leakage:**  
Leakage currents in the range of 20pA make these multiplexers suitable for high precision circuits.

# SPECIFICATIONS

Dual Supply ( $V_{DD} = +10.8V$  to  $+16.5V$ ,  $V_{SS} = -10.8V$  to  $-16.5V$  unless otherwise noted)

Parameter	ADG528A ADG529A K Version		ADG528A ADG529A B Version		ADG528A ADG529A T Version		Units	Comments
	+25°C	-40°C to +85°C	+25°C	-40°C to +85°C	+25°C	-55°C to +125°C		
<b>ANALOG SWITCH</b>								
Analog Signal Range	$V_{SS}$ $V_{DD}$	$V_{SS}$ $V_{DD}$	$V_{SS}$ $V_{DD}$	$V_{SS}$ $V_{DD}$	$V_{SS}$ $V_{DD}$	$V_{SS}$ $V_{DD}$	V min V max	
$R_{ON}$	280 450 300	600 400	280 450 300	600 400	280 450 300	600	$\Omega$ typ $\Omega$ max $\Omega$ max	$-10V \leq V_S \leq +10V$ , $I_{DS} = 1mA$  $V_{DD} = 15V (\pm 10\%)$ , $V_{SS} = -15V (\pm 10\%)$ $V_{DD} = 15V (\pm 5\%)$ , $V_{SS} = -15V (\pm 5\%)$ $-10V \leq V_S \leq +10V$ , $I_{DS} = 1mA$ $-10V \leq V_S \leq +10V$ , $I_{DS} = 1mA$
$R_{ON}$ Drift	0.6		0.6		0.6	400	%/°C typ	
$R_{ON}$ Match	5		5		5		% typ	
$I_S$ (OFF), Off Input Leakage	0.02 1	50	0.02 1	50	0.02 1	50	nA typ nA max	$V_{S1} = \pm 10V$ , $V_D = V_{S2}$ to $V_{SN} = \mp 10V$
$I_D$ (OFF), Off Output Leakage	0.04 1	100	0.04 1	100	0.04 1	100	nA typ nA max nA max	$V_{S1}$ to $V_{SN} = \pm 10V$ , $V_D = \mp 10V$
$I_D$ (ON), On Channel Leakage	0.04 1	100	0.04 1	100	0.04 1	100	nA typ nA max nA max	$V_{S2}$ to $V_{SN} = \pm 10V$ , $V_D = V_{S1} = \mp 10V$
$I_{DIFF}$ , Differential Off Output Leakage (ADG529A only)		25		25		25	nA max	$V_{S1A:B}$ to $V_{S4A:B} = \pm 10V$ , $V_{DA} = V_{DB} = \mp 10V$
<b>DIGITAL CONTROL</b>								
$V_{INH}$ , Input High Voltage		2.4		2.4		2.4	V min	
$V_{INL}$ , Input Low Voltage		0.8		0.8		0.8	V max	
$I_{IN1}$ or $I_{INH}$		1		1		1	$\mu A$ max	$V_{IN} = 0$ to $V_{DD}$
$C_{IN}$ , Digital Input Capacitance	8		8		8		pF max	
<b>DYNAMIC CHARACTERISTICS<sup>1</sup></b>								
$t_{TRANSITION}$	200 300	400	200 300	400	200 300	400	ns typ ns max	$R_L = 1M\Omega$ , $C_L = 35pF$
$t_{OPEN}$	50 25	10	50 25	10	50 25	10	ns typ ns min	$R_L = 1k\Omega$ , $C_L = 35pF$
$t_{ON}(EN, \overline{WR})$	200 300	400	200 300	400	200 300	400	ns typ ns max	$R_L = 1k\Omega$ , $C_L = 35pF$
$t_{OFF}(EN, \overline{RS})$	200 300	400	200 300	400	200 300	400	ns typ ns max	$R_L = 1k\Omega$ , $C_L = 35pF$
$t_W$ Write Pulse Width	100	120	100	120	100	130	ns min	See Figure 1
$t_S$ Address, Enable Setup Time		100		100		100	ns min	See Figure 1
$t_H$ Address, Enable Hold Time		10		10		10	ns min	See Figure 1
$t_{RS}$ Reset Pulse Width		100		100		100	ns min	See Figure 2
OFF Isolation	68 50		68 50		68 50		dB typ dB min	$V_{IN} = 0.8V$ , $R_L = 1k\Omega$ , $C_L = 15pF$ , $V_S = 7V$ rms, $f = 100kHz$
$C_S$ (OFF)	5		5		5		pF typ	$V_{IN} = 0.8V$
$C_D$ (OFF)	22		22		22		pF typ	$V_{IN} = 0.8V$
ADG528A	11		11		11		pF typ	
ADG529A	4		4		4		pC typ	$R_S = 0\Omega$ , $C_L = 1000pF$ , $V_S = 0V$
$Q_{INJ}$ , Charge Injection								
<b>POWER SUPPLY</b>								
$I_{DD}$	0.6	1.5	0.6	1.5	0.6	1.5	mA typ mA max	$V_{IN} = V_{INL}$ or $V_{INH}$
$I_{SS}$	20	0.2	20	0.2	20	0.2	$\mu A$ typ mA max	$V_{IN} = V_{INL}$ or $V_{INH}$
Power Dissipation	10		10		10		mW typ mW max	
		28		28		28		

**NOTE**

<sup>1</sup>Sample tested at +25°C to ensure compliance.

Specifications subject to change without notice.

Single Supply ( $V_{DD} = +10.8V$  to  $+16.5V$ ,  $V_{SS} = GND = 0V$  unless otherwise noted)

	ADG528A ADG529A K Version		ADG528A ADG529A B Version		ADG528A ADG529A T Version			
Parameter	-40°C to +25°C +85°C		-40°C to +25°C +85°C		-55°C to +25°C +125°C		Units	Comments
<b>ANALOG SWITCH</b>								
ANalog Signal Range	GND	GND	GND	GND	GND	GND	V min V max	GND ≤ V <sub>S</sub> ≤ +10V, I <sub>DS</sub> = 0.5mA
R <sub>ON</sub>	V <sub>DD</sub> 500	V <sub>DD</sub> 500	V <sub>DD</sub> 500	V <sub>DD</sub> 500	V <sub>DD</sub> 500	V <sub>DD</sub> 500	Ω typ	
R <sub>ON</sub> Drift	700	1000	700	1000	700	1000	Ω max	
R <sub>ON</sub> Match	0.6		0.6		0.6		%°C typ	
	5		5		5		% typ	
I <sub>S</sub> (OFF), Off Input Leakage	0.02		0.02		0.02		nA typ nA max	V <sub>S1</sub> = +10V; GND, V <sub>D</sub> = V <sub>S2</sub> to V <sub>SN</sub> = GND/ +10V
I <sub>D</sub> (OFF), Off Output Leakage	0.04		0.04		0.04		nA typ nA max nA max	V <sub>S1</sub> to V <sub>SN</sub> = +10V; GND, V <sub>D</sub> = GND/ +10V
ADG528A	1	100	1	100	1	100		
ADG529A	1	50	1	50	1	50		
I <sub>D</sub> (ON), On Channel Leakage	0.04		0.04		0.04		nA typ nA max nA max	V <sub>S2</sub> to V <sub>SN</sub> = +10V; GND, V <sub>D</sub> = V <sub>S1</sub> = GND/ +10V
ADG528A	1	100	1	100	1	100		
ADG529A	1	50	1	50	1	50		
I <sub>DIFF</sub> , Differential Off Output Leakage (ADG529A only)	25		25		25		nA max	V <sub>S1A,B</sub> to V <sub>S4A,B</sub> = +10V; GND, V <sub>DA</sub> = V <sub>DB</sub> = GND/ +10V
<b>DIGITAL CONTROL</b>								
V <sub>INH</sub> , Input High Voltage	2.4		2.4		2.4		V min	V <sub>IN</sub> = 0 to V <sub>DD</sub>
V <sub>INL</sub> , Input Low Voltage	0.8		0.8		0.8		V max	
I <sub>INL</sub> or I <sub>INH</sub>	1		1		1		μA max	
C <sub>IN</sub> , Digital Input Capacitance	8		8		8		pF max	
<b>DYNAMIC CHARACTERISTICS<sup>1</sup></b>								
t <sub>TRANSITION</sub>	300		300		300		ns typ ns max	R <sub>L</sub> = 1mΩ, C <sub>L</sub> = 35pF
t <sub>OPEN</sub>	50	600	50	600	50	600	ns typ ns min	R <sub>L</sub> = 1kΩ, C <sub>L</sub> = 35pF
t <sub>ON</sub> (EN, $\overline{WR}$ )	250		250		250		ns typ ns max	R <sub>L</sub> = 1kΩ, C <sub>L</sub> = 35pF
t <sub>OFF</sub> (EN, $\overline{RS}$ )	450	600	450	600	450	600	ns typ ns max	R <sub>L</sub> = 1kΩ, C <sub>L</sub> = 35pF
t <sub>w</sub> , Write Pulse Width	250		250		250		ns typ ns max	See Figure 1
t <sub>S</sub> , Address, Enable Setup Time	450	600	450	600	450	600	ns min	
t <sub>H</sub> , Address, Enable Hold Time	100	120	100	120	100	130	ns min	
t <sub>RS</sub> , Reset Pulse Width	100	100	100	100	100	100	ns min	
	100	100	100	100	100	100	ns min	
OFF Isolation	68		68		68		dB typ dB min	V <sub>EN</sub> = 0.8V, R <sub>L</sub> = 1kΩ, C <sub>L</sub> = 15pF, V <sub>S</sub> = 3.5V rms, f = 100kHz
C <sub>S</sub> (OFF)	50		50		50		pF typ	V <sub>EN</sub> = 0.8V
C <sub>D</sub> (OFF)	5		5		5		pF typ	V <sub>EN</sub> = 0.8V
ADG528A	22		22		22		pF typ	R <sub>S</sub> = 0Ω, C <sub>L</sub> = 1000pF, V <sub>S</sub> = 0V
ADG529A	11		11		11		pF typ	
Q <sub>INJ</sub> , Charge Injection	4		4		4		pC typ	
<b>POWER SUPPLY</b>								
I <sub>DD</sub>	0.6		0.6		0.6		mA typ mA max	V <sub>IN</sub> = V <sub>INL</sub> or V <sub>INH</sub>
Power Dissipation	11	1.5	11	1.5	11	1.5	mW typ mW max	
		25		25		25		

NOTE  
<sup>1</sup>Sample tested at +25°C to ensure compliance.  
 Specifications subject to change without notice.

TRUTH TABLES

A2	A1	A0	EN	$\overline{WR}$	$\overline{RS}$	ON SWITCH PAIR
X	X	X	X	$\overline{F}$	1	Retains Previous Switch Condition
X	X	X	X	X	0	NONE (Address and Enable Latches Cleared)
X	X	X	0	0	1	NONE
0	0	0	1	0	1	1
0	0	1	1	0	1	2
0	1	0	1	0	1	3
0	1	1	1	0	1	4
1	0	0	1	0	1	5
1	0	1	1	0	1	6
1	1	0	1	0	1	7
1	1	1	1	0	1	8

X = Don't Care

ADG528A

A1	A0	EN	$\overline{WR}$	$\overline{RS}$	ON SWITCH PAIR
X	X	X	$\overline{F}$	1	Retains Previous Switch Condition
X	X	X	X	0	NONE (Address and Enable Latches Cleared)
X	X	0	0	1	NONE
0	0	1	0	1	1
0	1	1	0	1	2
1	0	1	0	1	3
1	1	1	0	1	4

X = Don't Care

ADG529A

### ABSOLUTE MAXIMUM RATINGS\*

(T<sub>A</sub> = +25°C unless otherwise noted)

V <sub>DD</sub> to V <sub>SS</sub> . . . . .	44V
V <sub>DD</sub> to GND . . . . .	25V
V <sub>SS</sub> to GND . . . . .	-25V
Analog Inputs <sup>1</sup>	
Voltage at S, D . . . . .	V <sub>SS</sub> - 2V to V <sub>DD</sub> + 2V or 20mA, Whichever Occurs First
Continuous Current, S or D . . . . .	20mA
Pulsed Current S or D	
I <sub>ms</sub> Duration, 10% Duty Cycle . . . . .	40mA

### NOTE

<sup>1</sup>Overvoltage at A, EN,  $\overline{WR}$ ,  $\overline{RS}$ , S or D will be clamped by diodes. Current should be limited to the maximum rating above.

\*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

### Digital Inputs<sup>1</sup>

Voltage at A, EN,  $\overline{WR}$ ,  $\overline{RS}$  . . . . . V<sub>SS</sub> - 4V to V<sub>DD</sub> + 4V or 20mA, Whichever Occurs First

### Power Dissipation (Any Package)

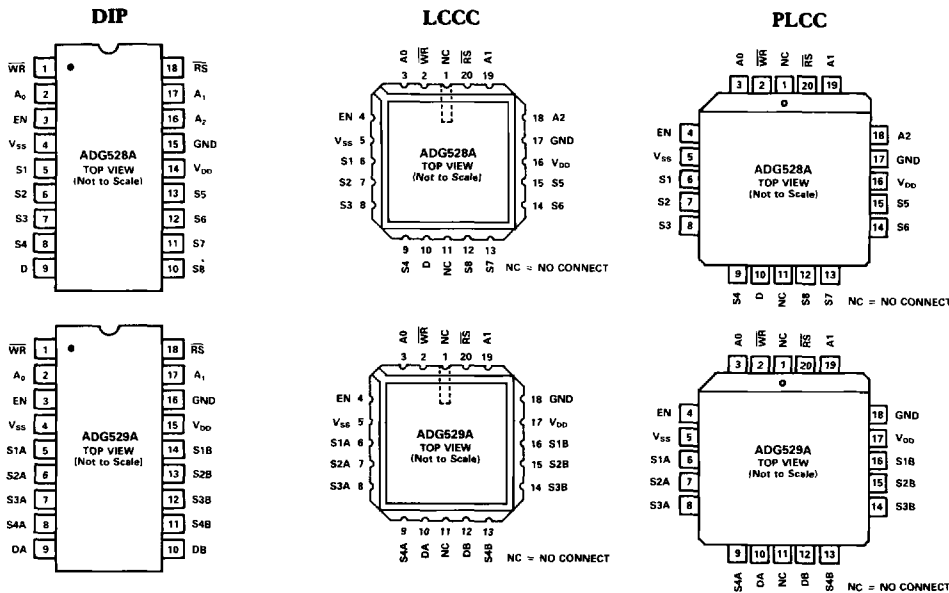
Up to +75°C . . . . . 470mW  
Derates above +75°C by . . . . . 6mW/°C

### Operating Temperature

Commercial (K Version) . . . . . -40°C to +85°C  
Industrial (B Version) . . . . . -40°C to +85°C  
Extended (T Version) . . . . . -55°C to +125°C  
Storage Temperature Range . . . . . -65°C to +150°C  
Lead Temperature (Soldering, 10sec) . . . . . +300°C



### PIN CONFIGURATIONS



### TIMING DIAGRAMS

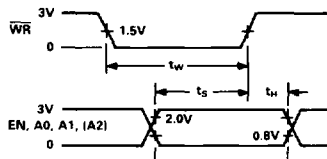


Figure 1

Figure 1 shows the timing sequence for latching the switch address and enable inputs. The latches are level sensitive; therefore, while  $\overline{WR}$  is held low, the latches are transparent and the switches respond to the address and enable inputs. This input data is latched on the rising edge of  $\overline{WR}$ .

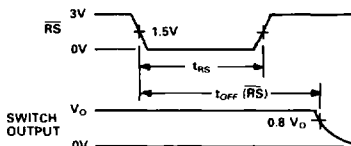


Figure 2

Figure 2 shows the Reset Pulse Width, t<sub>RS</sub>, and Reset Turn-off Time, t<sub>OFF</sub> ( $\overline{RS}$ ).

Note: All digital input signals rise and fall times measured from 10% to 90% of 3V. t<sub>R</sub> = t<sub>F</sub> = 20ns.