

# 54F825,74F825

*54F825 74F825 8-Bit D-Type Flip-Flop*



Literature Number: SNOS217A

## 54F/74F825 8-Bit D-Type Flip-Flop

### General Description

The 'F825 is an 8-bit buffered register. It has Clock Enable and Clear features which are ideal for parity bus interfacing in high performance microprogramming systems. Also included in the 'F825 are multiple enables that allow multi-user control of the interface.

The 'F825 is functionally and pin compatible with AMD's Am29825.

### Features

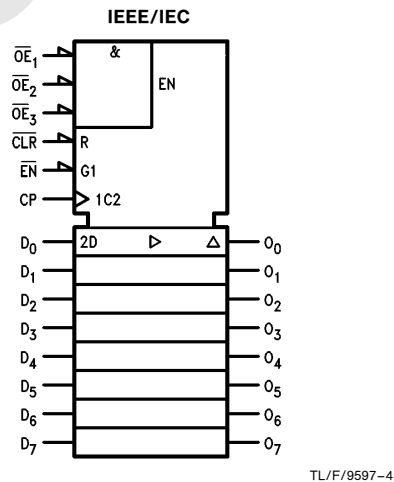
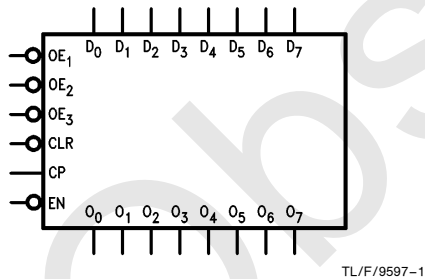
- TRI-STATE® output
- Clock enable and clear
- Multiple output enables
- Direct replacement for AMD's Am24825

Commercial	Military	Package Number	Package Description
74F825SPC		N24C	24-Lead (0.300" Wide) Molded Dual-In-Line
	54F825SDM (Note 2)	J24F	24-Lead (0.300" Wide) Ceramic Dual-In-Line
74F825SC (Note 1)		M24B	24-Lead (0.300" Wide) Molded Small Outline, JEDEC
	54F825FM (Note 2)	W24C	24-Lead Cerpack
	54F825LM (Note 2)	E28A	24-Lead Ceramic Leadless Chip Carrier, Type C

**Note 1:** Devices also available in 13" reel. Use suffix = SCX.

**Note 2:** Military grade device with environmental and burn-in processing. Use suffix = SDMQB, FMQB and LMQB.

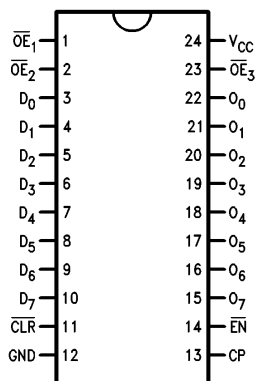
### Logic Symbols



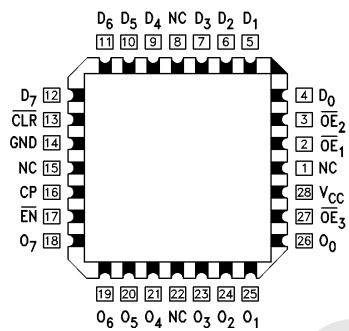
TRI-STATE® is a registered trademark of National Semiconductor Corporation.

## Connection Diagrams

Pin Assignment  
for DIP, SOIC and Flatpak



Pin Assignment  
for LCC



TL/F/9597-3

TL/F/9597-2

## Unit Loading/Fan Out

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
D <sub>0</sub> –D <sub>7</sub>	Data Inputs	1.0/1.0	20 $\mu$ A/–0.6 mA
O <sub>0</sub> –O <sub>7</sub>	TRI-STATE Data Outputs	150/40 (33.3)	–3 mA/24 mA (20 mA)
$\overline{OE}_1, \overline{OE}_2, \overline{OE}_3$	Output Enable Input	1.0/1.0	20 $\mu$ A/–0.6 mA
EN	Clock Enable	1.0/1.0	20 $\mu$ A/–0.6 mA
$\overline{CLR}$	Clear	1.0/1.0	20 $\mu$ A/–0.6 mA
CP	Clock Input	1.0/2.0	20 $\mu$ A/–1.2 mA

## Functional Description

The 'F825 consists of eight D-type edge-triggered flip-flops. This device has TRI-STATE true outputs and is organized in broadside pinning. In addition to the clock and output enable pins, the buffered clock (CP) and buffered Output Enable ( $\overline{OE}$ ) are common to all flip-flops. The flip-flops will store the state of their individual D inputs that meet the setup and hold times requirements on the LOW-to-HIGH CP transition. With the  $\overline{OE}$  LOW the contents of the flip-flops are available at the outputs. When the  $\overline{OE}$  is HIGH, the outputs go to the high impedance state. Operation of the  $\overline{OE}$

input does not affect the state of the flip-flops. The 'F825 has Clear ( $\overline{CLR}$ ) and Clock Enable ( $\overline{EN}$ ) pins.

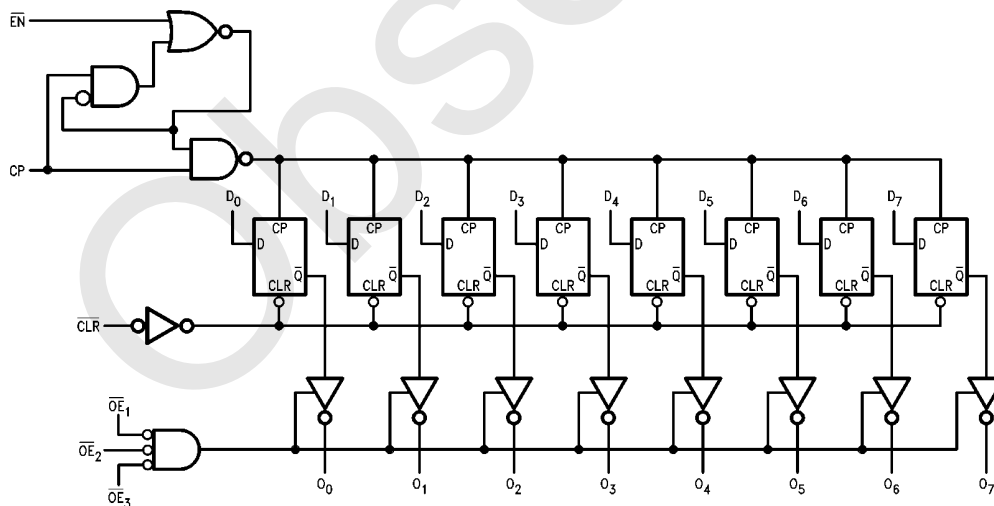
When the  $\overline{CLR}$  is LOW and the  $\overline{OE}$  is LOW the outputs are LOW. When  $\overline{CLR}$  is HIGH, data can be entered into the flip-flops. When  $\overline{EN}$  is LOW, data on the inputs is transferred to the outputs on the LOW-to-HIGH clock transition. When the  $\overline{EN}$  is HIGH the outputs do not change state, regardless of the data or clock input transitions.

Function Table

Inputs					Internal	Output	Function
$\overline{OE}$	$\overline{CLR}$	$\overline{EN}$	CP	D	$\overline{Q}$	O	
H	H	L	H	X	NC	Z	Hold
H	H	L	L	X	NC	Z	Hold
H	H	H	X	X	NC	Z	Hold
L	H	H	X	X	NC	NC	Hold
H	L	X	X	X	H	Z	Clear
L	L	X	X	X	H	L	Clear
H	H	L	↗	L	H	Z	Load
H	H	L	↘	H	L	Z	Load
L	H	L	↗	L	H	L	Data Available
L	H	L	↘	H	L	H	Data Available
L	H	L	H	X	NC	NC	No Change in Data
L	H	L	L	X	NC	NC	No Change in Data

L = LOW Voltage Level  
H = HIGH Voltage Level  
X = Immaterial  
Z = High Impedance  
↗ = LOW-to-HIGH Transition  
↘ = No Change

## Logic Diagram



TL/F/9597-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +175°C
Plastic	-55°C to +150°C
V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	
Standard Output	-0.5V to V <sub>CC</sub>
TRI-STATE Output	-0.5V to +5.5V

Current Applied to Output in LOW State (Max) twice the rated I<sub>OL</sub> (mA)

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

## Recommended Operating Conditions

Free Air Ambient Temperature	
Military	-55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

## DC Electrical Characteristics

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions	
		Min	Typ	Max				
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal	
V <sub>IL</sub>	Input LOW Voltage				V		Recognized as a LOW Signal	
V <sub>CD</sub>	Input Clamp Diode Voltage				V	Min	I <sub>IN</sub> = -18 mA	
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub>	2.5		V	Min	I <sub>OH</sub> = -1 mA	
		54F 10% V <sub>CC</sub>	2.4				I <sub>OH</sub> = -3 mA	
		74F 10% V <sub>CC</sub>	2.5				I <sub>OH</sub> = -1 mA	
		74F 10% V <sub>CC</sub>	2.4				I <sub>OH</sub> = -3 mA	
		74F 5% V <sub>CC</sub>	2.7				I <sub>OH</sub> = -1 mA	
		74F 5% V <sub>CC</sub>	2.7				I <sub>OH</sub> = -3 mA	
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub>		0.5	V	Min	I <sub>OL</sub> = 20 mA	
		74F 10% V <sub>CC</sub>		0.5			I <sub>OL</sub> = 24 mA	
I <sub>IH</sub>	Input HIGH Current	54F		20.0	μA	Max	V <sub>IN</sub> = 2.7V	
		74F		5.0				
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F		100	μA	Max	V <sub>IN</sub> = 7.0V	
		74F		7.0				
I <sub>CEX</sub>	Output HIGH Leakage Current	54F		250	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>	
		74F		50				
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded	
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded	
I <sub>IL</sub>	Input LOW Current			-0.6	mA	Max	V <sub>IN</sub> = 0.5V	
I <sub>OZH</sub>	Output Leakage Current			50	μA	Max	V <sub>OUT</sub> = 2.7V	
I <sub>OZL</sub>	Output Leakage Current			-50	μA	Max	V <sub>OUT</sub> = 0.5V	
I <sub>OS</sub>	Output Short-Circuit Current			-60	mA	Max	V <sub>OUT</sub> = 0V	
I <sub>ZZ</sub>	Buss Drainage Test			500	μA	0.0V	V <sub>OUT</sub> = 5.25V	
I <sub>CCZ</sub>	Power Supply Current			75	90	mA	Max	V <sub>O</sub> = HIGH Z

## AC Electrical Characteristics

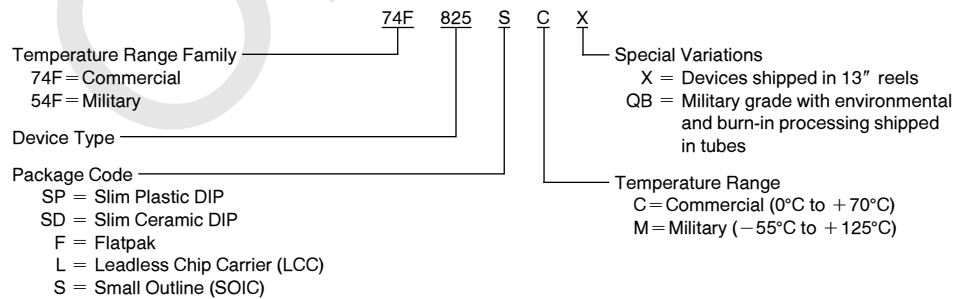
Symbol	Parameter	74F			54F		74F		Units
		$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$		
		Min	Typ	Max	Min	Max	Min	Max	
$f_{\text{max}}$	Maximum Clock Frequency	100	160		60		70		MHz
$t_{\text{PLH}}$	Propagation Delay	2.0	6.5	9.5	2.0	10.5	2.0	10.5	ns
$t_{\text{PHL}}$	CP to $O_n$	2.0	6.6	9.5	2.0	10.5	2.0	10.5	
$t_{\text{PHL}}$	Propagation Delay $\overline{\text{CLR}}$ to $O_n$	4.0	7.4	12.0	4.0	13.0	4.0	13.0	ns
$t_{\text{PZH}}$	Output Enable Time	2.0	6.5	10.5	2.0	13.0	2.0	11.5	ns
$t_{\text{PZL}}$	$\overline{\text{OE}}$ to $O_n$	2.0	6.6	10.5	2.0	13.0	2.0	11.5	
$t_{\text{PHZ}}$	Output Disable Time	1.5	3.5	7.0	1.0	7.5	1.5	7.5	ns
$t_{\text{P LZ}}$	$\overline{\text{OE}}$ to $O_n$	1.5	3.3	7.0	1.0	7.5	1.5	7.5	

## AC Operating Requirements

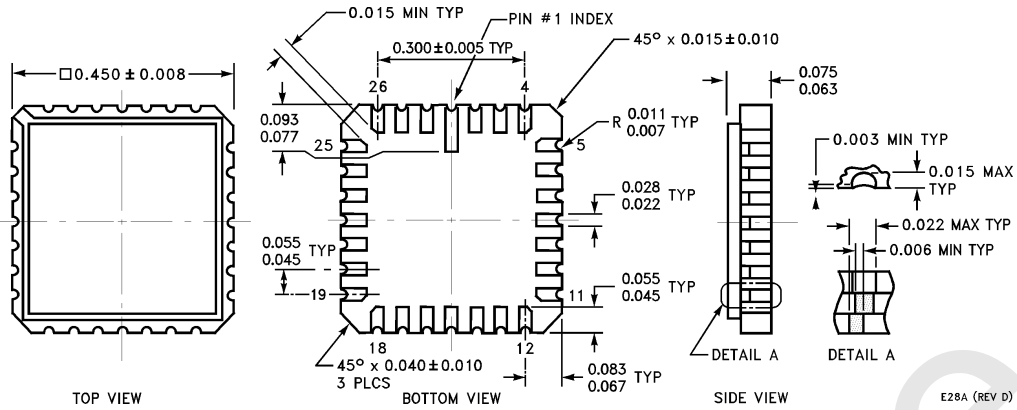
Symbol	Parameter	74F		54F		74F		Units
		$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A, V_{CC} = \text{Mil}$		$T_A, V_{CC} = \text{Com}$		
		Min	Max	Min	Max	Min	Max	
$t_{\text{s(H)}}$	Setup Time, HIGH or LOW	2.5		4.0		3.0		ns
$t_{\text{s(L)}}$	$D_n$ to CP	2.5		4.0		3.0		
$t_{\text{h(H)}}$	Hold Time, HIGH or LOW	2.5		2.5		2.5		ns
$t_{\text{h(L)}}$	$D_n$ to CP	2.5		2.5		2.5		
$t_{\text{s(H)}}$	Setup Time, HIGH or LOW	4.5		5.0		5.0		ns
$t_{\text{s(L)}}$	$\overline{\text{EN}}$ to CP	2.5		3.0		3.0		
$t_{\text{h(H)}}$	Hold Time, HIGH or LOW	2.0		3.0		1.0		ns
$t_{\text{h(L)}}$	$\overline{\text{EN}}$ to CP	0		2.0		0		
$t_{\text{w(H)}}$	CP Pulse Width	5.0		6.0		6.0		ns
$t_{\text{w(L)}}$	HIGH or LOW	5.0		6.0		6.0		ns
$t_{\text{w(L)}}$	$\overline{\text{CLR}}$ Pulse Width, LOW	5.0		5.0		5.0		ns
$t_{\text{rec}}$	$\overline{\text{CLR}}$ Recovery Time	5.0		5.0		5.0		ns

## Ordering Information

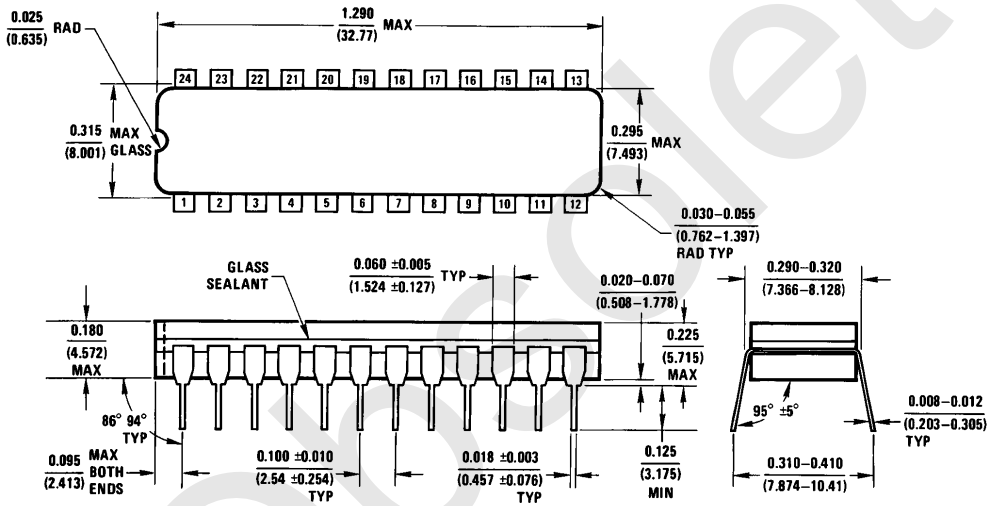
The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



**Physical Dimensions** inches (millimeters)

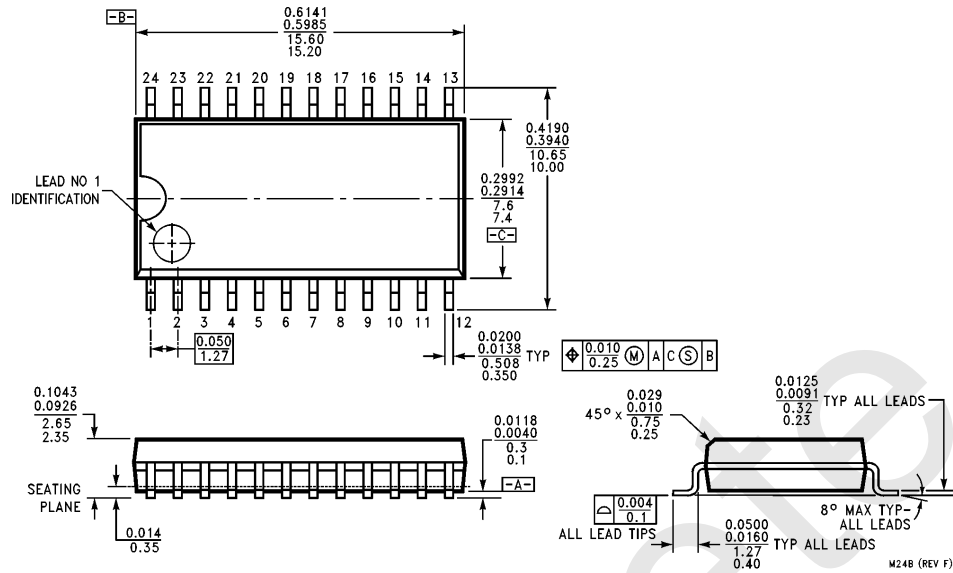


**28-Lead Ceramic Leadless Chip Carrier (L)  
NS Package Number E28A**

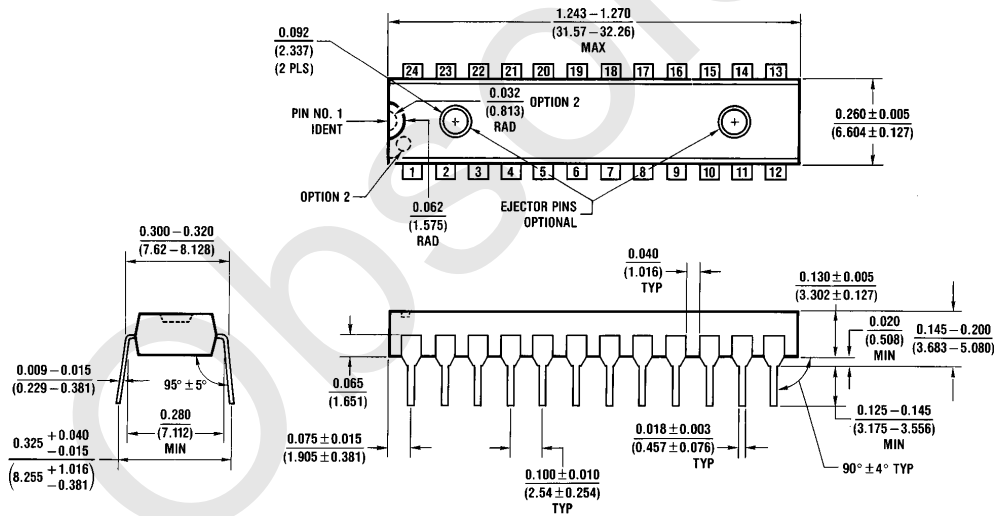


**24-Lead (0.300" Wide) Ceramic  
Dual-In-Line Package (SD)  
NS Package Number J24F**

**Physical Dimensions** inches (millimeters) (Continued)



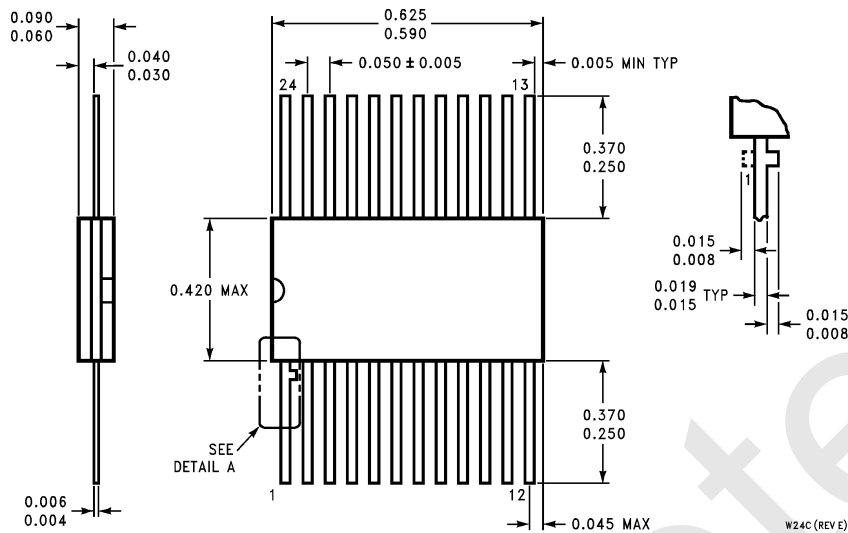
**24-Lead (0.300" Wide) Molded Small Outline Package, JEDEC (S)  
NS Package Number M24B**



**24-Lead (0.300" Wide) Molded Dual-In-Line Package (SP)  
NS Package Number N24C**



**Physical Dimensions** inches (millimeters) (Continued)



**24-Lead Ceramic Flatpak (F)  
NS Package Number W24C**

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