

# 100351 Low Power Hex D Flip-Flop

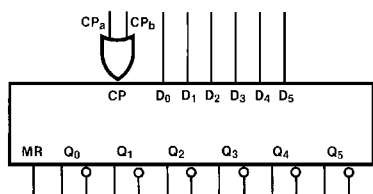
## General Description

The 100351 contains six D-type edge-triggered, master/slave flip-flops with true and complement outputs, a pair of common Clock inputs (CP<sub>a</sub> and CP<sub>b</sub>) and common Master Reset (MR) input. Data enters a master when both CP<sub>a</sub> and CP<sub>b</sub> are LOW and transfers to the slave when CP<sub>a</sub> and CP<sub>b</sub> (or both) go HIGH. The MR input overrides all other inputs and makes the Q outputs LOW. All inputs have 50 kΩ pull-down resistors.

## Features

- 40% power reduction of the 100151
- 2000V ESD protection
- Pin/function compatible with 100151
- Voltage compensated operating range: -4.2V to -5.7V
- Available to industrial grade temperature range

## Ordering Code: Logic Symbol

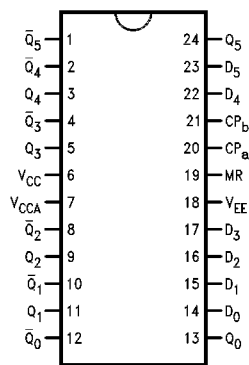


DS009885-11

Pin Names	Description
D <sub>0</sub> -D <sub>5</sub>	Data Inputs
CP <sub>a</sub> , CP <sub>b</sub>	Common Clock Inputs
MR	Asynchronous Master Reset Input
Q <sub>0</sub> -Q <sub>5</sub>	Data Outputs
$\bar{Q}_0$ - $\bar{Q}_5$	Complementary Data Outputs

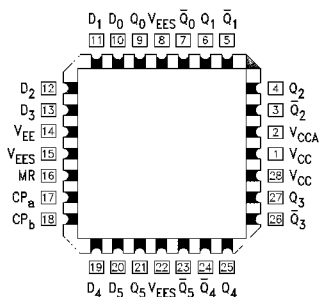
## Connection Diagrams

24-Pin DIP/SOIC



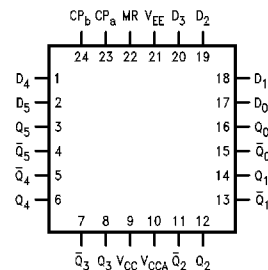
DS009885-1

28-Pin PCC



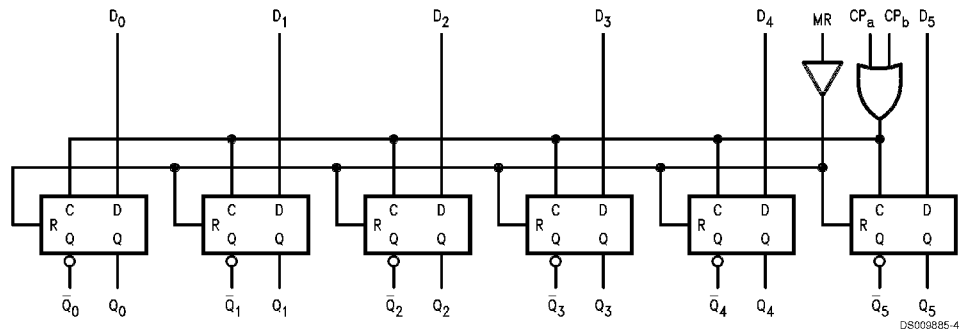
DS009885-3

24-Pin Quad Cerpak



DS009885-2

## Logic Diagram



## Truth Tables (Each Flip-flop)

### Synchronous Operation

Inputs				Outputs
$D_n$	$CP_a$	$CP_b$	MR	$Q_n(t+1)$
L	↗	L	L	L
H	↗	L	L	H
L	L	↗	L	L
H	L	↗	L	H
X	H	↗	L	$Q_n(t)$
X	↗	H	L	$Q_n(t)$
X	L	L	L	$Q_n(t)$

### Asynchronous Operation

Inputs				Outputs
$D_n$	$CP_a$	$CP_b$	MR	$Q_n(t+1)$
X	X	X	H	L

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Don't Care  
 t = Time before CP positive transition  
 t+1 = Time after CP positive transition  
 ↗ = LOW-to-HIGH transition

## Absolute Maximum Ratings (Note 1)

Above which the useful life may be impaired

Storage Temperature ( $T_{STG}$ )	-65°C to +150°C
Maximum Junction Temperature ( $T_J$ )	
Ceramic	+175°C
Plastic	+150°C
$V_{EE}$ Pin Potential to Ground Pin	-7.0V to +0.5V
Input Voltage (DC)	$V_{EE}$ to +0.5V
Output Current (DC Output HIGH)	-50 mA
ESD (Note 2)	≥2000V

## Recommended Operating Conditions

Case Temperature ( $T_C$ )	
Commercial	0°C to +85°C
Industrial	-40°C to +85°C
Military	-55°C to +125°C
Supply Voltage ( $V_{EE}$ )	-5.7V to -4.2V

**Note 1:** Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** ESD testing conforms to MIL-STD-883, Method 3015.

## Commercial Version

### DC Electrical Characteristics

$V_{EE} = -4.2V$  to  $-5.7V$ ,  $V_{CC} = V_{CCA} = GND$ ,  $T_C = 0^\circ C$  to  $+85^\circ C$  (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions	
$V_{OH}$	Output HIGH Voltage	-1025	-955	-870	mV	$V_{IN} = V_{IH}$ (Max) or $V_{IL}$ (Min)	Loading with 50Ω to -2.0V
$V_{OL}$	Output LOW Voltage	-1830	-1705	-1620			
$V_{OHC}$	Output HIGH Voltage	-1035			mV	$V_{IN} = V_{IH}$ (Min) or $V_{IL}$ (Max)	Loading with 50Ω to -2.0V
$V_{OLC}$	Output LOW Voltage			-1610			
$V_{IH}$	Input HIGH Voltage	-1165		-870	mV	Guaranteed HIGH Signal for All Inputs	
$V_{IL}$	Input LOW Voltage	-1830		-1475	mV	Guaranteed LOW Signal for All Inputs	
$I_{IL}$	Input LOW Current	0.50			μA	$V_{IN} = V_{IL}$ (Min)	
$I_{IH}$	Input HIGH Current MR D <sub>0</sub> -D <sub>5</sub> CP <sub>a</sub> , CP <sub>b</sub>			350	μA	$V_{IN} = V_{IH}$ (Max)	
				240			
				350			
$I_{EE}$	Power Supply Current	-129		-62	mA	Inputs Open	

**Note 3:** The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

### DIP AC Electrical Characteristics

$V_{EE} = -4.2V$  to  $-5.7V$ ,  $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = 0^\circ C$		$T_C = +25^\circ C$		$T_C = +85^\circ C$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
$f_{max}$	Toggle Frequency	375		375		375		MHz	Figures 2, 3
$t_{PLH}$	Propagation Delay CP <sub>a</sub> , CP <sub>b</sub> to Output	0.80	2.00	0.80	2.0	0.90	2.10	ns	Figures 1, 3
$t_{PLH}$	Propagation Delay MR to Output	1.10	2.30	1.10	2.30	1.20	2.40	ns	Figures 1, 4
$t_{TLH}$	Transition Time 20% to 80%, 80% to 20%	0.35	1.20	0.35	1.20	0.35	1.20	ns	Figures 1, 3
$t_s$	Setup Time D <sub>0</sub> -D <sub>5</sub> MR (Release Time)	0.40		0.40		0.40		ns	Figure 5
		1.60		1.60		1.60			Figure 4
		0.80		0.80		0.80		ns	Figure 5
$t_{pw(H)}$	Pulse Width HIGH CP <sub>a</sub> , CP <sub>b</sub> , MR	2.00		2.00		2.00		ns	Figures 3, 4

## SOIC, PCC and Cerpak AC Electrical Characteristics

$V_{EE} = -4.2V$  to  $-5.7V$ ,  $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = 0^\circ C$		$T_C = +25^\circ C$		$T_C = +85^\circ C$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
$f_{max}$	Toggle Frequency	375		375		375		MHz	Figures 2, 3
$t_{PLH}$	Propagation Delay	0.80	1.80	0.80	1.80	0.90	1.90	ns	Figures 1, 3
$t_{PHL}$	$CP_a$ , $CP_b$ to Output								
$t_{PLH}$	Propagation Delay	1.10	2.10	1.10	2.10	1.20	2.20	ns	Figures 1, 4
$t_{PHL}$	MR to Output								
$t_{TLH}$	Transition Time	0.45	1.70	0.45	1.60	0.45	1.70	ns	Figures 1, 3
$t_{THL}$	20% to 80%, 80% to 20%								
$t_s$	Setup Time								Figure 5
	$D_o-D_5$	0.30		0.30		0.30		ns	
	MR (Release Time)	1.50		1.50		1.50		ns	Figure 4
$t_H$	Hold Time	0.80		0.80		0.80		ns	Figure 5
	$D_o-D_5$								
$t_{pw(H)}$	Pulse Width HIGH	2.00		2.00		2.00		ns	Figures 3, 4
	$CP_a$ , $CP_b$ , MR								
$t_{OSHL}$	Maximum Skew Common Edge Output-to-Output Variation Clock to Output Path		220		220		220	ps	PCC only (Note 4)
$t_{OSLH}$	Maximum Skew Common Edge Output-to-Output Variation Clock to Output Path		210		210		210	ps	PCC only (Note 4)
$t_{OST}$	Maximum Skew Opposite Edge Output-to-Output Variation Clock to Output Path		240		240		240	ps	PCC only (Note 4)
$t_{PS}$	Maximum Skew Pin (Signal) Transition Variation Clock to Output Path		230		230		230	ps	PCC only (Note 4)

**Note 4:** Output-to-Output Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction either HIGH to LOW ( $t_{OSHL}$ ), or LOW to HIGH ( $t_{OSLH}$ ), or in opposite directions both HL and LH ( $t_{OST}$ ). Parameters  $t_{OST}$  and  $t_{PS}$  guaranteed by design.

## Industrial Version

### PCC DC Electrical Characteristics

$V_{EE} = -4.2V$  to  $-5.7V$ ,  $V_{CC} = V_{CCA} = GND$ ,  $T_C = 0^\circ C$  to  $+85^\circ C$  (Note 5)

Symbol	Parameter	$T_C = -40^\circ C$		$T_C = 0^\circ$ to $+85^\circ C$		Units	Conditions	
		Min	Max	Min	Max			
$V_{OH}$	Output HIGH Voltage	-1085	-870	-1025	-870	mV	$V_{IN} = V_{IH}$ (Max)	Loading with $50\Omega$ to $-2.0V$
$V_{OL}$	Output LOW Voltage	-1830	-1575	-1830	-1620		or $V_{IL}$ (Min)	
$V_{OHC}$	Output HIGH Voltage	-1095		-1035		mV	$V_{IN} = V_{IH}$ (Min)	Loading with $50\Omega$ to $-2.0V$
$V_{OLC}$	Output LOW Voltage		-1565		-1610		or $V_{IL}$ (Max)	
$V_{IH}$	Input HIGH Voltage	-1170	-870	-1165	-870	mV	Guaranteed HIGH Signal for All Inputs	
$V_{IL}$	Input LOW Voltage	-1830	-1480	-1830	-1475	mV	Guaranteed LOW Signal for All Inputs	
$I_{IL}$	Input LOW Current	0.50		0.50		$\mu A$	$V_{IN} = V_{IL}$ (Min)	
$I_{IH}$	Input HIGH Current							
	MR		350		350	$\mu A$	$V_{IN} = V_{IH}$ (Max)	
	$D_o-D_5$		240		240			
	$CP_a$ , $CP_b$		350		350			

## PCC DC Electrical Characteristics (Continued)

$V_{EE} = -4.2V$  to  $-5.7V$ ,  $V_{CC} = V_{CCA} = GND$ ,  $T_C = 0^\circ C$  to  $+85^\circ C$  (Note 5)

Symbol	Parameter	$T_C = -40^\circ C$		$T_C = 0^\circ$ to $+85^\circ C$		Units	Conditions
		Min	Max	Min	Max		
$I_{EE}$	Power Supply Current	-129	-62	-129	-62	mA	Inputs Open

**Note 5:** The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

## PCC AC Electrical Characteristics

$V_{EE} = -4.2V$  to  $-5.7V$ ,  $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = -40^\circ C$		$T_C = +25^\circ C$		$T_C = +85^\circ C$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
$f_{max}$	Toggle Frequency	375		375		375		MHz	Figures 2, 3
$t_{PLH}$	Propagation Delay	0.80	1.80	0.80	1.80	0.90	1.90	ns	Figures 1, 3
$t_{PHL}$	$CP_a$ , $CP_b$ to Output								
$t_{PLH}$	Propagation Delay	1.10	2.10	1.10	2.10	1.20	2.20	ns	Figures 1, 4
$t_{PHL}$	MR to Output								
$t_{TLH}$	Transition Time	0.45	1.70	0.45	1.60	0.45	1.70	ns	Figures 1, 3
$t_{THL}$	20% to 80%, 80% to 20%								
$t_s$	Setup Time								Figure 5
	$D_o - D_s$	0.60		0.30		0.30		ns	
	MR (Release Time)	2.20		1.50		1.50			Figure 4
$t_H$	Hold Time	0.60		0.90		0.90		ns	Figure 5
	$D_o - D_s$								
$t_{pw(H)}$	Pulse Width HIGH	2.00		2.00		2.00		ns	Figures 3, 4
	$CP_a$ , $CP_b$ , MR								

## Military Version—Preliminary

### DC Electrical Characteristics

$V_{EE} = -4.2V$  to  $-5.7V$ ,  $V_{CC} = V_{CCA} = GND$ ,  $T_C = -55^\circ C$  to  $+125^\circ C$

Symbol	Parameter	Min	Max	Units	$T_C$	Conditions	Notes	
$V_{OH}$	Output HIGH Voltage	-1025	-870	mV	$0^\circ C$ to $+125^\circ C$	$V_{IN} = V_{IH}$ (Max) or $V_{IL}$ (Min)	Loading with $50\Omega$ to $-2.0V$	(Notes 6, 7, 8)
		-1085	-870	mV	$-55^\circ C$			
$V_{OL}$	Output LOW Voltage	-1830	-1620	mV	$0^\circ C$ to $+125^\circ C$	$V_{IN} = V_{IH}$ (Min) or $V_{IL}$ (Max)	Loading with $50\Omega$ to $-2.0V$	(Notes 6, 7, 8)
		-1830	-1555	mV	$-55^\circ C$			
$V_{OHc}$	Output HIGH Voltage	-1035		mV	$0^\circ C$ to $+125^\circ C$	$V_{IN} = V_{IH}$ (Min) or $V_{IL}$ (Max)	Loading with $50\Omega$ to $-2.0V$	(Notes 6, 7, 8)
		-1085		mV	$-55^\circ C$			
$V_{OLc}$	Output LOW Voltage		-1610	mV	$0^\circ C$ to $+125^\circ C$	$V_{IN} = V_{IH}$ (Min) or $V_{IL}$ (Max)	Loading with $50\Omega$ to $-2.0V$	(Notes 6, 7, 8)
			-1555	mV	$-55^\circ C$			
$V_{IH}$	Input HIGH Voltage	-1165	-870	mV	$-55^\circ C$ to $+125^\circ C$	Guaranteed HIGH Signal for All Inputs	(Notes 6, 7, 8, 9)	
$V_{IL}$	Input LOW Voltage	-1830	-1475	mV	$-55^\circ C$ to $+125^\circ C$	Guaranteed LOW Signal for All Inputs	(Notes 6, 7, 8, 9)	
$I_{IL}$	Input LOW Current	0.50		$\mu A$	$-55^\circ C$ to $+125^\circ C$	$V_{EE} = -4.2V$ $V_{IN} = V_{IL}$ (Min)	(Notes 6, 7, 8)	

## DC Electrical Characteristics (Continued)

$V_{EE} = -4.2V$  to  $-5.7V$ ,  $V_{CC} = V_{CCA} = GND$ ,  $T_C = -55^\circ C$  to  $+125^\circ C$

Symbol	Parameter	Min	Max	Units	$T_C$	Conditions	Notes
$I_{IH}$	Input HIGH Current					$V_{EE} = -5.7V$ $V_{IN} = V_{IH} (Max)$	(Notes 6, 7, 8)
	CP, MR $D_0-D_5$		350 240	$\mu A$	$0^\circ C$ to $+125^\circ C$		
	CP, MR $D_0-D_5$		500 340	$\mu A$	$-55^\circ C$		
$I_{EE}$	Power Supply Current	-135	-50	mA	$-55^\circ C$ to $+125^\circ C$	Inputs Open	(Notes 6, 7, 8)

**Note 6:** F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals  $-55^\circ C$ ), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

**Note 7:** Screen tested 100% on each device at  $-55^\circ C$ ,  $+25^\circ C$ , and  $+125^\circ C$ , Subgroups 1, 2, 3, 7, and 8.

**Note 8:** Sample tested (Method 5005, Table I) on each manufactured lot at  $-55^\circ C$ ,  $+25^\circ C$ , and  $+125^\circ C$ , Subgroups A1, 2, 3, 7, and 8.

**Note 9:** Guaranteed by applying specified input condition and testing  $V_{OH}/V_{OL}$ .

## AC Electrical Characteristics

$V_{EE} = -4.2V$  to  $-5.7V$ ,  $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = -55^\circ C$		$T_C = +25^\circ C$		$T_C = +125^\circ C$		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
$f_{max}$	Toggle Frequency	375		375		375		MHz	Figures 2, 3	(Note 13)
$t_{PLH}$	Propagation Delay	0.50	2.40	0.60	2.20	0.60	2.60	ns	Figures 1, 3	(Notes 10, 11, 12)
$t_{PHL}$	CP <sub>a</sub> , CP <sub>b</sub> to Output									
$t_{PLH}$	Propagation Delay	0.70	2.70	0.80	2.60	0.80	2.90	ns	Figures 1, 4	
$t_{PHL}$	MR to Output									
$t_{TLH}$	Transition Time	0.20	1.60	0.20	1.60	0.20	1.60	ns	Figures 1, 3	(Note 13)
$t_{THL}$	20% to 80%, 80% to 20%									
$t_s$	Setup Time									
	$D_0-D_5$ MR (Release Time)	0.90 1.60		0.80 1.80		0.90 2.60		ns	Figure 5 Figure 4	
$t_h$	Hold Time	1.50		1.40		1.60		ns	Figure 5	
	$D_0-D_5$									
$t_{pw(H)}$	Pulse Width HIGH	2.00		2.00		2.00		ns	Figures 3, 4	
	CP <sub>a</sub> , CP <sub>b</sub> , MR									

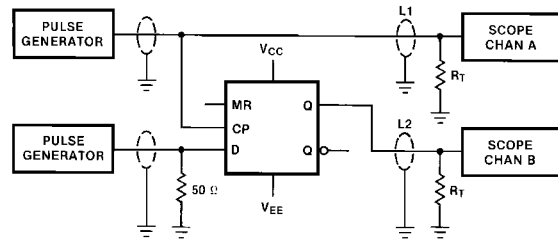
**Note 10:** F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals  $-55^\circ C$ ), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

**Note 11:** Screen tested 100% on each device at  $+25^\circ C$ , Temperature only, Subgroup A9.

**Note 12:** Sample tested (Method 5005, Table I) on each Mfg. lot at  $+25^\circ C$ , Subgroup A9, and at  $+125^\circ C$ , and  $-55^\circ C$  Temperature, Subgroups A10 and A11.

**Note 13:** Not tested at  $+25^\circ C$ ,  $+125^\circ C$  and  $-55^\circ C$  Temperature (design characterization data).

## Test Circuitry

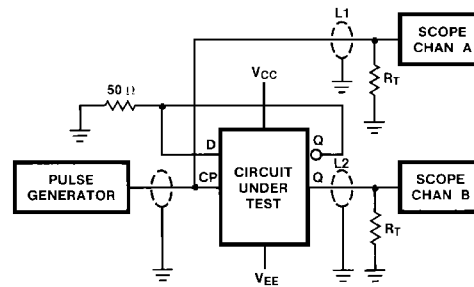


DS009885-5

### Notes:

$V_{CC}$ ,  $V_{CCA} = +2V$ ,  $V_{EE} = -2.5V$   
 $L1$  and  $L2$  = equal length  $50\Omega$  impedance lines  
 $R_T = 50\Omega$  terminator internal to scope  
 Decoupling  $0.1 \mu F$  from GND to  $V_{CC}$  and  $V_{EE}$   
 All unused outputs are loaded with  $50\Omega$  to GND  
 $C_L$  = Fixture and stray capacitance  $\leq 3$  pF

FIGURE 1. AC Test Circuit



DS009885-6

### Notes:

$V_{CC}$ ,  $V_{CCA} = +2V$ ,  $V_{EE} = -2.5V$   
 $L1$  and  $L2$  = equal length  $50\Omega$  impedance lines  
 $R_T = 50\Omega$  terminator internal to scope  
 Decoupling  $0.1 \mu F$  from GND to  $V_{CC}$  and  $V_{EE}$   
 All unused outputs are loaded with  $50\Omega$  to GND  
 $C_L$  = jig and stray capacitance  $\leq 3$  pF

FIGURE 2. Toggle Frequency Test Circuit

## Switching Waveforms

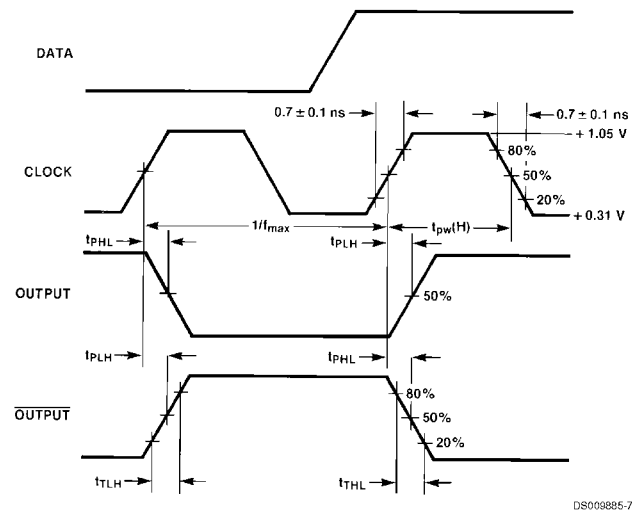


FIGURE 3. Propagation Delay (Clock) and Transition Times

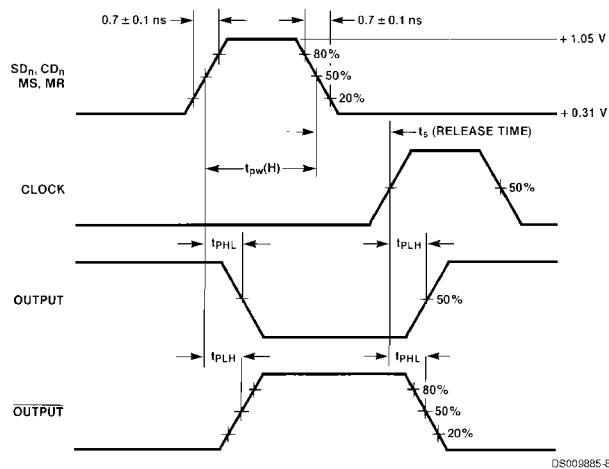
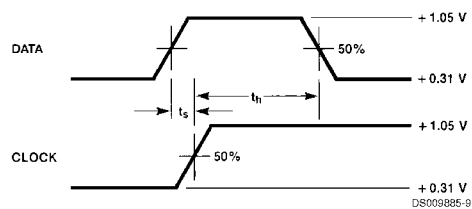


FIGURE 4. Propagation Delay (Reset)



**Notes:**

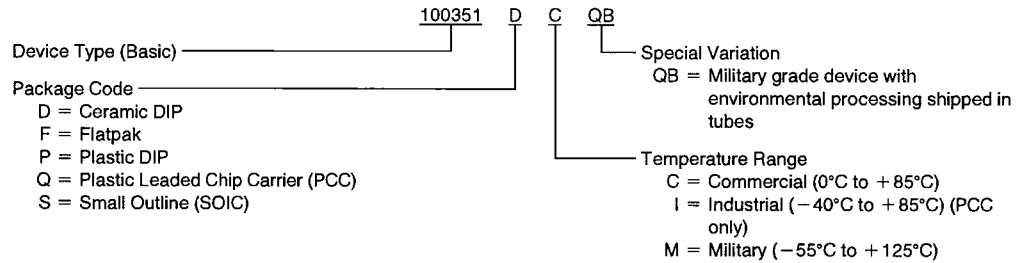
- $t_s$  is the minimum time before the transition of the clock that information must be present at the data input.
- $t_h$  is the minimum time after the transition of the clock that information must remain unchanged at the data input.

FIGURE 5. Setup and Hold Time

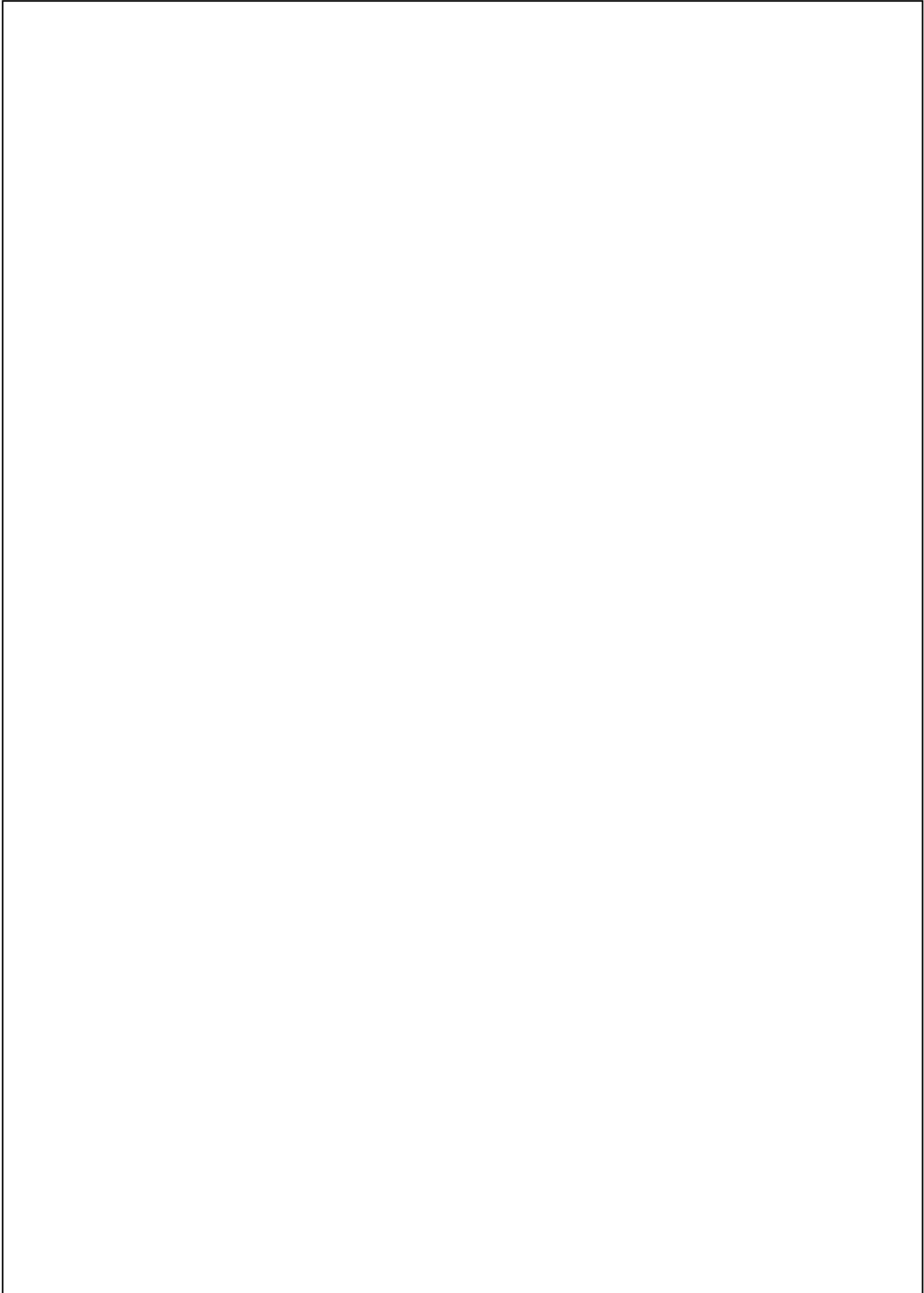


## Ordering Information

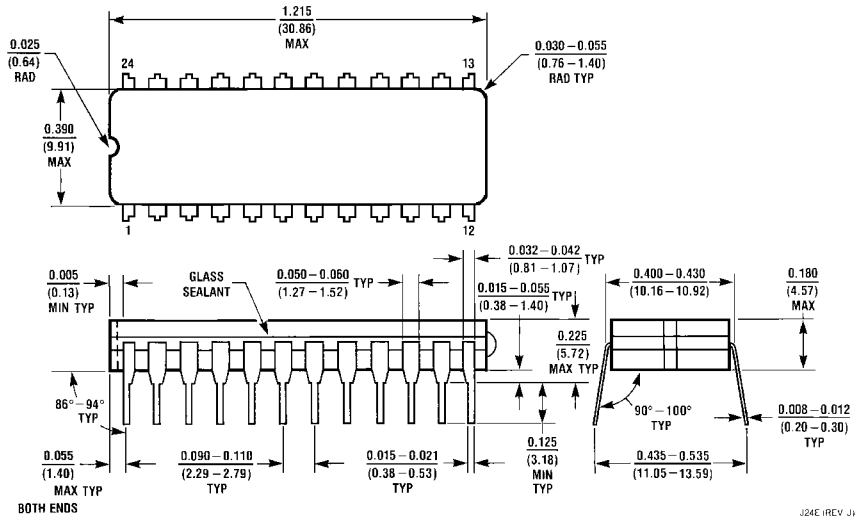
The device number is used to form part of a simplified purchasing code where a package type and temperature range are defined as follows:



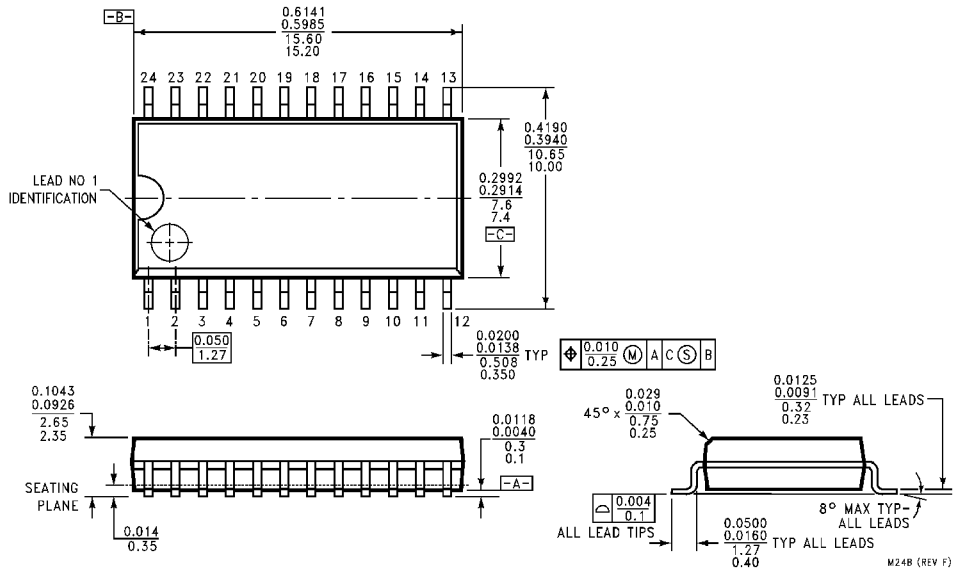
DS009885-12



**Physical Dimensions** inches (millimeters) unless otherwise noted

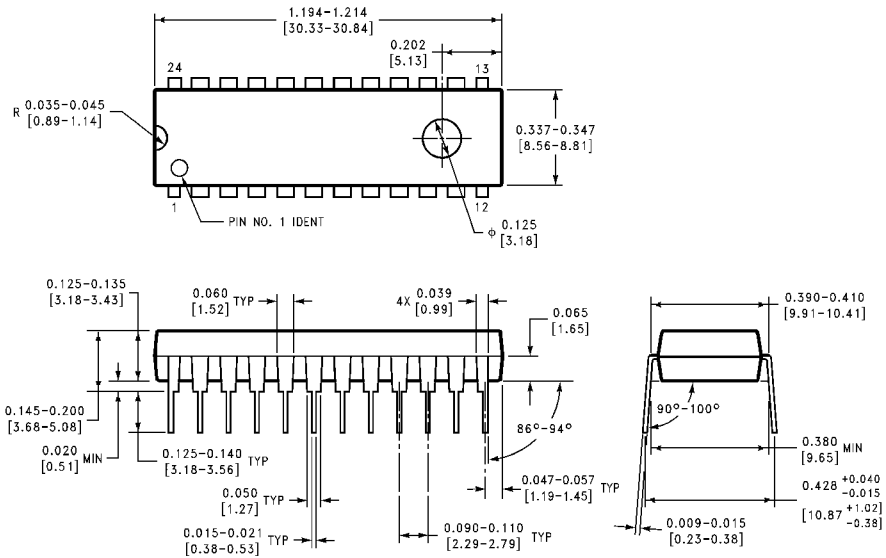


**24-Lead Ceramic Dual-In-Line Package (0.400" Wide) (D)  
Package Number J24E**



**24-Lead Molded Package (0.300" Wide) (S)  
Package Number M24B**

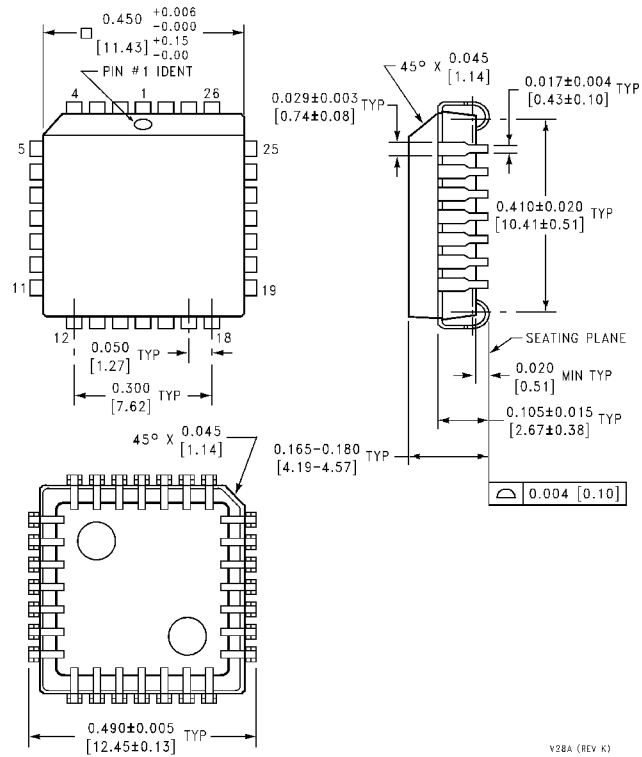
**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**24-Lead Plastic Dual-In-Line Package (P)**  
**Package Number N24E**

N24E (REV A)

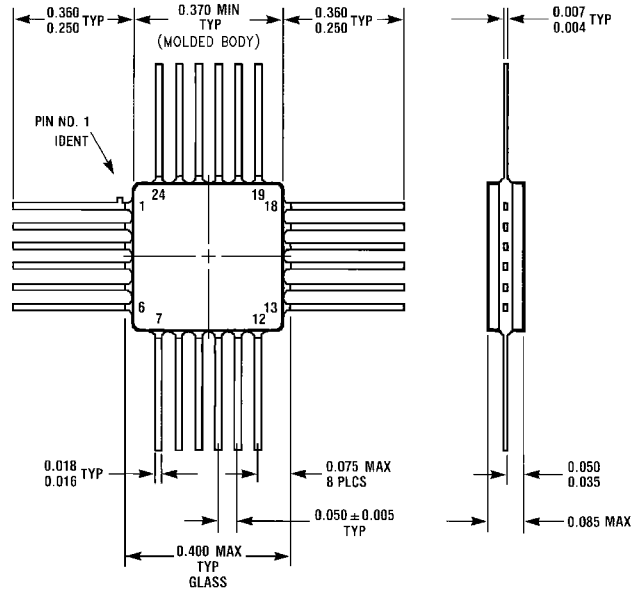
**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**28-Lead Plastic Chip Carrier (Q)  
Package Number V28A**

V28A (REV K)

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



W24B (REV D)

**24-Lead Quad Cerpak (F)  
Package Number W24B**

**LIFE SUPPORT POLICY**

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

Fairchild Semiconductor Corporation  
Americas  
Customer Response Center  
Tel: 1-888-522-5372

Fairchild Semiconductor Europe  
Fax: +49 (0) 1 80-530 85 86  
Email: europe.support@nsc.com  
Deutsch Tel: +49 (0) 8 141-35-0  
English Tel: +44 (0) 1 793-85-68-56  
Italy Tel: +39 (0) 2 57 5631

Fairchild Semiconductor Hong Kong Ltd.  
13th Floor, Straight Block,  
Ocean Centre, 5 Canton Rd.  
Tsimshatsui, Kowloon  
Hong Kong  
Tel: +852 2737-7200  
Fax: +852 2314-0061

National Semiconductor Japan Ltd.  
Tel: 81-3-5620-6175  
Fax: 81-3-5620-6179

www.fairchildsemi.com