M2148H
HIGH SPEED 1024 x 4 BIT STATIC RAM

Military

	M2148H-3	M2148H
Max. Access Time (ns)	55	70
Max. Active Current (mA)	180	180
Max. Standby Current (mA)	30	30

- **HMOS III Technology**
- **Completely Static Memory — No Clock or Timing Strobe Required**
- **Equal Access and Cycle Times**
- **Single +5V Supply**
- **Power-Down**
- **High Density 18-Pin Package**
- **Industry Standard M2114A Pinout**
- **Common Data Input and Output**
- **Three-State Output**
- **Full Military Temperature Range −55°C to +125°C (T_C)**

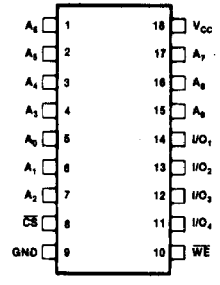
The Intel M2148H is a 4096-bit static Random Access Memory organized as 1024 words by 4 bits using HMOS III, a high-performance MOS technology. It uses a uniquely innovative design approach which provides the ease-of-use features associated with non-clocked static memories and the reduced standby power dissipation associated with clocked static memories. To the user this means low standby power dissipation without the need for clocks, address setup and hold times, nor reduced data rates due to cycle times that are longer than access times.

Intel's HMOS III process provides superior radiation tolerance for applications with stringent radiation requirements. Contact your local sales office for the latest information.

$\overline{CS}$ controls the power-down feature. In less than a cycle time after $\overline{CS}$ goes high—disabling the M2148H—the part automatically reduces its power requirements and remains in this low power standby mode as long as $\overline{CS}$ remains high. This device feature results in system power savings as great as 85% in larger systems, where the majority of devices are disabled.

The M2148H is placed in an 18-pin package configured with the industry standard 1K x 4 pinout. It is directly TTL compatible in all respects: inputs, outputs, and single +5V supply. The data is read out nondestructively and has the same polarity as the input data.

Pin Configuration



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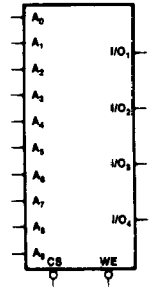
Logic Symbol



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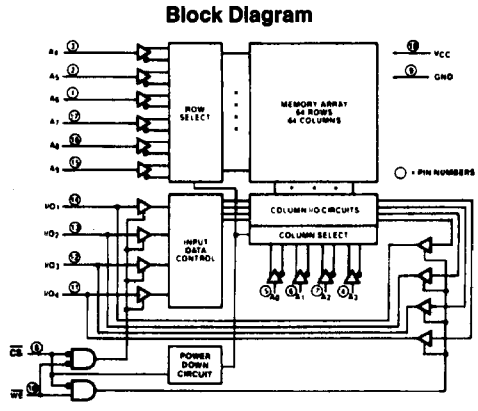
Block Diagram



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Pin Names

A_0–A_9	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
I/O_1–I/O_4	Data Input/Output
V_{CC}	Power (+5V)
GND	Ground

Truth Table

$\overline{CS}$	$\overline{WE}$	Mode	I/O	Power
H	X	Not Selected	HIGH-Z	Standby
L	L	Write	D_{IN}	Active
L	H	Read	D_{OUT}	Active

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November 1989
Order Number: 270031-003

ABSOLUTE MAXIMUM RATINGS*

Case Temperature Under Bias . . . −65°C to +135°C
Storage Temperature . . . . . −65°C to +150°C
Voltage on Any Pin
With Respect to Ground . . . . . −3.5V to +7V
Power Dissipation 1.2W
D.C. Output Current . . . . . 20 mA

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

Operating Conditions

Symbol	Description	Min	Max	Units
T_C	Case Temperature (Instant On)	−55	+125	°C
V_{CC}	Digital Supply Voltage	4.50	5.50	V

D.C. AND OPERATING CHARACTERISTICS (Over Specified Operating Conditions)

Symbol	Parameter	M2148H/H-3			Unit	Comments
		Min	Typ(1)	Max		
I_{LI}	Input Load Current (All Input Pins)		0.01	1.0	μA	V_{CC} = Max., V_{IN} = GND to V_{CC}
$\|I_{LO}\|$	Output Leakage Current		0.1	10	μA	$\overline{CS}$ = V_H, V_{CC} = Max., V_{OUT} = GND to 4.5V
I_{CC}	Operating Current		120	180	mA	T_C = −55°C | V_{CC} = Max., $\overline{CS}$ = V_{IL}, Outputs Open
I_{SB}	Standby Current		15	30	mA	V_{CC} = Min. to Max., $\overline{CS}$ = V_{IH}
I_{PO}(2)	Peak Power-On Current		25	50	mA	V_{CC} = GND to V_{CC} Min. $\overline{CS}$ = Lower of V_{CC} or V_{IH} Min.
V_{IL}	Input Low Voltage	−3.0		0.8	V	
V_{IH}	Input High Voltage	2.0		6.0	V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 8 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = −4.0 mA
I_{OS}(3)	Output Short Circuit Current	−200	+200		mA	V_{OUT} = GND to V_{CC}

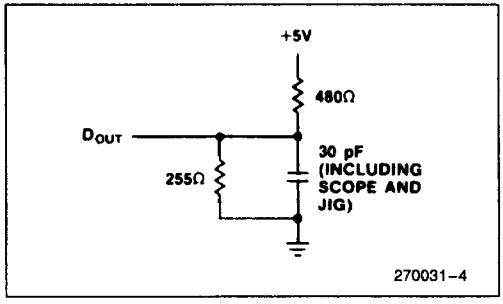
NOTES:
1. Typical limits are at V_{CC} = 5V, T_C = +25°C, and Load A.
2. A pull-up resistor to V_{CC} on the $\overline{CS}$ input is required to keep the device deselected; otherwise, power-on current approaches I_{CC} active.
3. Duration not to exceed one second. No more than one output shorted at a time.

CAPACITANCE T_C = 25°C, f = 1.0 MHz

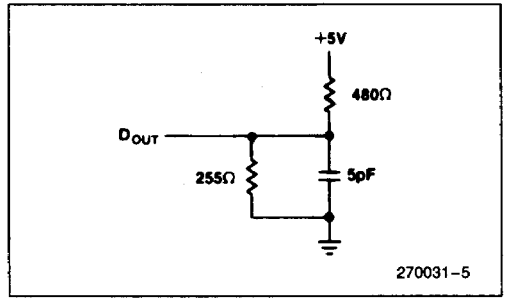
Symbol	Parameter	Max	Unit	Conditions
C_{IN}	Input Capacitance	5	pF	V_{IN} = 0V
$C_{I/O}$	Input/Output Capacitance	7	pF	$V_{I/O}$ = 0V

A.C. TEST CONDITIONS

Input Pulse Levels ..... GND to 3.0V
Input Rise and Fall Times ..... 5 ns
Input Timing Reference Levels 1.5V
Output Timing Reference Levels ..... 0.8V & 2.0V
Output Load ..... See Load A



Load A



Load B

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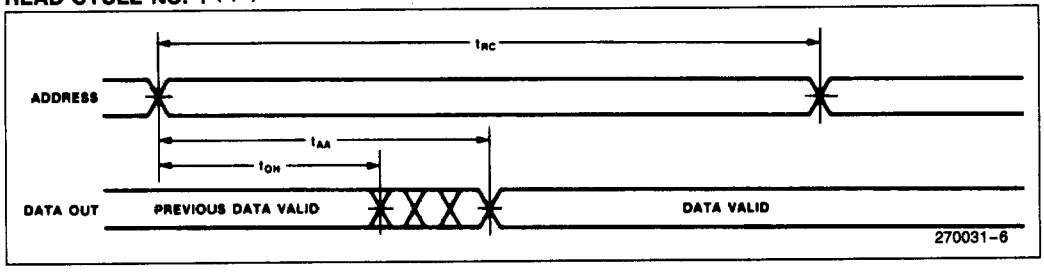
A.C. CHARACTERISTICS (Over Specified Operating Conditions)

READ CYCLE

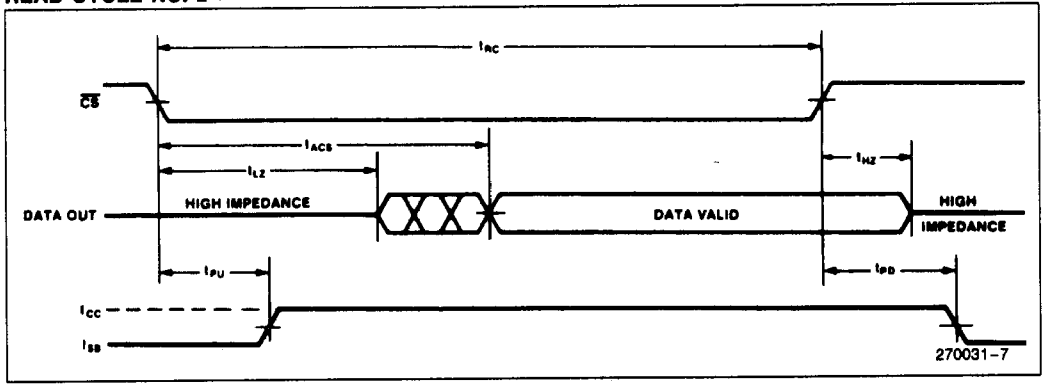
Symbol	Parameter	M2148H		M2148H-3		Unit	Comments
		Min	Max	Min	Max		
t_{RC}	Read Cycle Time	70		55		ns	
t_{AA}	Address Access Time		70		55	ns	
t_{ACS}	Chip Select Access Time		70		55	ns	
t_{OH}	Output Hold from Address Change	5		5		ns	
t_{LZ}	Chip Selection Output in Low Z	10		10		ns	(Note 4)
t_{HZ}	Chip Deselection to Output in High Z	0	20	0	20	ns	(Note 4)
t_{PU}	Chip Selection to Power Up Time	0		0		ns	
t_{PD}	Chip Deselection to Power Down Time		30		30	ns	

WAVEFORMS

READ CYCLE NO. 1 (1, 2)



READ CYCLE NO. 2 (1, 3)



NOTES:
1. $\overline{WE}$ is high for Read Cycles.
2. Device is continuously selected $\overline{CS}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. Transition is measured ±500 mV from high impedance voltage with Load B.
5. Case temperatures are "instant on".

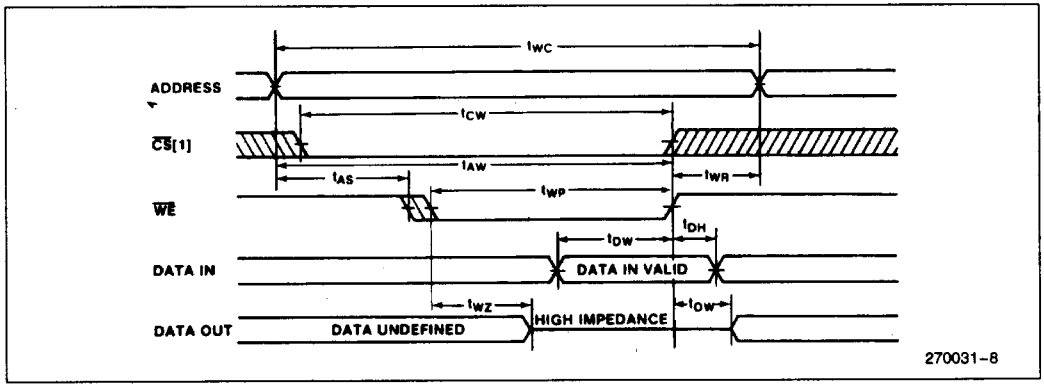
A.C. CHARACTERISTICS (Over Specified Operating Conditions) (Continued)

WRITE CYCLE

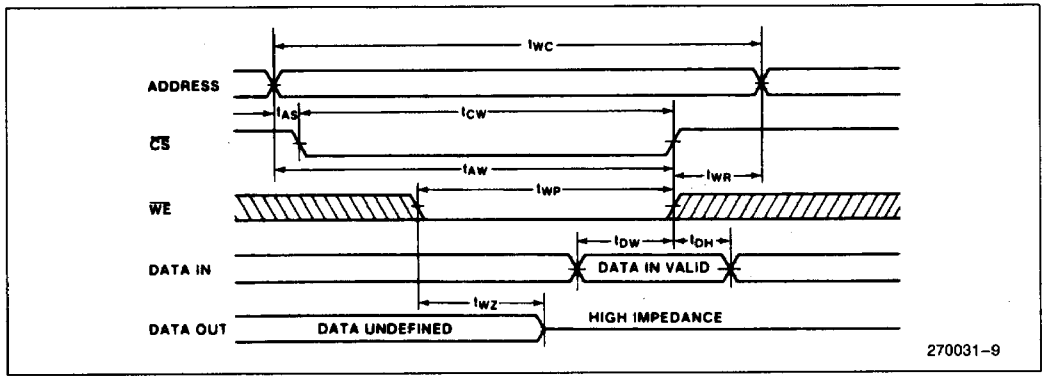
Symbol	Parameter	M2148H		M2148H-3		Unit	Comments
		Min	Max	Min	Max		
t_{WC}	Write Cycle Time	70		55		ns	
t_{CW}	Chip Selection to End of Write	65		50		ns	
t_{AW}	Address Valid to End of Write	65		50		ns	
t_{AS}	Address Setup Time	0		0		ns	
t_{WP}	Write Pulse Width	50		40		ns	
t_{WR}	Write Recovery Time	5		5		ns	
t_{DW}	Data Valid to End to Write	25		20		ns	
t_{DH}	Data Hold Time	0		0		ns	
t_{WZ}	Write Enabled to Output in High Z	0	25	0	20	ns	(Note 2)
t_{OW}	Output Active from End of Write	0		0		ns	(Note 2)

WAVEFORMS

WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)



WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED)



NOTES:
1. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.
2. Transition is measured ±500 mV from high impedance voltage with Load B.

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