Power Field Effect Transistors

P-Channel Enhancement-Mode Silicon Gate TMOS

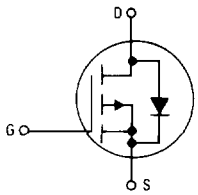
IRF9640

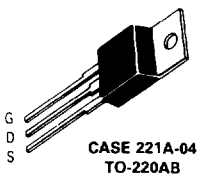
This TMOS Power FET is designed for high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds
- Low $r_{DS(on)}$ to Minimize On-Losses. Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

TMOS™

TMOS POWER FET
11 AMPERES
$r_{DS(on)}$ = 0.5 OHM
200 VOLTS
$r_{DS(on)}$ = 0.035 OHM





CASE 221A-04
TO-220AB

3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	200	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	200	Vdc
Gate-Source Voltage	V_{GS}	± 20	Vdc
Drain Current — *Continuous* @ T_C = 25°C — Continuous @ T_C = 100°C — Pulsed @ T_C = 25°C	I_D I_{DM}	11 7 44	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	125 1	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$	1 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from Case for 5 Seconds	T_L	300	°C

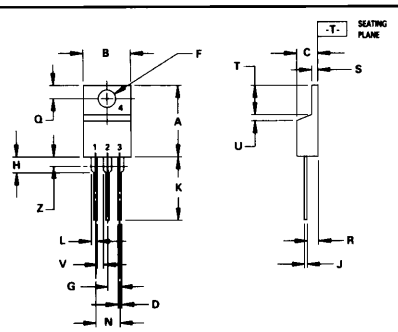
See the MTP12P20 Data Sheet for a complete set of design curves

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)	$V_{(BR)DSS}$	200	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)	I_{DSS}	 — —	 250 1000	μAdc
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)	I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)	I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*				
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 0.25 mA)	$V_{GS(th)}$	2	4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 6 Adc)	$r_{DS(on)}$	—	0.5	Ohm
On-State Drain Current (V_{GS} = 10 V, V_{DS} ≥ 25 Vdc)	$I_{D(on)}$	11	—	Adc
Forward Transconductance (V_{DS} ≥ 5.5 V, I_D = 6 A)	g_{FS}	4	—	mhos
DYNAMIC CHARACTERISTICS				
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz)	C_{iss}	—	1300	pF
Output Capacitance		C_{oss}	—	450	
Reverse Transfer Capacitance		C_{rss}	—	250	
SWITCHING CHARACTERISTICS*					
Turn-On Delay Time	(V_{DD} ≈ 100 V, I_D = 6 Apk, R_{gen} = 4.7 Ohms)	$t_{d(on)}$	—	30	ns
Rise Time		t_r	—	15	
Turn-Off Delay Time		$t_{d(off)}$	—	18	
Fall Time		t_f	—	12	
Total Gate Charge	(V_{DS} = 160 V, V_{GS} = 15 Vdc, I_D = 22 A)	Q_g	70 (Typ)	90	nC
Gate-Source Charge		Q_{gs}	55 (Typ)	—	
Gate-Drain Charge		Q_{gd}	15 (Typ)	—	
SOURCE-DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = 11 A, V_{GS} = 0)	V_{SD}	2.7 (Typ)	4.6	Vdc
Forward Turn-On Time	(I_S = 11 A, V_{GS} = 0 dI_S/dt = 100 A/μs, V_R = 50 V)	t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	270 (Typ)	—	ns

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

OUTLINE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

CASE 221A-04
TO-220AB

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080