CY28RS400

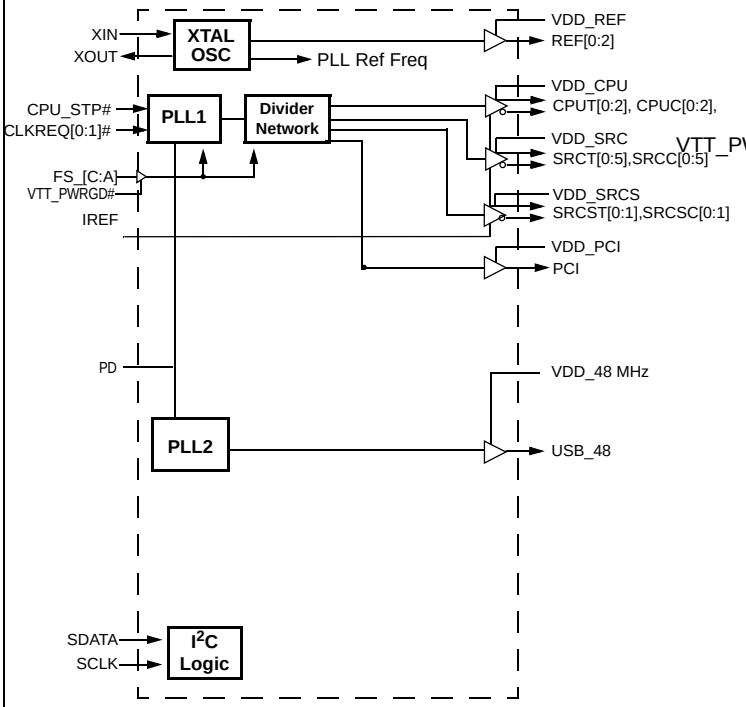
Clock Generator for ATI® RS400 Chipset

Features

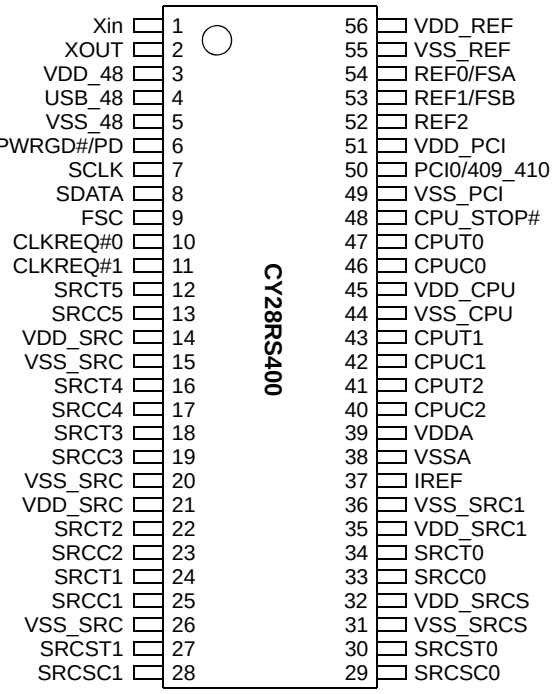
- Supports Intel® CPU
- Selectable CPU frequencies
- Differential CPU clock pairs
- 100 MHz differential SRC clocks
- 48 MHz USB clock
- 33 MHz PCI clock
- Low-voltage frequency select input
- I²C support with readback capabilities
- Ideal Lexmark Spread Spectrum profile for maximum electromagnetic interference (EMI) reduction
- 3.3V power supply
- 56-pin SSOP and TSSOP packages

CPU	SRC	PCI	REF	USB_48
x3	x8	x1	x 3	x 1

Block Diagram



Pin Configuration



56 SSOP/TSSOP

2200 Laurelwood Road, Santa Clara, CA 95054 Tel:(408) 855-0555 Fax:(408) 855-0550 www.SpectraLinear.com

Pin Description

Pin No.	Name	Type	Description
47,46,43,42, 41,40	CPUT/C[2:0]	O, DIF	Differential CPU clock output. Intel Type-X buffer.
50	PCI0/409_410	I/O, PD	33 MHz clock output/CPU Frequency table Select Intel Type-5 buffer. 0 = 410 frequency select table 1 = 409 frequency select table. This has an internal pull-down
37	IREF	I	A precision resistor attached to this pin is connected to the internal current reference.
54	REF0/ FSA	I/O, SE,	14.318 MHz REF clock ouput/ CPU Frequency Select. Intel® Type-5 buffer.
53	REF1/FSB	I/O, SE	14.318 MHz REF clock ouput/ CPU Frequency Select. Intel Type-5 buffer.
52	REF2	O, SE	14.318 MHz REF clock ouput. Intel Type-5 buffer.
7	SCLK	I,PU	SMBus-compatible SCLOCK.This pin has an internal pullup, but is tri-stated in power-down.
8	SDATA	I/O, PU	SMBus compatible SDATA.This pin has an internal pullup, but is tri-stated in power-down.
27, 28, 30, 29	SRCST/C[1:0]	O, DIF	Differential Selectable Serial reference clock. Intel Type-X buffer. Includes overclock support through SMBUS
12, 13, 16, 17, 18, 19, 22, 23, 24, 25 ,34,33	SRCT/C[5:0]	O, DIF	100 MHz Differential Serial reference clock. Intel Type-X buffer.
10,11	CLKREQ#[0:1]	I, SE, PD	Output Enable control for SRCT/C. Output enable control required by Minicard specification. These pins have an internal pull-down. 0 = Selected SRC outputs are enabled, 1 = Selected SRC outputs are disabled
4	USB_48	O, SE	48 MHz clock output. Intel Type-3A buffer.
6	VTT_PWRGD#/PD	I PD	3.3V LVTTL input. This pin is a level sensitive strobe used to latch the FS_A, FS_B, FS_C and 409_410 inputs. After asserting VTT_PWRGD# (active low), this pin becomes a realtime input for asserting power down (active high)
48	CPU_STP#	I, PU	3.3V LVTTL input. This pin is used to gate the CPU outputs. CPU outputs are turned off two cycles after assertion of this pin
9	FSC	I	3.3V LVTTL input. CPU Clock Frequency Select
3	VDD_48	PWR	3.3V power supply for USB outputs
45	VDD_CPU	PWR	3.3V power supply for CPU outputs
51	VDD_PCI	PWR	3.3V power supply for PCI outputs
56	VDD_REF	PWR	3.3V power supply for REF outputs
14, 21	VDD_SRC	PWR	3.3V power supply for SRC outputs
35	VDD_SRC1	PWR	3.3V power supply for SRC outputs
32	VDD_SRCS	PWR	3.3V power supply for SRCS outputs
39	VDDA	PWR	3.3V Analog Power for PLLs
5	VSS_48	GND	Ground for USB outputs
44	VSS_CPU	GND	Ground for CPU outputs
49	VSS_PCI	GND	Ground for PCI outputs
55	VSS_REF	GND	Ground for REF outputs
15, 20, 26	VSS_SRC	GND	Ground for SRC outputs
36	VSS_SRC1	GND	Ground for SRC outputs
31	VSS_SRCS	GND	Ground for SRCS outputs
38	VSSA	GND	Analog Ground
1	XIN	I	14.318 MHz Crystal Input
2	XOUT	O	14.318 MHz Crystal Output

Frequency Select Pins (FS_A, FS_B, FS_C and 409_410)

Host clock frequency selection is achieved by applying the appropriate logic levels to FS_A, FS_B, FS_C and 409_410 inputs prior to VTT_PWRGD# assertion (as seen by the clock synthesizer). Upon VTT_PWRGD# being sampled low by the clock chip (indicating processor VTT voltage is stable), the clock chip samples the FS_A, FS_B, FS_C and 409_410 input values. For all logic levels of FS_A, FS_B, FS_C and 409_410 VTT_PWRGD# employs a one-shot functionality in that once a valid low on VTT_PWRGD# has been sampled, all further VTT_PWRGD#, FS_A, FS_B, FS_C and 409-410 transitions will be ignored. There are 2 CPU frequency select tables. One based on the CK409 specifications and one based on the CK410 specifications. The table to be used is determined by the value latched on the PCI0/409_410 pin by the VTT_PWRGD/PD# pin. A '0' on this pin selects the 410 frequency table and a '1' on this pin selects the 409 frequency table. In the 409 table, only the FS_A and FS_B pins influence the frequency selection.

Table 1. Frequency Select Table (FS_A FS_B FS_C) 410 mode, 409_410 = 0

FS_C	FS_B	FS_A	CPU	SRC	PCIF/PCI	REF0	USB
1	0	1	100 MHz	100 MHz	33 MHz	14.318 MHz	48 MHz
0	0	1	133 MHz	100 MHz	33 MHz	14.318 MHz	48 MHz
0	1	0	200 MHz	100 MHz	33 MHz	14.318 MHz	48 MHz
0	0	0	266 MHz	100 MHz	33 MHz	14.318 MHz	48 MHz
1	1	1	Reserved	100 MHz	33 MHz	14.318 MHz	48 MHz

Table 2. Frequency Select Table (FS_A FS_B) 410 mode, 409_410 = 1

FS_B	FS_A	CPU	SRC	PCIF/PCI	REF0	USB
0	0	100 MHz	100 MHz	33 MHz	14.318 MHz	48 MHz
0	1	133 MHz	100 MHz	33 MHz	14.318 MHz	48 MHz
1	0	200 MHz	100 MHz	33 MHz	14.318 MHz	48 MHz

Serial Data Interface

To enhance the flexibility and function of the clock synthesizer, a two-signal serial interface is provided. Through the Serial Data Interface, various device functions, such as individual clock output buffers, can be individually enabled or disabled. The registers associated with the Serial Data Interface initializes to their default setting upon power-up, and therefore use of this interface is optional. Clock device register changes are normally made upon system initialization, if any are required. The interface cannot be used during system operation for power management functions.

Data Protocol

The clock driver serial protocol accepts byte write, byte read, block write, and block read operations from the controller. For block write/read operation, the bytes must be accessed in sequential order from lowest to highest byte (most significant bit first) with the ability to stop after any complete byte has been transferred. For byte write and byte read operations, the system controller can access individually indexed bytes. The offset of the indexed byte is encoded in the command code, as described in *Table 3*.

The block write and block read protocol is outlined in *Table 4* while *Table 5* outlines the corresponding byte write and byte read protocol. The slave receiver address is 11010010 (D2h).

Table 3. Command Code Definition

Bit	Description
7	0 = Block read or block write operation, 1 = Byte read or byte write operation
(6:5)	Chip select address, set to ‘00’ to access device
(4:0)	Byte offset for byte read or byte write operation. For block read or block write operations, these bits should be '00000'

Table 4. Block Read and Block Write Protocol

Block Write Protocol		Block Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
8:2	Slave address – 7 bits	8:2	Slave address – 7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
18:11	Command Code – 8 bits	18:11	Command Code – 8 bits
19	Acknowledge from slave	19	Acknowledge from slave

Table 4. Block Read and Block Write Protocol (continued)

Block Write Protocol		Block Read Protocol	
Bit	**Description**	**Bit**	**Description**
27:20	Byte Count – 8 bits	20	Repeat start
28	Acknowledge from slave	27:21	Slave address – 7 bits
36:29	Data byte 1 – 8 bits	28	Read = 1
37	Acknowledge from slave	29	Acknowledge from slave
45:38	Data byte 2 – 8 bits	37:30	Byte Count from slave – 8 bits
46	Acknowledge from slave	38	Acknowledge
....	Data Byte /Slave Acknowledges	46:39	Data byte 1 from slave – 8 bits
....	Data Byte N –8 bits	47	Acknowledge
....	Acknowledge from slave	55:48	Data byte 2 from slave – 8 bits
....	Stop	56	Acknowledge
		....	Data bytes from slave / Acknowledge
		....	Data Byte N from slave – 8 bits
		....	NOT Acknowledge

Table 5. Byte Read and Byte Write Protocol

Byte Write Protocol		Byte Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
8:2	Slave address – 7 bits	8:2	Slave address – 7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
18:11	Command Code – 8 bits	18:11	Command Code – 8 bits
19	Acknowledge from slave	19	Acknowledge from slave
27:20	Data byte – 8 bits	20	Repeated start
28	Acknowledge from slave	27:21	Slave address – 7 bits
29	Stop	28	Read
		29	Acknowledge from slave
		37:30	Data from slave – 8 bits
		38	NOT Acknowledge
		39	Stop

Control Registers

Byte 0:Control Register 0

Bit	@Pup	Name	Description
7	1	SRC[T/C]5	SRC[T/C]5 Output Enable 0 = Disable (Hi-Z), 1 = Enable
6	1	SRC[T/C]4	SRC[T/C]4 Output Enable 0 = Disable (Hi-Z), 1 = Enable
5	1	SRC[T/C]3	SRC[T/C]3 Output Enable 0 = Disable (Hi-Z), 1 = Enable
4	1	SRC[T/C]2	SRC[T/C]2 Output Enable 0 = Disable (Hi-Z), 1 = Enable
3	1	SRC[T/C]1	SRC[T/C]1 Output Enable 0 = Disable (Hi-Z), 1 = Enable
2	1	SRC [T/C]0	SRC[T/C]0 Output Enable 0 = Disable (Hi-Z), 1 = Enable
1	1	SRCS[T/C]1	SRCS[T/C]1 Output Enable 0 = Disable (Hi-Z), 1 = Enable
0	1	SRCS[T/C]0	SRCS[T/C]0 Output Enable 0 = Disable (Hi-Z), 1 = Enable

Byte 1: Control Register 1

Bit	@Pup	Name	Description
7	1	REF2	REF2 Output Enable 0 = Disable, 1 = Enable
6	1	REF1	REF1 Output Enable 0 = Disable, 1 = Enable
5	1	REF0	REF0 Output Enable 0 = Disable, 1 = Enable
4	1	PCI0	PCI0 Output Enable 0 = Disable, 1 = Enable
3	1	USB_48	USB_48MHz Output Enable 0 = Disable, 1 = Enable
2	1	CPU[T/C]2	CPU[T/C]2 Output Enable 0 = Disable (Hi-Z), 1 = Enable
1	1	CPU[T/C]1	CPU[T/C]1 Output Enable 0 = Disable (Hi-Z), 1 = Enable
0	1	CPU[T/C]0	CPU[T/C]0 Output Enable 0 = Disable (Hi-Z), 1 = Enable

Byte 2: Control Register 2

Bit	@Pup	Name	Description
7	1	CPUT/C SRCT/C	Spread Spectrum Selection '0' = -0.35% '1' = -0.50%
6	1	USB_48	48MHz Output Drive Strength 0 = 1x, 1 = 2x
5	1	PCI	33MHz Output Drive Strength 0 = 1x, 1 = 2x
4	0	Reserved	Reserved
3	1	Reserved	Reserved
2	0	CPU SRC	CPU/SRC Spread Spectrum Enable 0 = Spread off, 1 = Spread on
1	1	Reserved	Reserved

Byte 2: Control Register 2 (continued)

Bit	@Pup	Name	Description
0	1	Reserved	Reserved

Byte 3: Control Register 3

Bit	@Pup	Name	Description
7	1	CLKREQ#	CLKREQ# drive mode 0 = SRC clocks driven when stopped, 1 = SRC clocks tri-state when stopped
6	0	CPU	CPU pd drive mode 0 = CPU clocks driven when power down, 1 = CPU clocks tri-state
5	1	SRC	SRC pd drive mode 0 = SRC clocks driven when power down, 1 = SRC clocks tri-state
4	0	CPU	CPU_STOP# drive mode 0 = CPU clocks driven , 1 = CPU clocks tri-state
3	1	CPU2	Allow control of CPU2 with CPU_STOP# 0 = CPU2 is free running, 1 = CPU2 is stopped with CPU_STOP#
2	1	CPU1	Allow control of CPU1 with CPU_STOP# 0 = CPU1 is free running, 1 = CPU1 is stopped with CPU_STOP#
1	1	CPU0	Allow control of CPU0 with CPU_STOP# 0 = CPU0 is free running, 1 = CPU0 is stopped with CPU_STOP#
0	1	Reserved	Reserved

Byte 4: Control Register 4

Bit	@Pup	Name	Description
7	0	SRC[T/C]5	SRC[T/C]5 CLKREQ0 control 1 = SRC[T/C]5 stoppable by CLKREQ#0 pin 0 = SRC[T/C]5 free running
6	0	SRC[T/C]4	SRC[T/C]4 CLKREQ#0 control 1 = SRC[T/C]4 stoppable by CLKREQ#0 pin 0 = SRC[T/C]4 free running
5	0	SRC[T/C]3	SRC[T/C]3 CLKREQ#0 control 1 = SRC[T/C]3 stoppable by CLKREQ#0 pin 0 = SRC[T/C]3 free running
4	0	SRC[T/C]2	SRC[T/C]2 CLKREQ#0 control 1 = SRC[T/C]2 stoppable by CLKREQ#0 pin 0 = SRC[T/C]2 free running
3	0	SRC[T/C]1	SRC[T/C]1 CLKREQ#0 control 1 = SRC[T/C]1 stoppable by CLKREQ#0 pin 0 = SRC[T/C]1 free running
2	0	SRC[T/C]0	SRC[T/C]0 CLKREQ#0 control 1 = SRC[T/C]1 stoppable by CLKREQ#0 pin 0 = SRC[T/C]1 free running
1	1	Reserved	Reserved
0	1	Reserved	Reserved

Byte 5: Control Register 5

Bit	@Pup	Name	Description
7	0	SRC[T/C]5	SRC[T/C]5 CLKREQ#1 control 1 = SRC[T/C]5 stoppable by CLKREQ#1 pin 0 = SRC[T/C]5 free running
6	0	SRC[T/C]4	SRC[T/C]4 CLKREQ#1 control 1 = SRC[T/C]4 stoppable by CLKREQ#1 pin 0 = SRC[T/C]4 free running

Byte 5: Control Register 5 (continued)

Bit	@Pup	Name	Description
5	0	SRC[T/C]3	SRC[T/C]3 CLKREQ#1 control 1 = SRC[T/C]3 stoppable by CLKREQ#1 pin 0 = SRC[T/C]3 free running
4	0	SRC[T/C]2	SRC[T/C]2 CLKREQ#1 control 1 = SRC[T/C]2 stoppable by CLKREQ#1 pin 0 = SRC[T/C]2 free running
3	0	SRC[T/C]1	SRC[T/C]1 CLKREQ#1 control 1 = SRC[T/C]1 stoppable by CLKREQ#1 pin 0 = SRC[T/C]1 free running
2	0	SRC[T/C]0	SRC[T/C]0 CLKREQ#1 control 1 = SRC[T/C]1 stoppable by CLKREQ#1 pin 0 = SRC[T/C]1 free running
1	0	Reserved	Reserved
0	0	Reserved	Reserved

Byte 6: Control Register 6

Bit	@Pup	Name	Description
7	0	TEST_SEL	REF/N or Tri-state Select 1 = REF/N Clock, 0 = Tri-state
6	0	TEST_MODE	Test Clock Mode Entry Control 1 = REF/N or Tri-state mode, 0 = Normal operation
5	0	REF	REF output drive strength. 0 = Low drive, 1 = High drive.
4	0	Reserved	Reserved
3	HW	409_410	409_410 reflects the value of the 409_410 pin sampled on power up. 0 = 409_410 was low during VTT_PWRGD# assertion
2	HW	FS_C	FS_C Reflects the value of the FS_C pin sampled on power up. 0 = FS_C was low during VTT_PWRGD# assertion.
1	HW	FS_B	FS_B Reflects the value of the FS_B pin sampled on power up. 0 = FS_B was low during VTT_PWRGD# assertion.
0	HW	FS_A	FS_A Reflects the value of the FS_A pin sampled on power up. 0 = FS_A was low during VTT_PWRGD# assertion.

Byte 7: Vendor ID

Bit	@Pup	Name	Description
7	0		Revision Code Bit 3
6	0		Revision Code Bit 2
5	0		Revision Code Bit 1
4	1		Revision Code Bit 0
3	1		Vendor ID Bit 3
2	0		Vendor ID Bit 2
1	0		Vendor ID Bit 1
0	0		Vendor ID Bit 0

Crystal Recommendations

The CY28RS400 requires a Parallel Resonance Crystal. Substituting a series resonance crystal will cause the CY28RS400 to operate at the wrong frequency and violate the ppm specification. For most applications there is a 300-ppm frequency shift between series and parallel crystals due to incorrect loading.

Table 6. Crystal Recommendations

Frequency (Fund)	Cut	Loading	Load Cap	Drive (max.)	Shunt Cap (max.)	Motional (max.)	Tolerance (max.)	Stability (max.)	Aging (max.)
14.31818 MHz	AT	Parallel	20 pF	0.1 mW	5 pF	0.016 pF	35 ppm	30 ppm	5 ppm

Crystal Loading

Crystal loading plays a critical role in achieving low ppm performance. To realize low ppm performance, the total capacitance the crystal will see must be considered to calculate the appropriate capacitive loading (CL).

The following diagram shows a typical crystal configuration using the two trim capacitors. An important clarification for the following discussion is that the trim capacitors are in series with the crystal not parallel. It's a common misconception that load capacitors are in parallel with the crystal and should be approximately equal to the load capacitance of the crystal. This is not true.

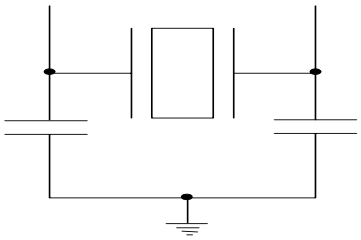


Figure 1. Crystal Capacitive Clarification

Calculating Load Capacitors

In addition to the standard external trim capacitors, trace capacitance and pin capacitance must also be considered to correctly calculate crystal loading. As mentioned previously, the capacitance on each side of the crystal is in series with the crystal. This means the total capacitance on each side of the crystal must be twice the specified crystal load capacitance (CL). While the capacitance on each side of the crystal is in series with the crystal, trim capacitors (Ce1,Ce2) should be calculated to provide equal capacitive loading on both sides.

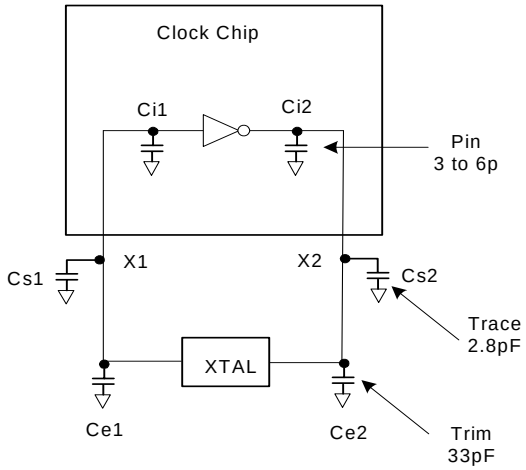


Figure 2. Crystal Loading Example

As mentioned previously, the capacitance on each side of the crystal is in series with the crystal. This mean the total capacitance on each side of the crystal must be twice the specified load capacitance (CL). While the capacitance on each side of the crystal is in series with the crystal, trim capacitors (Ce1,Ce2) should be calculated to provide equal capacitance loading on both sides.

Use the following formulas to calculate the trim capacitor values for Ce1 and Ce2.

Load Capacitance (each side)

$$Ce = 2 * CL - (Cs + Ci)$$

Total Capacitance (as seen by the crystal)

$$CLe = \frac{1}{\left(\frac{1}{Ce1 + Cs1 + Ci1} + \frac{1}{Ce2 + Cs2 + Ci2}\right)}$$

CL ..... Crystal load capacitance

CLe .....Actual loading seen by crystal using standard value trim capacitors

Ce .....External trim capacitors

Cs ..... Stray capacitance (terraced)

Ci ..... Internal capacitance (lead frame, bond wires etc.)

CL ..... Crystal load capacitance

CLe .....Actual loading seen by crystal using standard value trim capacitors

Ce .....External trim capacitors

Cs ..... Stray capacitance (terraced)

Ci ..... Internal capacitance (lead frame, bond wires etc.)

PD (Power-down) Clarification

The VTT_PWRGD# /PD pin is a dual function pin. During initial power up, the pin functions as VTT_PWRGD#. Once VTT_PWRGD# has been sampled low by the clock chip, the pin assumes PD functionality. The PD pin is an asynchronous active high input used to shut off all clocks cleanly prior to shutting off power to the device. This signal is synchronized internal to the device prior to powering down the clock synthesizer. PD is also an asynchronous input for powering up the system. When PD is asserted high, all clocks need to be driven to a low value and held prior to turning off the VCOs and the crystal oscillator.

PD (Power-down) – Assertion

When PD is sampled high by two consecutive rising edges of CPUC, all single-ended outputs will be held low on their next high to low transition and differential clocks must held high or Hi-Zd (depending on the state of the control register drive mode bit) on the next diff clock# high to low transition within four clock periods. When the SMBus PD drive mode bit corresponding to the differential (CPU, SRC, and DOT) clock output of interest is programmed to '0', the clock output are held with "Diff clock" pin driven high at 2 x Iref, and "Diff clock#" tristate. If the control register PD drive mode bit corresponding to the output of interest is programmed to "1", then both the "Diff clock" and the "Diff clock#" are three-state. Note the example below shows CPUT = 133 MHz and PD drive mode = '1' for all differential outputs. This diagram and description is applicable to valid CPU frequencies 100,133,200 and 266MHz. In the event that PD mode is desired as the initial power-on state, PD must be asserted high in less than 10 uS after asserting Vtt_PwrGd#.

PD Deassertion

The power-up latency is less than 1.8 ms. This is the time from the deassertion of the PD pin or the ramping of the power supply until the time that stable clocks are output from the clock chip. All differential outputs stopped in a three-state condition resulting from power down will be driven high in less than 300 μs of PD deassertion to a voltage greater than 200 mV. After the clock chip's internal PLL is powered up and locked, all outputs will be enabled within a few clock cycles of each other. Below is an example showing the relationship of clocks coming up.

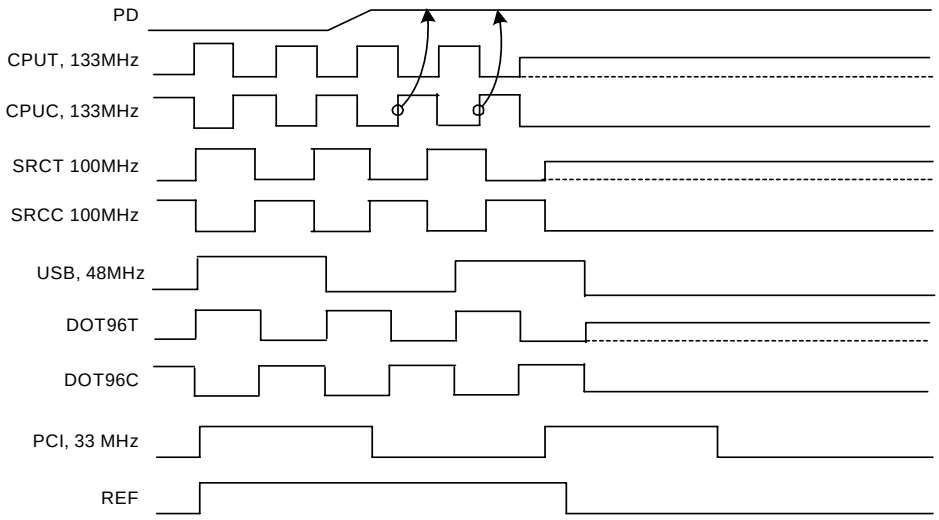


Figure 3. Power-down Assertion Timing Waveform

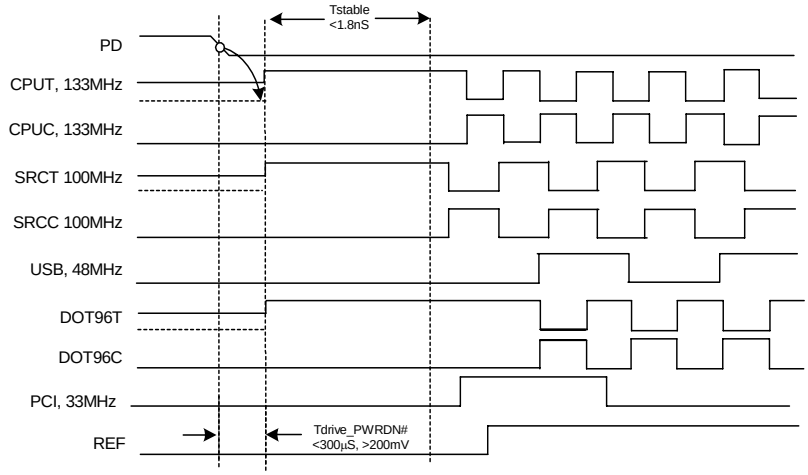


Figure 4. Power-down Deassertion Timing Waveform

CPU_STP# Assertion

The CPU_STP# signal is an active low input used for synchronous stopping and starting the CPU output clocks while the rest of the clock generator continues to function. When the CPU_STP# pin is asserted, all CPU outputs that are set with the SMBus configuration to be stoppable via assertion of CPU_STP# will be stopped within two–six CPU clock periods after being sampled by two rising edges of the internal CPUC clock. The final states of the stopped CPU signals are CPUT = HIGH and CPUC = LOW. There is no change to the output drive current values during the stopped state. The CPUT is driven HIGH with a current value equal to 6 x (Iref), and the CPUC signal will be Hi-Z. When the control register CPU_STP Hi-Z bit corresponding to the output of interest is programmed to '1', the final state of the stopped CPU clock is low (due to external 50 ohm pull-down resistor), both CPUT clock and CPUC clock outputs will not be driven.

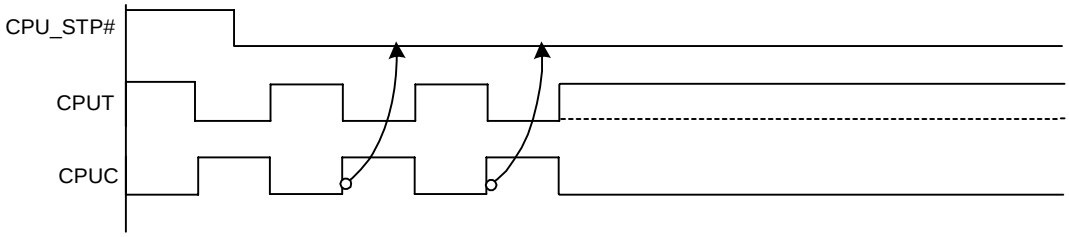


Figure 5. CPU_STP# Assertion Waveform

CPU_STP# Deassertion

The deassertion of the CPU_STP# signal will cause all CPU outputs that were stopped to resume normal operation in a synchronous manner. Synchronous manner meaning that no short or stretched clock pulses will be produce when the clock resumes. The maximum latency from the deassertion to active outputs is 2 - 6 CPU clock cycles.

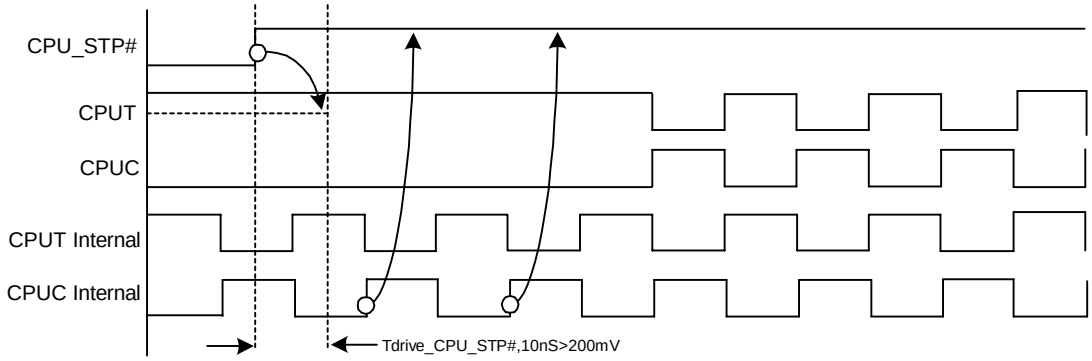


Figure 6. CPU_STP# Deassertion Waveform

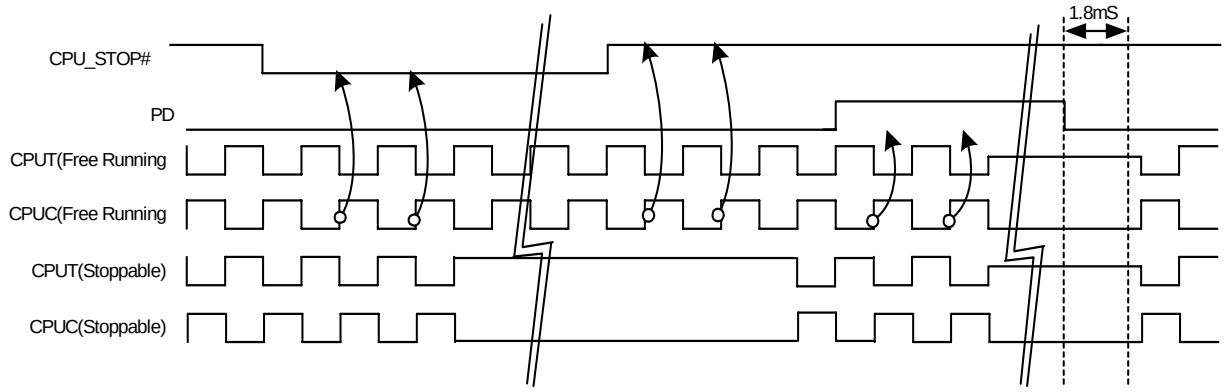


Figure 7. CPU_STP#= Driven, CPU_PD = Driven

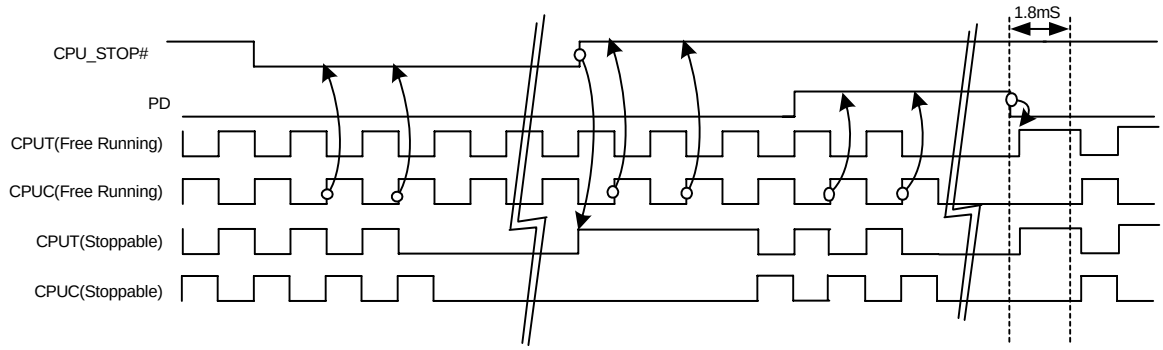


Figure 8. CPU_STP# = Hi-Z, CPU_PD = Hi-Z

CLK_REQ[0:1]# Description

The CLKREQ#[1:0] signals are active low input used for clean stopping and starting selected SRC outputs. The outputs controlled by CLKREQ#[1:0] are determined by the settings in register bytes 4 and 5. The CLKREQ# signal is a de-bounced signal in that it's state must remain unchanged during two consecutive rising edges of DIFC to be recognized as a valid assertion or de-assertion. (The assertion and de-assertion of this signal is absolutely asynchronous).

CLK_REQ[0:1]# De-assertion [Low to High transition]

The impact of deasserting the CLKREQ#[1:0] pins is all DIF outputs that are set in the control registers to stoppable via de-assertion of CLKREQ#[1:0] are to be stopped after their next transition. When the control register CLKREQ# drive mode bit is programmed to '0', the final state of all stopped SRC signals is SRCT clock = High and SRCC = Low. There is to be no change to the output drive current values, SRCT will be driven high with a current value equal 6 x Iref,. When the control register CLKREQ# drive mode bit is programmed to '1', the final state of all stopped DIF signals is low, both SRCT clock and SRCC clock outputs will not be driven.

CLK_REQ[0:1]# Assertion [High to Low transition]

All differential outputs that were stopped are to resume normal operation in a glitch free manner. The maximum latency from the assertion to active outputs is between two–six SRC clock periods (two clocks are shown) with all SRC outputs resuming simultaneously. If the CLKREQ# drive mode bit is programmed to '1' (three-state), the all stopped SRC outputs must be driven high within 10 ns of CLKREQ#[1:0] assertion to a voltage greater than 200 mV.

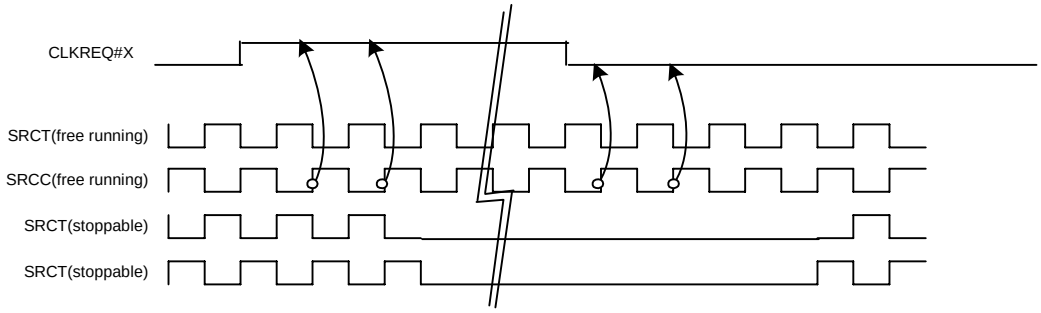


Figure 9. CLK_REQ#[0:1] Assertion/Deassertion Waveform

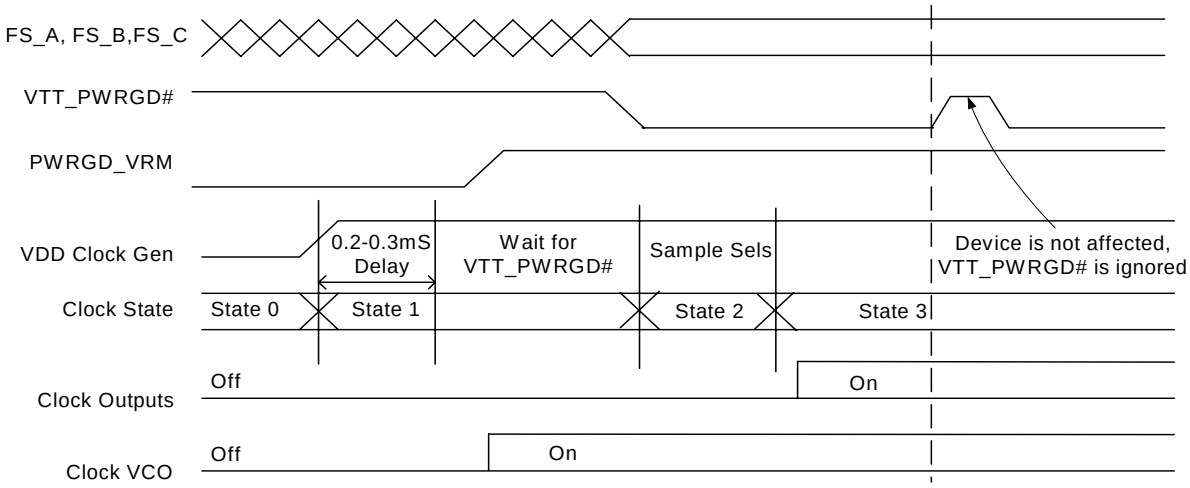


Figure 10. VTT_PWRGD# Timing Diagram

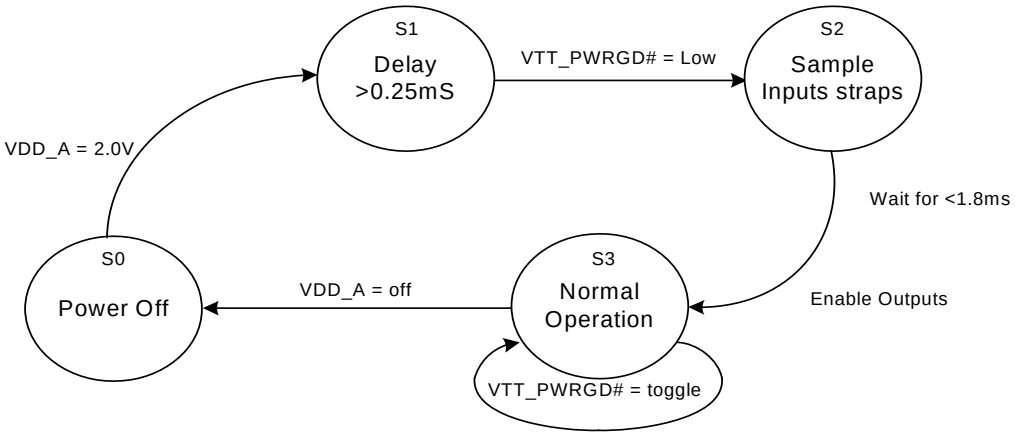


Figure 11. Clock Generator Power-up/Run State Diagram

Absolute Maximum Conditions

Parameter	Description	Condition	Min.	Max.	Unit
VDD	Core Supply Voltage		–0.5	4.6	V
VDDA	Analog Supply Voltage		–0.5	4.6	V
VIN	Input Voltage	Relative to VSS	–0.5	VDD+0.5	VDC
TS	Temperature, Storage	Non Functional	–65	+150	°C
TA	Temperature, Operating Ambient	Functional	0	70	°C
TJ	Temperature, Junction	Functional	–	150	°C
ESDHBM	ESD Protection (Human Body Model)	MIL-STD-883, Method 3015	2000	–	V
ØJC	Dissipation, Junction to Case	Mil-Spec 883E Method 1012.1	–	20	°C/W
ØJA	Dissipation, Junction to Ambient	JEDEC (JESD 51)	–	60	°C/W
UL-94	Flammability Rating	At 1/8 in.	V–0		
MSL	Moisture Sensitivity Level		1		
Multiple Supplies: The voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.					

DC Electrical Specifications

Parameter	Description	Condition	Min.	Max.	Unit
VDD_REF, VDD_CPU, VDD_PCI, VDD_SRC, VDD_48,	3.3V Operating Voltage	3.3V ± 5%	3.135	3.465	V
V_{IL_FS}	FS_A,FS_B and FS_C Input Low Voltage		V_{SS} – 0.3	0.35	V
V_{IH_FS}	FS_A,FS_B and FS_C Input Low Voltage		0.7	V_{DD} + 0.5	V
VILSMBUS	Input Low Voltage	SDATA, SCLK	–	1.0	V
VIHSMBUS	Input High Voltage	SDATA, SCLK	2.2	–	V
VIL	Input Low Voltage	VDD	V_{SS} – 0.3	0.8	V
VIH	Input High Voltage		2.0	VDD + 0.3	V
IIL	Input Leakage Current	except Pull-ups or Pull downs 0<VIN<VDD	–5	5	mA
VOL	Output Low Voltage	IOL = 1 mA	–	0.4	V
VOH	Output High Voltage	IOH = 1 mA	2.4	-	V
IOZ	High-Impedance Output Current		–10	10	uA
CIN	Input Pin Capacitance		3	5	pF
COUT	Output Pin Capacitance		3	5	pF
LIN	Pin Inductance		–	7	nH
VXIH	Xin High Voltage		0.7*VDD	VDD	V
VXIL	Xin Low Voltage		0	0.3*VDD	V
IDD	Dynamic Supply Current	At max load and frequency	–	450	mA
IPD_D	Power Down Supply Current	PD asserted, Outputs driven	–	75	mA
IPD_T	Power Down Supply Current	PD asserted, Outputs Hi-Z	–	2	mA

AC Electrical Specifications

Parameter	Description	Condition	Min.	Max.	Unit
Crystal					
T_{DC}	XIN Duty Cycle	The device will operate reliably with input duty cycles up to 30/70 but the REF clock duty cycle will not be within specification	47.5	52.5	%

AC Electrical Specifications (continued)

Parameter	Description	Condition	Min.	Max.	Unit
T_{PERIOD}	XIN Period	When XIN is driven from an external clock source	69.841	71.0	ns
T_R / T_F	XIN Rise and Fall Times	Measured between $0.3V_{DD}$ and $0.7V_{DD}$	–	10.0	ns
T_{CCJ}	XIN Cycle to Cycle Jitter	As an average over 1-μs duration	–	500	ps
L_{ACC}	Long-term Accuracy	Over 150 ms	–	300	ppm
CPU at 0.7V					
T_{DC}	CPUT and CPUC Duty Cycle	Measured at crossing point V_{OX}	45	55	%
T_{PERIOD}	100-MHz CPUT and CPUC Period	Measured at crossing point V_{OX}	9.997001	10.00300	ns
T_{PERIOD}	133-MHz CPUT and CPUC Period	Measured at crossing point V_{OX}	7.497751	7.502251	ns
T_{PERIOD}	200-MHz CPUT and CPUC Period	Measured at crossing point V_{OX}	4.998500	5.001500	ns
T_{PERIOD}	266-MHz CPUT and CPUC Period	Measured at crossing point V_{OX}	3.748875	3.751125	ns
$T_{PERIODSS}$	100-MHz CPUT and CPUC Period, SSC	Measured at crossing point V_{OX}	9.997001	10.05327	ns
$T_{PERIODSS}$	133-MHz CPUT and CPUC Period, SSC	Measured at crossing point V_{OX}	7.497751	7.539950	ns
$T_{PERIODSS}$	200-MHz CPUT and CPUC Period, SSC	Measured at crossing point V_{OX}	4.998500	5.026634	ns
$T_{PERIODSS}$	266-MHz CPUT and CPUC Period, SSC	Measured at crossing point V_{OX}	3.748875	3.769975	ns
$T_{PERIODAbs}$	100-MHz CPUT and CPUC Absolute period	Measured at crossing point V_{OX}	9.912001	10.08800	ns
$T_{PERIODAbs}$	133-MHz CPUT and CPUC Absolute period	Measured at crossing point V_{OX}	7.412751	7.587251	ns
$T_{PERIODAbs}$	200-MHz CPUT and CPUC Absolute period	Measured at crossing point V_{OX}	4.913500	5.086500	ns
$T_{PERIODAbs}$	266-MHz CPUT and CPUC Absolute period	Measured at crossing point V_{OX}	3.663875	3.836125	ns
$T_{PERI-ODSSAbs}$	100-MHz CPUT and CPUC Absolute period, SSC	Measured at crossing point V_{OX}	9.912001	10.13827	ns
$T_{PERI-ODSSAbs}$	133-MHz CPUT and CPUC Absolute period, SSC	Measured at crossing point V_{OX}	7.412751	7.624950	ns
$T_{PERI-ODSSAbs}$	200-MHz CPUT and CPUC Absolute period, SSC	Measured at crossing point V_{OX}	4.913500	5.111634	ns
$T_{PERI-ODSSAbs}$	266-MHz CPUT and CPUC Absolute period, SSC	Measured at crossing point V_{OX}	3.663875	3.854975	ns
T_{CCJ}	CPUT/C Cycle to Cycle Jitter	Measured at crossing point V_{OX}	–	95	ps
T_R / T_F	CPUT and CPUC Rise and Fall Times	Measured from V_{OL} = 0.175 to V_{OH} = 0.525V	175	700	ps
T_{RFM}	Rise/Fall Matching	Determined as a fraction of $2*(T_R - T_F)/(T_R + T_F)$	–	20	%
ΔT_R	Rise Time Variation		–	250	ps
ΔT_F	Fall Time Variation		–	250	ps
TSKEW	Any CPU to CPU Clock Skew	Measured at crossing point Vox	–	100	ps
V_{HIGH}	Voltage High	Math averages *Figure 13*	660	850	mv
V_{LOW}	Voltage Low	Math averages *Figure 13*	–150	–	mv
V_{OX}	Crossing Point Voltage at 0.7V Swing		250	550	mv
V_{OVS}	Maximum Overshoot Voltage		–	V_{HIGH} + 0.3	V
V_{UDS}	Minimum Undershoot Voltage		–0.3	–	V
V_{RB}	Ring Back Voltage	See *Figure 13*. Measure SE	–	0.2	V
SRC					
T_{DC}	SRCT and SRCC Duty Cycle	Measured at crossing point V_{OX}	45	55	%
T_{PERIOD}	100-MHz SRCT and SRCC Period	Measured at crossing point V_{OX}	9.997001	10.00300	ns

AC Electrical Specifications (continued)

Parameter	Description	Condition	Min.	Max.	Unit
$T_{PERIODSS}$	100-MHz SRCT and SRCC Period, SSC	Measured at crossing point V_{OX}	9.997001	10.05327	ns
$T_{PERIODAbs}$	100-MHz SRCT and SRCC Absolute Period	Measured at crossing point V_{OX}	10.12800	9.872001	ns
$T_{PERI-ODSSAbs}$	100-MHz SRCT and SRCC Absolute Period, SSC	Measured at crossing point V_{OX}	9.872001	10.17827	ns
T_{SKEW}	Any SRCT/C to SRCT/C Clock Skew	Measured at crossing point V_{OX}	–	250	ps
TSKEW	Any SRCS clock to Any SRCS clock Skew	Measured at crossing point Vox	-	250	ps
T_{CCJ}	SRCT/C Cycle to Cycle Jitter	Measured at crossing point V_{OX}	–	125	ps
L_{ACC}	SRCT/C Long Term Accuracy	Measured at crossing point V_{OX}	–	300	ppm
T_R / T_F	SRCT and SRCC Rise and Fall Times	Measured from V_{OL} = 0.175 to V_{OH} = 0.525V	175	700	ps
T_{RFM}	Rise/Fall Matching	Determined as a fraction of $2*(T_R - T_F)/(T_R + T_F)$	–	20	%
ΔT_R	Rise TimeVariation		–	125	ps
ΔT_F	Fall Time Variation		–	125	ps
V_{HIGH}	Voltage High	Math averages *Figure 13*	660	850	mv
V_{LOW}	Voltage Low	Math averages *Figure 13*	–150	–	mv
V_{OX}	Crossing Point Voltage at 0.7V Swing		250	550	mV
V_{OVS}	Maximum Overshoot Voltage		–	V_{HIGH} + 0.3	V
V_{UDS}	Minimum Undershoot Voltage		–0.3	–	V
V_{RB}	Ring Back Voltage	See *Figure 13.* Measure SE	–	0.2	V
PCI					
T_{DC}	PCI Duty Cycle	Measurement at 1.5V	45	55	%
T_{PERIOD}	Spread Disabled PCI Period	Measurement at 1.5V	29.99100	30.00900	ns
$T_{PERIODSS}$	Spread Enabled PCI Period, SSC	Measurement at 1.5V	29.9910	30.15980	ns
$T_{PERIODAbs}$	Spread Disabled PCI Period	Measurement at 1.5V	29.49100	30.50900	ns
$T_{PERI-ODSSAbs}$	Spread Enabled PCI Period, SSC	Measurement at 1.5V	29.49100	30.65980	ns
T_{HIGH}	PCI high time	Measurement at 2.4V	12.0	–	ns
T_{LOW}	PCI low time	Measurement at 0.4V	12.0	–	ns
T_R / T_F	PCI rise and fall times	Measured between 0.8V and 2.0V	1.0	4.0	V/ns
T_{CCJ}	PCI Cycle to Cycle Jitter	Measurement at 1.5V	–	500	ps
USB					
T_{DC}	Duty Cycle	Measurement at 1.5V	45	55	%
T_{PERIOD}	Period	Measurement at 1.5V	20.83125	20.83542	ns
$T_{PERIODAbs}$	Absolute Period	Measurement at 1.5V	20.48125	21.18542	ns
T_{HIGH}	USB high time	Measurement at 2.4V	8.094	10.036	ns
T_{LOW}	USB low time	Measurement at 0.4V	7.694	9.836	ns
T_R / T_F	Rise and Fall Times	Measured between 0.8V and 2.0V	1.0	2.0	V/ns
T_{CCJ}	Cycle to Cycle Jitter	Measurement at 1.5V	–	350	ps
REF					
T_{DC}	REF Duty Cycle	Measurement at 1.5V	45	55	%
T_{PERIOD}	REF Period	Measurement at 1.5V	69.8203	69.8622	ns
$T_{PERIODAbs}$	REF Absolute Period	Measurement at 1.5V	68.82033	70.86224	ns

AC Electrical Specifications (continued)

Parameter	Description	Condition	Min.	Max.	Unit
T_R / T_F	REF Rise and Fall Times	Measured between 0.8V and 2.0V	0.5	4.0	V/ns
T_{CCJ}	REF Cycle to Cycle Jitter	Measurement at 1.5V	–	1000	ps
ENABLE/DISABLE and SET-UP					
T_{STABLE}	Clock Stabilization from Power-up		–	1.8	ms
T_{SS}	Stopclock Set-up Time		10.0	–	ns
T_{SH}	Stopclock Hold Time		0	–	ns

Test and Measurement Set-up

For PCI Single-ended Signals and Reference

The following diagram shows the test load configurations for the single-ended PCI, USB, and REF output signals.

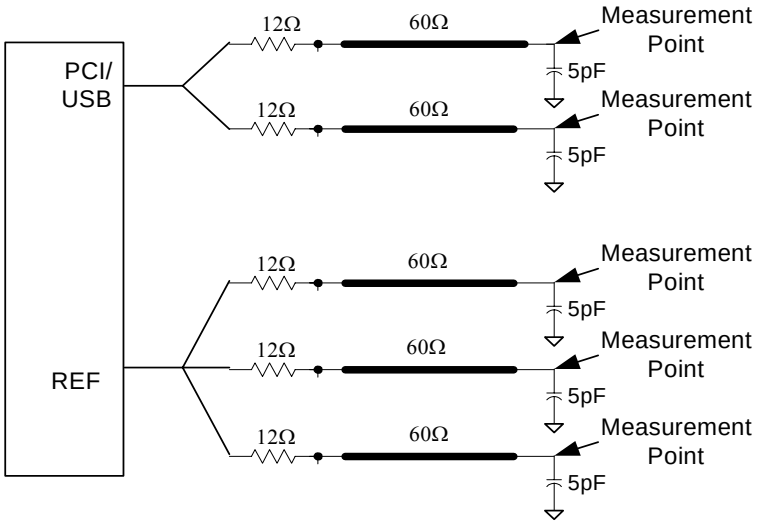


Figure 12. Single-ended Load Configuration

For Differential CPU and SRC Output Signals

The following diagram shows the test load configuration for the differential CPU and SRC outputs.

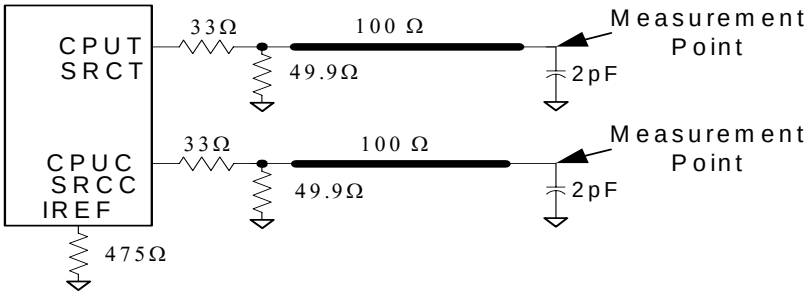


Figure 13. 0.7V Load Configuration

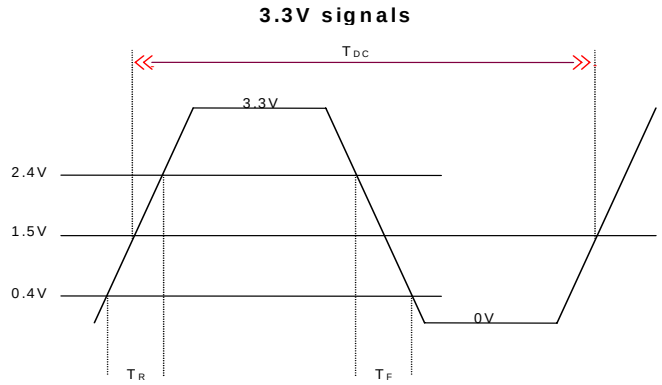


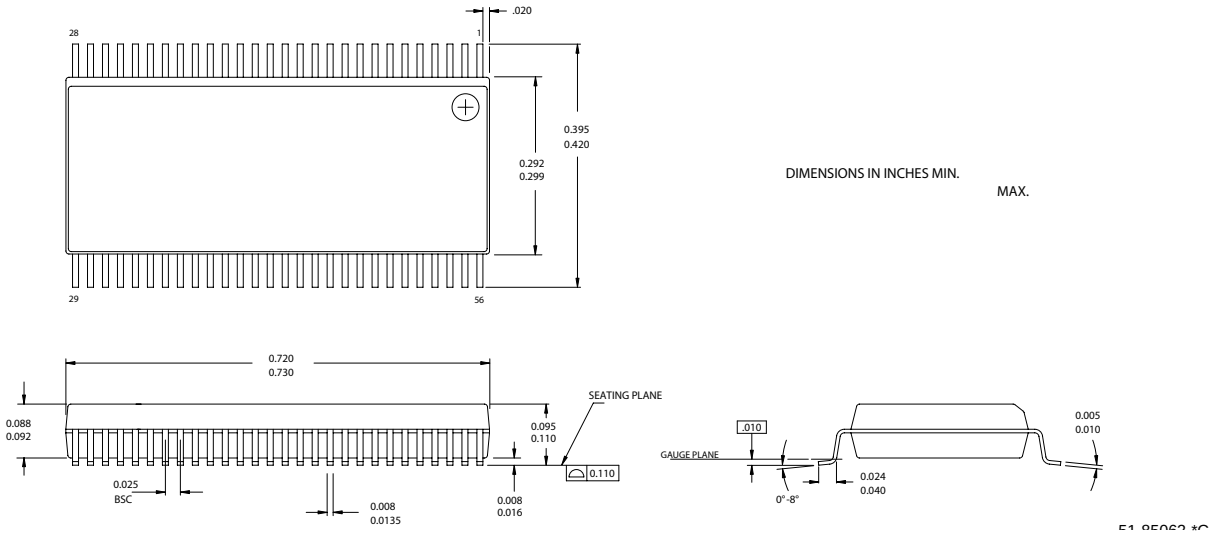
Figure 14. Single-ended Output Signals (for AC Parameters Measurement)

Ordering Information

Part Number	Package Type	Product Flow
Standard		
CY28RS400OC	56-pin SSOP	Commercial, 0° to 70°C
CY28RS400OCT	56-pin SSOP – Tape and Reel	Commercial, 0° to 70°C
CY28RS400ZC	56-pin TSSOP	Commercial, 0° to 70°C
CY28RS400ZCT	56-pin TSSOP – Tape and Reel	Commercial, 0° to 70°C
Lead-free		
CY28RS400OXC	56-pin SSOP	Commercial, 0° to 70°C
CY28RS400OXCT	56-pin SSOP – Tape and Reel	Commercial, 0° to 70°C
CY28RS400ZXC	56-pin TSSOP	Commercial, 0° to 70°C
CY28RS400ZXCT	56-pin TSSOP – Tape and Reel	Commercial, 0° to 70°C

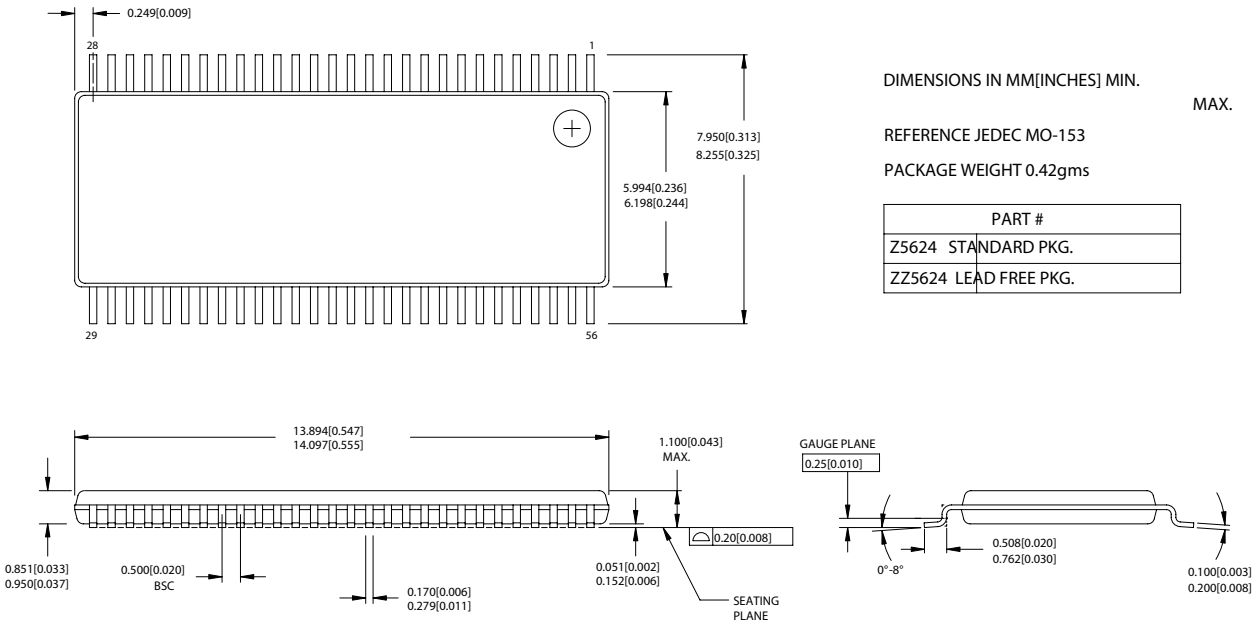
Package Diagrams

56-Lead Shrunk Small Outline Package O56



Package Diagrams (continued)

56-Lead Thin Shrunk Small Outline Package, Type II (6 mm x 12 mm) Z56



DIMENSIONS IN MM[INCHES] MIN.
MAX.

REFERENCE JEDEC MO-153

PACKAGE WEIGHT 0.42gms

PART #
Z5624 STANDARD PKG.
ZZ5624 LEAD FREE PKG.

51-85060-*C