M5M5256BP,FP,KP-70,-85,-10,-12,-15,-70L,-85L, -10L,-12L,-15L,-70LL,-85LL,-10LL,-12LL,-15LL

262144-BIT (32768-WORD BY 8-BIT) CMOS STATIC RAM

DESCRIPTION

This M5M5256BP, FP, KP is a 262144-bit CMOS static RAM organized as 32768-words by 8-bits which is fabricated using high-performance double polysilicon CMOS technology. The use of resistive load NMOS cells and CMOS periphery result in a high-density and low-power static RAM. It is ideal for the memory systems which require simple interface.

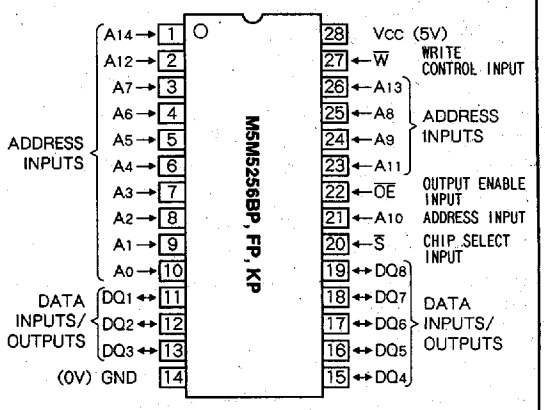
The stand-by current is low enough for a battery back-up application. It is mounted in a standard 28pin package and configured in an industrial standard 32K × 8-bit pinout.

FEATURES

Type name	Access time (max)	Power supply current	
		Active (max)	Stand-by (max)
M5M5256BP, FP, KP-70	70ns	70mA	2mA
M5M5256BP, FP, KP-85	85ns		
M5M5256BP, FP, KP-10	100ns		
M5M5256BP, FP, KP-12	120ns		
M5M5256BP, FP, KP-15	150ns		
M5M5256BP, FP, KP-70L	70ns		100 μA (Vcc = 5.5V) 50 μA (Vcc = 3.0V)
M5M5256BP, FP, KP-85L	85ns		
M5M5256BP, FP, KP-10L	100ns		
M5M5256BP, FP, KP-12L	120ns		
M5M5256BP, FP, KP-15L	150ns		
M5M5256BP, FP, KP-70LL	70ns		20 μA (Vcc = 5.5V) 10 μA (Vcc = 3.0V)
M5M5256BP, FP, KP-85LL	85ns		
M5M5256BP, FP, KP-10LL	100ns		
M5M5256BP, FP, KP-12LL	120ns		
M5M5256BP, FP, KP-15LL	150ns		

- Single +5V power supply
- No clocks, no refresh
- Data-hold on +2V power supply

PIN CONFIGURATION (TOP VIEW)



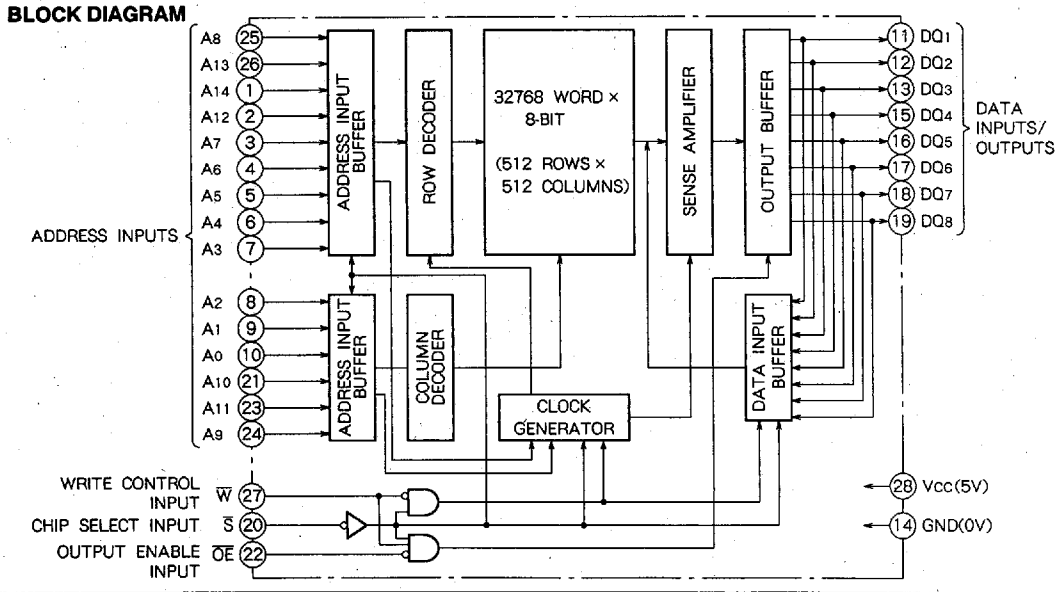
Outline 28P4(P)
28P2W-C(FP)
28P4Y(KP)

- Directly TTL compatible : All inputs and outputs
- Three-state outputs : OR-tie capability
- Simple memory expansion by $\overline{S}$
- $\overline{OE}$ prevents data contention in the I/O bus
- Common data I/O
- Package
  - M5M5256BP ..... 28pin 600mil DIP
  - M5M5256BKP ..... 28pin 300mil DIP
  - M5M5256BFP ..... 28pin small outline package(SOP)

APPLICATION

Small capacity memory units

BLOCK DIAGRAM



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FUNCTION

The operation mode of the M5M5256BP, FP, KP is determined by a combination of the device control inputs $\overline{S}$, $\overline{W}$ and $\overline{OE}$. Each mode is summarized in the function table.

A write cycle is executed whenever the low level $\overline{W}$ overlaps with the low level $\overline{S}$. The address must be set up before the write cycle and must be stable during the entire cycle. The data is latched into a cell on the trailing edge of $\overline{W}$, $\overline{S}$, whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained. The output enable $\overline{OE}$ directly controls the output stage. Setting the $\overline{OE}$ at a high level, the output stage is in a high-impedance state, and the data bus contention problem in the write cycle is eliminated.

A read cycle is executed by setting $\overline{W}$ at a high level and $\overline{OE}$ at a low level while $\overline{S}$ are in an active state.

When setting $\overline{S}$ at a high level, the chip is in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expansion by $\overline{S}$. The power supply current is reduced as low as the stand-by current which is specified as I_{CC3} or I_{CC4}, and the memory data can be held + 2V power supply, enabling battery back-up operation during power failure or power-down operation in the non-selected mode.

FUNCTION TABLE

$\overline{S}$	$\overline{W}$	$\overline{OE}$	Mode	DQ	Icc
H	X	X	Non selection	High-impedance	Stand-by
L	L	X	Write	D_{in}	Active
L	H	L	Read	D_{out}	Active
L	H	H		High-impedance	Active

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to GND	− 0.3 ~7	V
V_I	Input voltage	With respect to GND	− 0.3 ~V_{CC} + 0.3	V
V_O	Output voltage	With respect to GND	0 ~V_{CC}	V
P_d	Power dissipation	T_a = 25℃	700	mW
T_{opr}	Operating temperature		0~70	℃
T_{stg}	Storage temperature		− 65~150	℃

ELECTRICAL CHARACTERISTICS (T_a = 0~70℃, V_{CC} = 5V ± 10%, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits Min	Limits Typ	Limits Max	Unit
V_{IH}	High input voltage			2.2		V_{CC}+0.3	V
V_{IL}	Low input voltage			− 0.3		0.8	V
V_{OH}	High output voltage	I_{OH} = − 1mA		2.4			V
V_{OL}	Low output voltage	I_{OL} = 2mA				0.4	V
I_I	Input leakage current	V_I = 0~V_{CC}				± 1	μA
I_O	Output leakage current	$\overline{S}$ = V_{IH} or $\overline{OE}$ = V_{IH}, $V_{I/O}$ = 0~V_{CC}				± 1	μA
I_{CC1}	Active supply current(AC MOS level)	$\overline{S}$ < 0.2, $\overline{W}$ > V_{CC} − 0.2 output open Other inputs < 0.2 or > V_{CC} − 0.3 Min cycle			30	65	mA
I_{CC2}	Active supply current(AC TTL level)	$\overline{S}$ = V_{IL}, $\overline{W}$ = V_{IH} output open Other inputs = V_{IL} or V_{IH} Min cycle			35	70	mA
I_{CC3}	Stand by supply current	$\overline{S}$ ≧ V_{CC} − 0.2V Other inputs = 0~V_{CC}	BP, FP, KP			2	mA
			BP, FP, KP-L			100	μA
			BP, FP, KP-LL			20	μA
I_{CC4}	Stand by supply current	$\overline{S}$ = V_{IH}, other inputs = 0~V_{CC}				3	mA
C_I	Input capacitance (T_a = 25℃)	V_I = GND, V_I = 25mVrms, f = 1MHz				6	pF
C_O	Output capacitance (T_a = 25℃)	V_O = GND, V_O = 25mVrms, f = 1MHz				8	pF

Note 1. Direction for current flowing into IC is indicated as positive (no mark)
2. Typical value is V_{CC} = 5V, T_a = 25℃

SWITCHING CHARACTERISTICS (Ta = 0~70℃, Vcc = 5V ± 10%, unless otherwise noted)
Read cycle

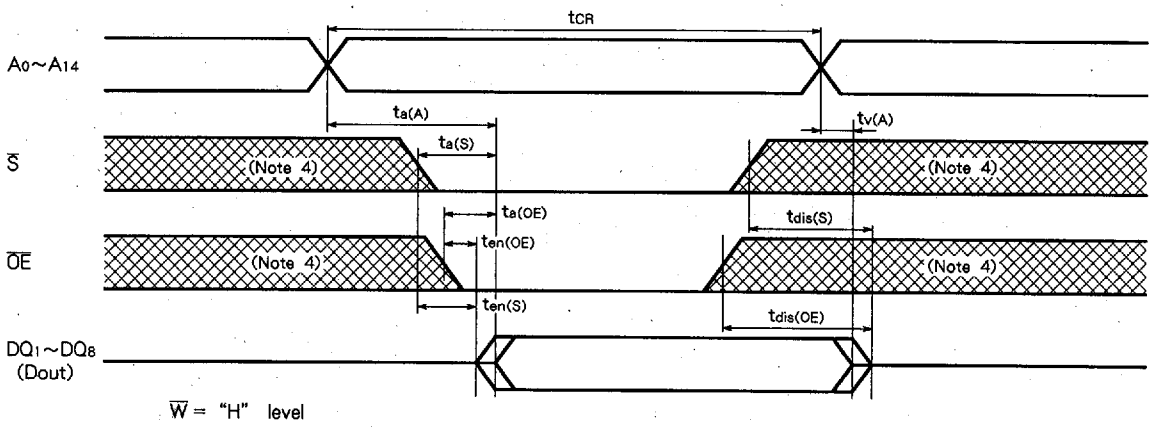
Symbol	Parameter	Limits										Unit
		M5M5256-70 M5M5256-70L M5M5256-70LL		M5M5256-85 M5M5256-85L M5M5256-85LL		M5M5256-10 M5M5256-10L M5M5256-10LL		M5M5256-12 M5M5256-12L M5M5256-12LL		M5M5256-15 M5M5256-15L M5M5256-15LL		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{CR}	Read cycle time	70		85		100		120		150		ns
$t_{a(A)}$	Address access time		70		85		100		120		150	ns
$t_{a(S)}$	Chip select access time		70		85		100		120		150	ns
$t_{a(OE)}$	Output enable access time		35		45		50		60		75	ns
$t_{dis(S)}$	Output disable time after $\overline{S}$ high		30		30		35		40		45	ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high		25		30		35		40		45	ns
$t_{en(S)}$	Output enable time after $\overline{S}$ low	5		5		10		10		10		ns
$t_{en(OE)}$	Output enable time after $\overline{OE}$ low	5		5		10		10		10		ns
$t_{v(A)}$	Data valid time after address change	20		20		20		20		20		ns

TIMING REQUIREMENTS (Ta = 0~70℃, Vcc = 5V ± 10%, unless otherwise noted)
Write cycle

Symbol	Parameter	Limits										Unit
		M5M5256-70 M5M5256-70L M5M5256-70LL		M5M5256-85 M5M5256-85L M5M5256-85LL		M5M5256-10 M5M5256-10L M5M5256-10LL		M5M5256-12 M5M5256-12L M5M5256-12LL		M5M5256-15 M5M5256-15L M5M5256-15LL		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{CW}	Write cycle time	70		85		100		120		150		ns
$t_{w(W)}$	Write pulse width	55		60		60		70		80		ns
$t_{su(A)}$	Address set up time	0		0		0		0		0		ns
$t_{su(A-WH)}$	Address set up time with respect to $\overline{W}$ high	65		75		80		85		90		ns
$t_{su(S)}$	Chip select set up time	65		75		80		85		90		ns
$t_{su(D)}$	Data set up time	30		35		35		40		50		ns
$t_{h(D)}$	Data hold time	0		0		0		0		0		ns
$t_{rec(W)}$	Write recovery time	0		0		0		0		0		ns
$t_{dis(W)}$	Output disable time after $\overline{W}$ low		25		30		35		40		45	ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high		25		30		35		40		45	ns
$t_{en(W)}$	Output enable time after $\overline{W}$ high	5		5		10		10		10		ns
$t_{en(OE)}$	Output enable time after $\overline{OE}$ low	5		5		10		10		10		ns

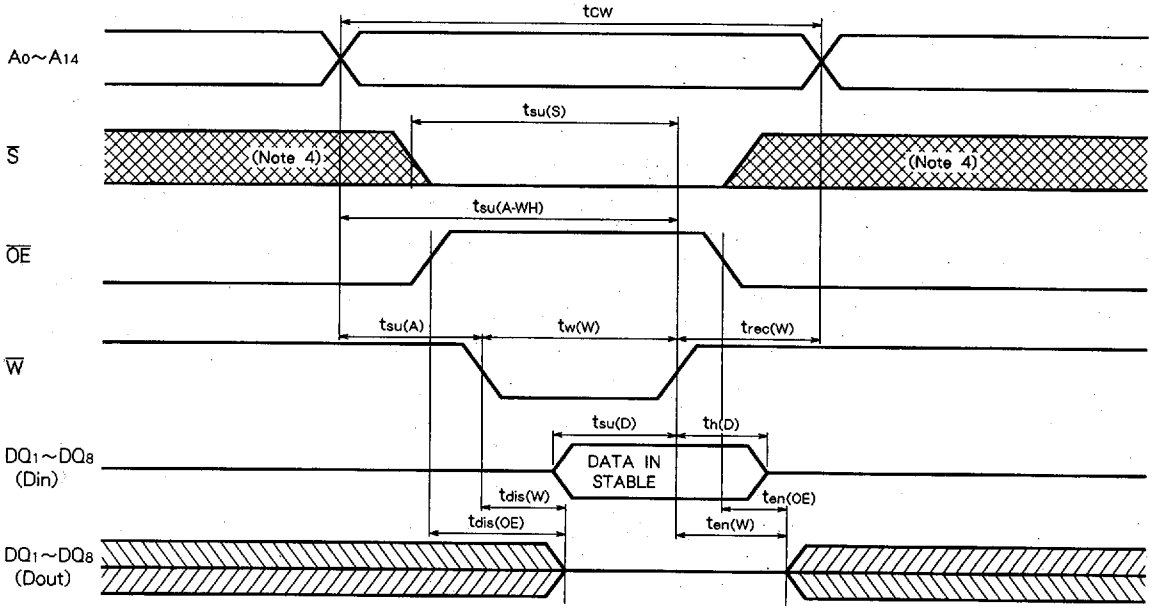
TIMING DIAGRAM

Read cycle



W = "H" level

Write cycle (W control)



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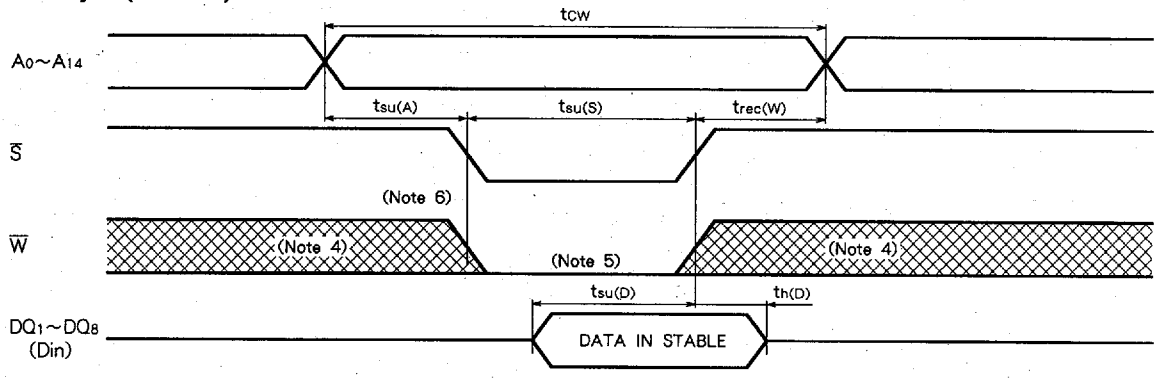
262144-BIT (32768-WORD BY 8-BIT) CMOS STATIC RAM

Write cycle ($\overline{S}$ control)



Note 3 : Test condition

Input pulse levels ..... V_{IH} = 2.4V, V_{IL} = 0.6V

Input rise and fall time 10ns

Reference levels ..... V_{OH} = V_{OL} = 1.5V

Transition is measured ±500mV from steady state voltage.(for t_{en}, t_{dis})

Output loads ..... Fig. 1, C_L = 100pF (BP, FP, KP-85, -10, -12, -15, -85L, -10L, -12L, -15L, -85LL, -10LL, -12LL, -15LL)

C_L = 30pF (BP, FP, KP-70, -70L, -70LL)

C_L = 5pF (for t_{en}, t_{dis})

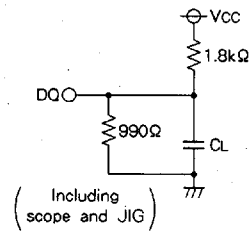


Fig. 1 Output load

Note 4. Hatching indicates the state is don't care.
5. Writing is executed in overlap of $\overline{S}$ and $\overline{W}$ low.
6. If $\overline{W}$ goes low simultaneously with or prior to $\overline{S}$, the output remains in the high-impedance state.
7. Don't apply inverted phase signal externally when DQ pin is in output mode.

POWER DOWN CHARACTERISTICS

ELECTRICAL CHARACTERISTICS (Ta = 0~70℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ	Max	
$V_{CC(PD)}$	Power down supply voltage			2			V
$V_{I(\overline{S})}$	Chip select input $\overline{S}$	2.2V ≦ $V_{CC(PD)}$		2.2			V
		2V ≦ $V_{CC(PD)}$ ≦ 2.2V			$V_{CC(PD)}$		
$I_{CC(PD)}$	Power down supply current	V_{CC} = 3V, 0ther inputs=3V	BP,FP,KP			2	mA
			BP,FP,KP-L			50	µA
			BP,FP,KP-LL			10*	µA

* Ta = 25℃, $I_{CC(PD)}$ = 1 µA

TIMING REQUIREMENTS (Ta = 0~70℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{su(PD)}$	Power down setup time		0			ns
$t_{rec(PD)}$	Power down recovery time		tCR			ns

POWER DOWN CHARACTERISTICS