Si5345/44/42 Rev D Data Sheet

10-Channel, Any-Frequency, Any-Output Jitter Attenuator/ Clock Multiplier

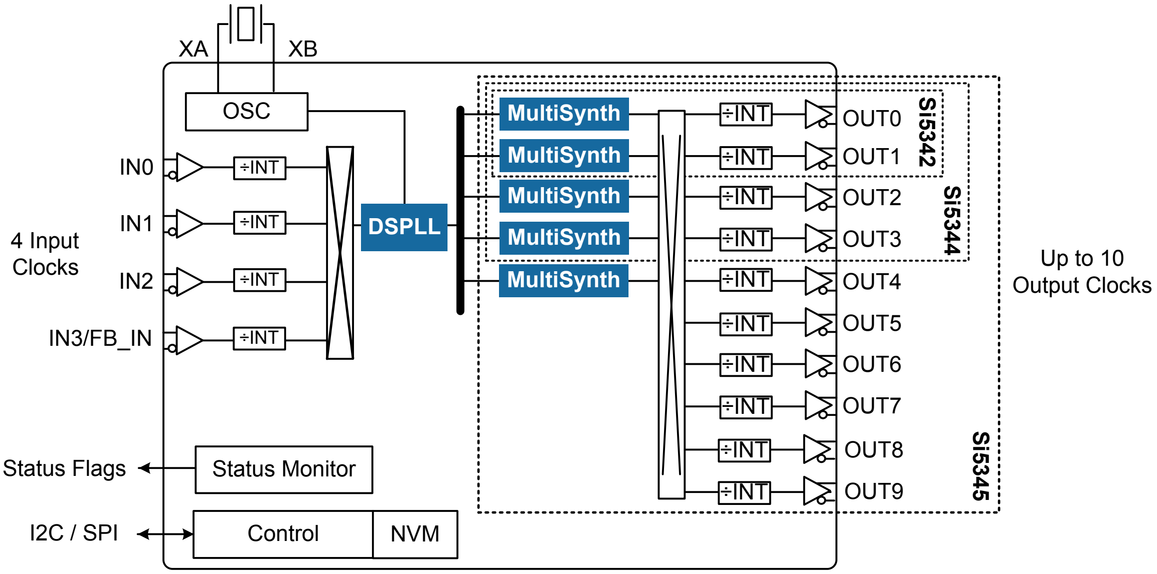
These jitter attenuating clock multipliers combine fourth-generation DSPLL™ and MultiSynth™ technologies to enable any-frequency clock generation and jitter attenuation for applications requiring the highest level of jitter performance. These devices are programmable via a serial interface with in-circuit programmable non-volatile memory (NVM) so they always power up with a known frequency configuration. They support free-run, synchronous, and holdover modes of operation, and offer both automatic and manual input clock switching. The loop filter is fully integrated on-chip, eliminating the risk of noise coupling associated with discrete solutions. Furthermore, the jitter attenuation bandwidth is digitally programmable, providing jitter performance optimization at the application level. Programming the Si5345/44/42 is easy with Silicon Labs' ClockBuilder Pro™ software. Factory preprogrammed devices are also available.

Applications:

- OTN muxponders and transponders
- 10/40/100 G networking line cards
- GbE/10 GbE/100 GbE Synchronous Ethernet (ITU-T G.8262)
- Carrier Ethernet switches
- SONET/SDH line cards
- Broadcast video
- Test and measurement
- ITU-T G.8262 (SyncE) compliant

KEY FEATURES

- Generates any combination of output frequencies from any input frequency
- Ultra-low jitter of 90 fs rms
- External Crystal: 25 to 54 MHz
- Input frequency range
  - Differential: 8 kHz to 750 MHz
  - LVCMOS: 8 kHz to 250 MHz
- Output frequency range
  - Differential: 100 Hz to 1028 MHz
  - LVCMOS: 100 Hz to 250 MHz
- Meets G.8262 EEC Option 1, 2 (SyncE)
- Highly configurable outputs compatible with LVDS, LVPECL, LVCMOS, CML, and HCSL with programmable signal amplitude
- Si5345: 4 input, 10 output, 64-QFN 9×9 mm
- Si5344: 4 input, 4 output, 44-QFN 7×7 mm
- Si5342: 4 input, 2 output, 44-QFN 7×7 mm



1. Features List

The Si5345/44/42 Rev D features are listed below:

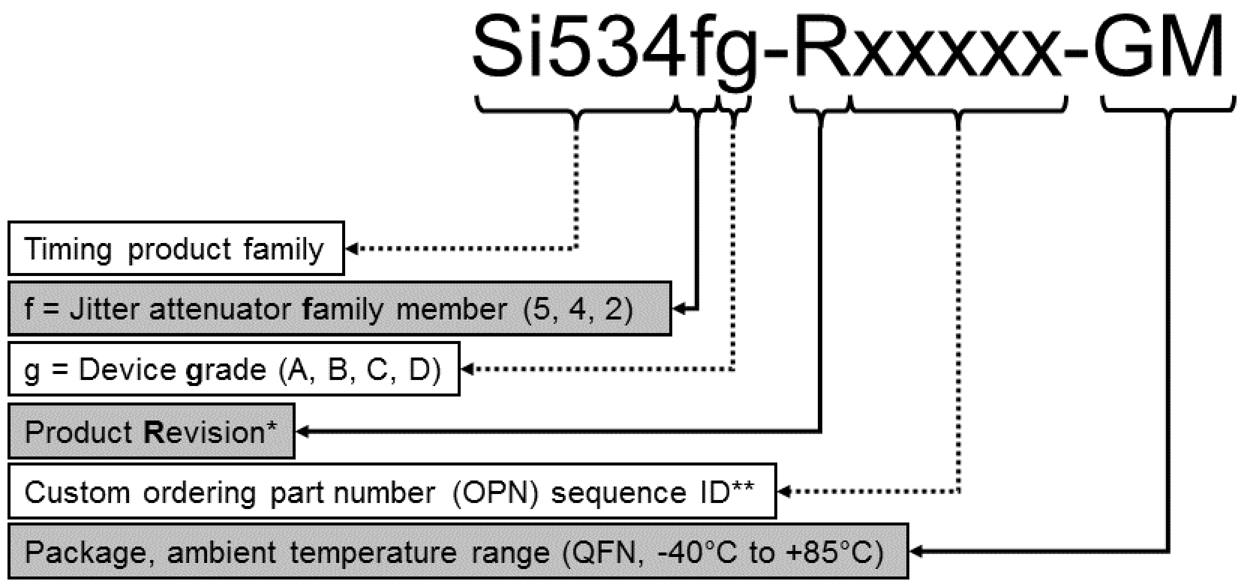
- Generates any combination of output frequencies from any input frequency
- Ultra-low jitter of 90 fs rms
- Input frequency range
  - Differential: 8 kHz–750 MHz
  - LVCMOS: 8 kHz–250 MHz
- Output frequency range
  - Differential: 100 Hz to 1028 MHz
  - LVCMOS: 100 Hz to 250 MHz
- Programmable jitter attenuation bandwidth: 0.1 Hz to 4 kHz
- Meets G.8262 EEC Option 1, 2 (SyncE)
- Highly configurable outputs compatible with LVDS, LVPECL, LVCMOS, CML, and HCSL with programmable signal amplitude
- Status monitoring (LOS, OOF, LOL)
- Hitless input clock switching: automatic or manual
- Locks to gapped clock inputs
- Free-run and holdover modes
- Optional zero delay mode
- Fastlock feature for low nominal bandwidths
- Glitchless on the fly output frequency changes
- DCO mode: as low as 0.001 ppb step size
- Core voltage
  - V_{DD}: 1.8 V ±5%
  - V_{DDA}: 3.3 V ±5%
- Independent output clock supply pins
  - 3.3 V, 2.5 V, or 1.8 V
- Serial interface: I^2C or SPI
- In-circuit programmable with non-volatile OTP memory
- ClockBuilder Pro software simplifies device configuration
- Si5345: 4 input, 10 output, 64-QFN 9×9 mm
- Si5344: 4 input, 4 output, 44-QFN 7×7 mm
- Si5342: 4 input, 2 output, 44-QFN 7×7 mm
- Temperature range: –40 to +85 °C
- Pb-free, RoHS-6 compliant

2. Ordering Guide

Ordering Part Number (OPN)	Number of Input/ Output Clocks	Output Clock Frequency Range (MHz)	Supported Frequency Synthesis Modes	Package	Temperature Range
Si5345					
Si5345A-D-GM[1, 2]	4/10	0.001 to 1028 MHz	Integer and Fractional	64-QFN 9×9 mm	–40 to 85 °C
Si5345B-D-GM[1, 2]		0.001 to 350 MHz			
Si5345C-D-GM[1, 2]		0.001 to 1028 MHz	Integer Only		
Si5345D-D-GM[1, 2]		0.001 to 350 MHz			
Si5344					
Si5344A-D-GM[1, 2]	4/4	0.001 to 1028 MHz	Integer and Fractional	44-QFN 7×7 mm	–40 to 85 °C
Si5344B-D-GM[1, 2]		0.001 to 350 MHz			
Si5344C-D-GM[1, 2]		0.001 to 1028 MHz	Integer Only		
Si5344D-D-GM[1, 2]		0.001 to 350 MHz			
Si5342					
Si5342A-D-GM[1, 2]	4/2	0.001 to 1028 MHz	Integer and Fractional	44-QFN 7×7 mm	–40 to 85 °C
Si5342B-D-GM[1, 2]		0.001 to 350 MHz			
Si5342C-D-GM[1, 2]		0.001 to 1028 MHz	Integer Only		
Si5342D-D-GM[1, 2]		0.001 to 350 MHz			
Si5345/44/42-D-EVB					
Si5345-D-EVB	—	—	—	Evaluation Board	—
Si5344-D-EVB					
Si5342-D-EVB					

Notes:

1. Add an R at the end of the OPN to denote tape and reel ordering options.
2. Custom, factory preprogrammed devices are available. Ordering part numbers are assigned by Silicon Labs and the ClockBuilder Pro software utility. Custom part number format is “Si5345A-Dxxxxx-GM” where “xxxxx” is a unique numerical sequence representing the preprogrammed configuration.



*See Ordering Guide table for current product revision
** 5 digits; assigned by ClockBuilder Pro

Figure 2.1. Ordering Part Number Fields

3. Functional Description

The Si5345's internal DSPLL provides jitter attenuation and any-frequency multiplication of the selected input frequency. Fractional input dividers (P) allow the DSPLL to perform hitless switching between input clocks (INx) that are fractionally related. Input switching is controlled manually or automatically using an internal state machine. The oscillator circuit (OSC) provides a frequency reference which determines output frequency stability and accuracy while the device is in free-run or holdover mode. The high-performance MultiSynth dividers (N) generate integer or fractionally related output frequencies for the output stage. A crosspoint switch connects any of the MultiSynth generated frequencies to any of the outputs. Additional integer division (R) determines the final output frequency.

3.1 Frequency Configuration

The frequency configuration of the DSPLL is programmable through the serial interface and can also be stored in non-volatile memory. The combination of fractional input dividers (P_n/P_d), fractional frequency multiplication (M_n/M_d), fractional output MultiSynth division (N_n/N_d), and integer output division (R_n) allows the generation of virtually any output frequency on any of the outputs. All divider values for a specific frequency plan are easily determined using the ClockBuilder Pro utility.

3.2 DSPLL Loop Bandwidth

The DSPLL loop bandwidth determines the amount of input clock jitter attenuation. Register configurable DSPLL loop bandwidth settings in the range of 0.1 Hz to 4 kHz are available for selection. Since the loop bandwidth is controlled digitally, the DSPLL will always remain stable with less than 0.1 dB of peaking regardless of the loop bandwidth selection.

3.3 Fastlock Feature

Selecting a low DSPLL loop bandwidth (e.g. 0.1 Hz) will generally lengthen the lock acquisition time. The fastlock feature allows setting a temporary Fastlock Loop Bandwidth that is used during the lock acquisition process. Higher fastlock loop bandwidth settings will enable the DSPLLs to lock faster. Fastlock Loop Bandwidth settings of in the range of 100 Hz to 4 kHz are available for selection. The DSPLL will revert to its normal loop bandwidth once lock acquisition has completed.

3.4 Modes of Operation

Once initialization is complete the DSPLL operates in one of four modes: Free-run Mode, Lock Acquisition Mode, Locked Mode, or Holdover Mode. A state diagram showing the modes of operation is shown in Figure 3.1 Modes of Operation on page 5. The following sections describe each of these modes in greater detail.

3.4.1 Initialization and Reset

Once power is applied, the device begins an initialization period where it downloads default register values and configuration data from NVM and performs other initialization tasks. Communicating with the device through the serial interface is possible once this initialization period is complete. No clocks will be generated until the initialization is complete. There are two types of resets available. A hard reset is functionally similar to a device power-up. All registers will be restored to the values stored in NVM, and all circuits including the serial interface will be restored to their initial state. A hard reset is initiated using the RSTb pin or by asserting the hard reset register bit. A soft reset bypasses the NVM download. It is simply used to initiate register configuration changes.

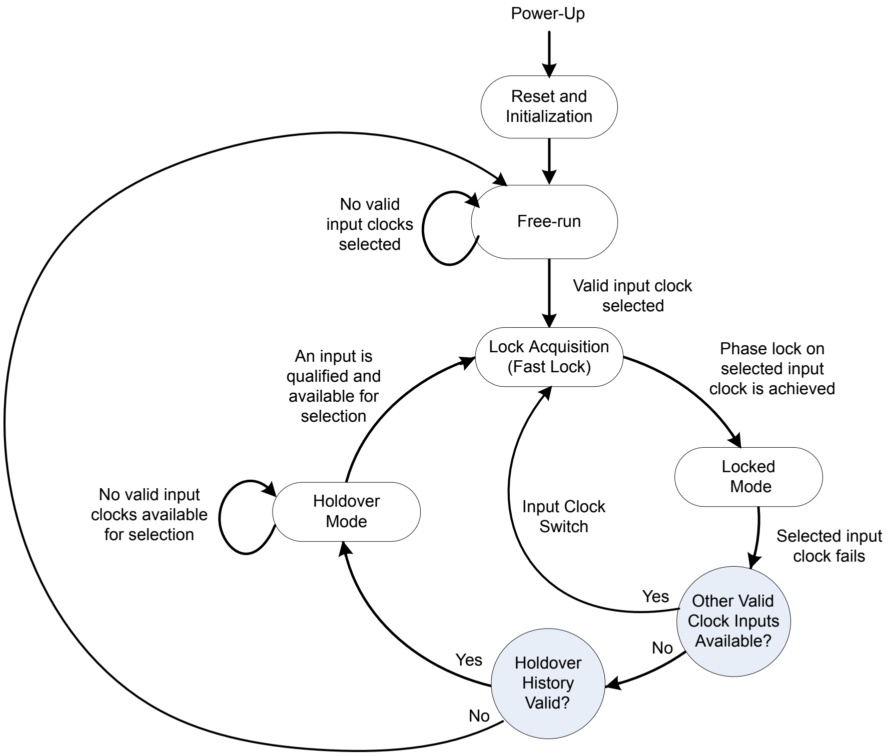


Figure 3.1. Modes of Operation

3.4.2 Freerun Mode

The DSPLL will automatically enter freerun mode once power is applied to the device and initialization is complete. The frequency accuracy of the generated output clocks in freerun mode is entirely dependent on the frequency accuracy of the external crystal or reference clock on the XA/XB pins. For example, if the crystal frequency is ±100 ppm, then all the output clocks will be generated at their configured frequency ±100 ppm in freerun mode. Any drift of the crystal frequency will be tracked at the output clock frequencies. A TCXO or OCXO is recommended for applications that need better frequency accuracy and stability while in freerun or holdover modes.

3.4.3 Lock Acquisition Mode

The device monitors all inputs for a valid clock. If at least one valid clock is available for synchronization, the DSPLL will automatically start the lock acquisition process. If the fast lock feature is enabled, the DSPLL will acquire lock using the Fastlock Loop Bandwidth setting and then transition to the DSPLL Loop Bandwidth setting when lock acquisition is complete. During lock acquisition the outputs will generate a clock that follows the VCO frequency change as it pulls in to the input clock frequency.

3.4.4 Locked Mode

Once locked, the DSPLL will generate output clocks that are both frequency and phase locked to their selected input clocks. At this point, any XTAL frequency drift will not affect the output frequency. A loss of lock pin (LOL) and status bit indicate when lock is achieved. See 3.8.4 LOL Detection for more details on the operation of the loss-of-lock circuit.

3.4.5 Holdover Mode

The DSPLL will automatically enter holdover mode when the selected input clock becomes invalid and no other valid input clocks are available for selection. The DSPLL uses an averaged input clock frequency as its final holdover frequency to minimize the disturbance of the output clock phase and frequency when an input clock suddenly fails. The holdover circuit for the DSPLL stores up to 120 seconds of historical frequency data while locked to a valid clock input. The final averaged holdover frequency value is calculated from a programmable window within the stored historical frequency data. Both the window size and the delay are programmable as shown in the figure below. The window size determines the amount of holdover frequency averaging. The delay value allows ignoring frequency data that may be corrupt just before the input clock failure.

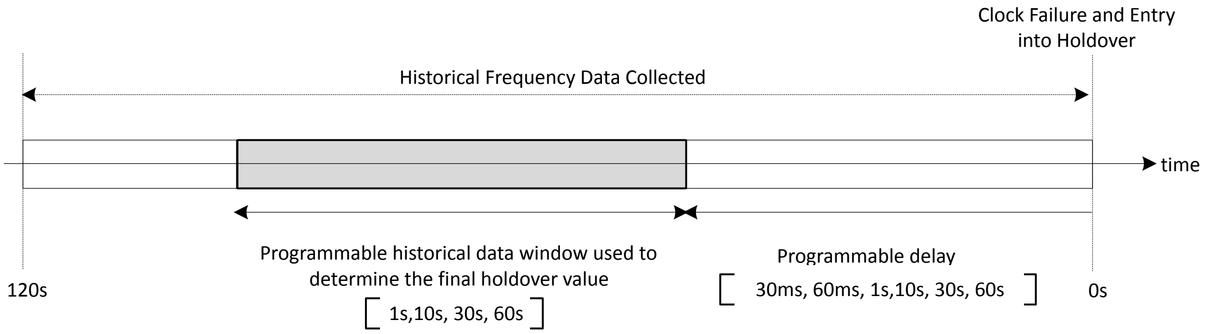


Figure 3.2. Programmable Holdover Window

When entering holdover, the DSPLL will pull its output clock frequency to the calculated averaged holdover frequency. While in holdover, the output frequency drift is entirely dependent on the external crystal or external reference clock connected to the XA/XB pins. If the clock input becomes valid, the DSPLL will automatically exit the holdover mode and re-acquire lock to the new input clock. This process involves pulling the output clock frequency to achieve frequency and phase lock with the input clock. This pull-in process is glitchless and its rate is controlled by the DSPLL or the Fastlock bandwidth.

The DSPLL output frequency when exiting holdover can be ramped (recommend). Just before the exit is initiated, the difference between the current holdover frequency and the new desired frequency is measured. Using the calculated difference and a user-selectable ramp rate, the output is linearly ramped to the new frequency. The ramp rate can be 0.2 ppm/s, 40,000 ppm/s, or any of about 40 values in between. The DSPLL loop BW does not limit or affect ramp rate selections (and vice versa). CBPro defaults to ramped exit from holdover. The same ramp rate settings are used for both exit from holdover and ramped input switching. For more information on ramped input switching, see 3.7.4 Ramped Input Switching.

Note: If ramped holdover exit is not selected, the holdover exit is governed either by (1) the DSPLL loop BW or (2) a user-selectable holdover exit BW.

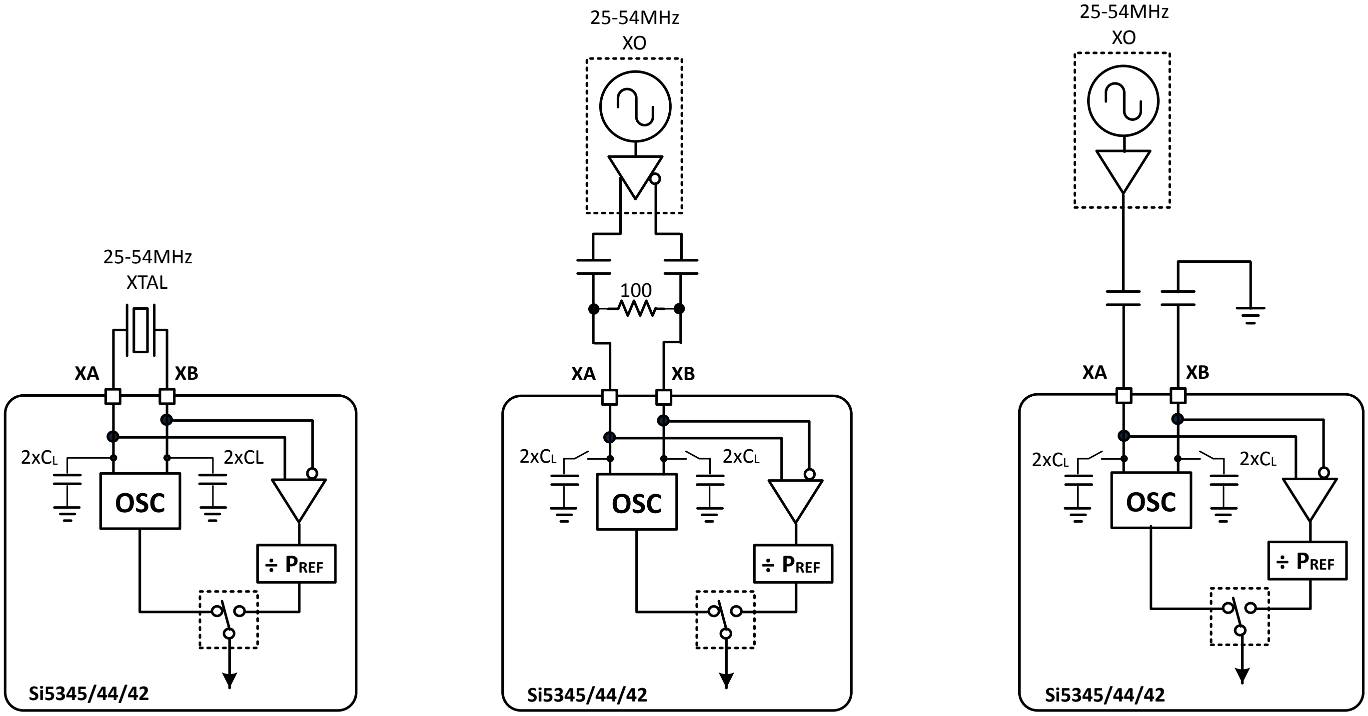
3.5 External Reference (XA/XB)

An external crystal (XTAL) is used in combination with the internal oscillator (OSC) to produce an ultra low jitter reference clock for the DSPLL and for providing a stable reference for the free-run and holdover modes. A simplified diagram is shown in Figure 3.3 Crystal Resonator and External Reference Clock Connection Options on page 7. The device includes internal XTAL loading capacitors which eliminates the need for external capacitors and also has the benefit of reduced noise coupling from external sources. Refer to Table 5.12 Crystal Specifications on page 36 for crystal specifications. A crystal in the range of 48 MHz to 54 MHz is recommended for best jitter performance. Frequency offsets due to CL mismatch can be adjusted using the frequency adjustment feature which allows frequency adjustments of ±200 ppm. The Si5345/44/42 Family Reference Manual provides additional information on PCB layout recommendations for the crystal to ensure optimum jitter performance.

To achieve optimal jitter performance and minimize BOM cost, a crystal is recommended on the XA/XB reference input. For SyncE line card PLL applications (e.g. loop bandwidth set to 0.1 Hz), a TCXO is required on the XA/XB reference to minimize wander and to provide a stable holdover reference. See the Si5345/44/42 Family Reference Manual for more information. Selection between the external XTAL or REFCLK is controlled by register configuration. The internal crystal loading capacitors (CL) are disabled in the REFCLK mode. Refer to Table 5.3 Input Clock Specifications on page 25 for REFCLK requirements when using this mode. A PREF divider is available to accommodate external clock frequencies higher than 54 MHz. Frequencies in the range of 48 MHz to 54 MHz will achieve the best output jitter performance.

3.6 Digitally Controlled Oscillator (DCO) Mode

The output MultiSynths support a DCO mode where their output frequencies are adjustable in predefined steps defined by frequency step words (FSW). The frequency adjustments are controlled through the serial interface or by pin control using frequency increment (FINC) or decrement (FDEC). A FINC will add the frequency step word to the DSPLL output frequency, while a FDEC will decrement it. Any number of MultiSynths can be updated at once or independently controlled. The DCO mode is available when the DSPLL is operating in either free-run or locked mode.



Crystal Resonator Connection

Differential XO Connection

Single-Ended XO Connection

Figure 3.3. Crystal Resonator and External Reference Clock Connection Options

3.7 Inputs (IN0, IN1, IN2, IN3)

There are four inputs that can be used to synchronize the DSPLL. The inputs accept both differential and single-ended clocks. Input selection can be manual (pin or register controlled) or automatic with user definable priorities.

3.7.1 Manual Input Switching (IN0, IN1, IN2, IN3)

Input clock selection can be made manually using the IN_SEL[1:0] pins or through a register. A register bit determines input selection as pin selectable or register selectable. The IN_SEL pins are selected by default. If there is no clock signal on the selected input, the device will automatically enter free-run or holdover mode. When the zero delay mode is enabled, IN3 becomes the feedback input (FB_IN) and is not available for selection as a clock input.

Table 3.1. Manual Input Selection Using IN_SEL[1:0] Pins

IN_SEL[1:0]		Selected Input	
		Zero Delay Mode Disabled	Zero Delay Mode Enabled
0	0	IN0	IN0
0	1	IN1	IN1
1	0	IN2	IN2
1	1	IN3	Reserved

3.7.2 Automatic Input Selection (IN0, IN1, IN2, IN3)

An automatic input selection state machine is available in addition to the manual switching option. In automatic mode, the selection criteria is based on input clock qualification, input priority, and the revertive option. Only input clocks that are valid can be selected by the automatic clock selection state machine. If there are no valid input clocks available the DSPLL will enter the holdover mode. With revertive switching enabled, the highest priority input with a valid input clock is always selected. If an input with a higher priority becomes valid then an automatic switchover to that input will be initiated. With non-revertive switching, the active input will always remain selected while it is valid. If it becomes invalid an automatic switchover to a valid input with the highest priority will be initiated.

3.7.3 Hitless Input Switching

Hitless switching is a feature that prevents a phase offset from propagating to the output when switching between two clock inputs that have a fixed phase relationship. A hitless switch can only occur when the two input frequencies are frequency locked meaning that they have to be exactly at the same frequency, or at a fractional frequency relationship to each other. When hitless switching is enabled, the DSPLL simply absorbs the phase difference between the two input clocks during a input switch. When disabled, the phase difference between the two inputs is propagated to the output at a rate determined by the DSPLL Loop Bandwidth. The hitless switching feature supports clock frequencies down to the minimum input frequency of 8 kHz.

3.7.4 Ramped Input Switching

When switching between two plesiochronous input clocks (i.e., the frequencies are "almost the same" but not quite), ramped input switching should be enabled to ensure a smooth transition between the two inputs. Ramped input switching avoids frequency transients and overshoot when switching between frequencies and so is the default switching mode in CBPro. The feature should be turned off when switching between input clocks that are always frequency locked (i.e., are always the same exact frequency). The same ramp rate settings are used for both holdover exit and clock switching. For more information on ramped exit from holdover see 3.4.5 Holdover Mode.

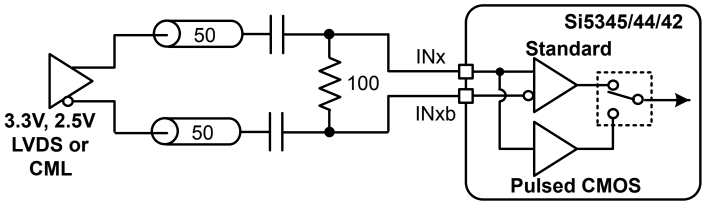
3.7.5 Glitchless Input Switching

The DSPLL has the ability of switching between two input clock frequencies that are up to ±500 ppm apart. The DSPLL will pull-in to the new frequency using the DSPLL Loop Bandwidth or using the Fastlock Loop Bandwidth if enabled. The loss of lock (LOL) indicator will assert while the DSPLL is pulling-in to the new clock frequency. There will be no abrupt phase change at the output during the transition.

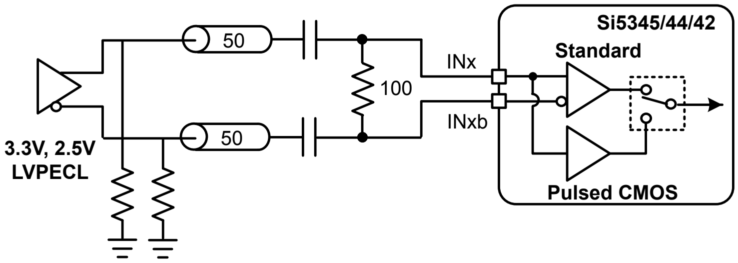
3.7.6 Input Configuration and Terminations

Each of the inputs can be configured as differential or single-ended LVCMOS. The recommended input termination schemes are shown in Figure 14. Differential signals must be ac-coupled, while single-ended LVCMOS signals can be ac or dc-coupled. Unused inputs can be disabled and left unconnected when not in use.

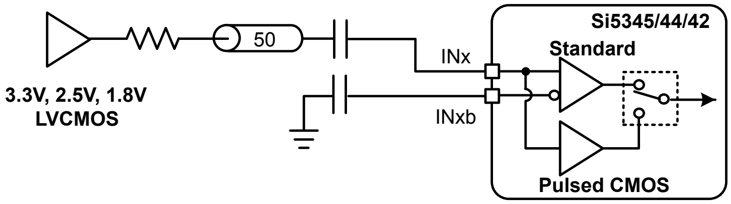
Standard AC Coupled Differential LVDS



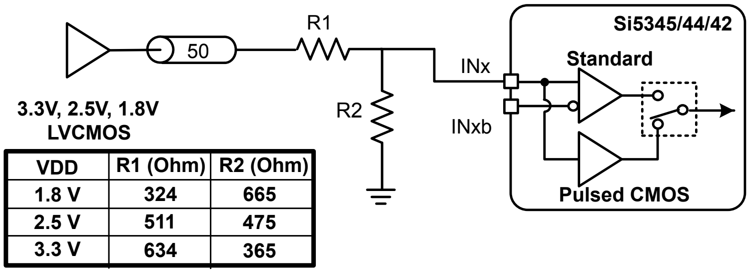
Standard AC Coupled Differential LVPECL



Standard AC Coupled Single Ended



Pulsed CMOS DC Coupled Single Ended



VDD	R1 (Ohm)	R2 (Ohm)
1.8 V	324	665
2.5 V	511	475
3.3 V	634	365

Figure 3.4. Termination of Differential and LVCMOS Input Signals

3.7.7 Synchronizing to Gapped Input Clocks

The DSPLL supports locking to an input clock that has missing periods. This is also referred to as a gapped clock. The purpose of gapped clocking is to modulate the frequency of a periodic clock by selectively removing some of its cycles. Gapping a clock severely increases its jitter so a phase-locked loop with high jitter tolerance and low loop bandwidth is required to produce a low-jitter periodic clock. The resulting output will be a periodic non-gapped clock with an average frequency of the input with its missing cycles. For example, an input clock of 100 MHz with one cycle removed every 10 cycles will result in a 90 MHz periodic non-gapped output clock. This is shown in the following figure. For more information on gapped clocks, see “AN561: Introduction to Gapped Clocks and PLLs”.

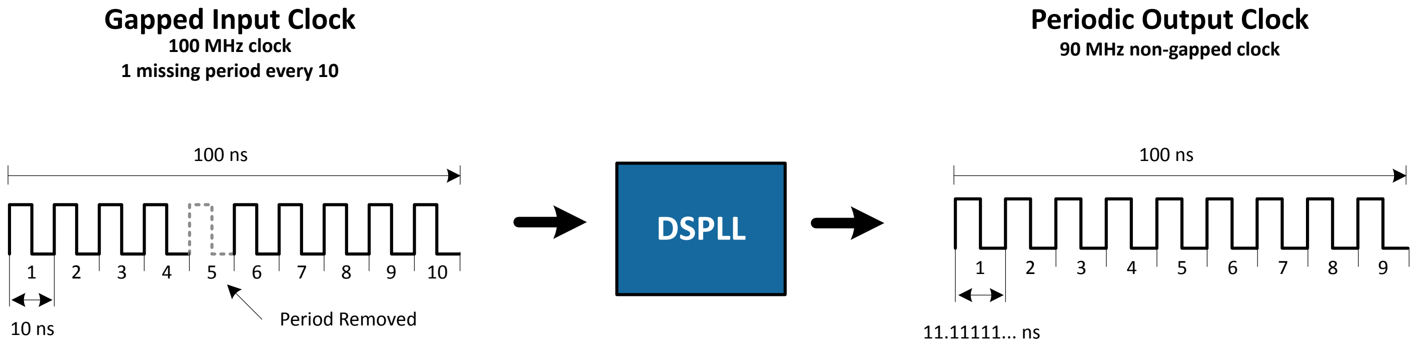


Figure 3.5. Generating an Averaged Clock Output Frequency from a Gapped Clock Input

A valid gapped clock input must have a minimum frequency of 10 MHz with a maximum of two missing cycles out of every eight. Locking to a gapped clock will not trigger the LOS, OOF, and LOL fault monitors. Clock switching between gapped clocks may violate the hitless switching specification in Table 5.8 Performance Characteristics on page 31 when the switch occurs during a gap in either input clock.

3.8 Fault Monitoring

All four input clocks (IN0, IN1, IN2, IN3/FB_IN) are monitored for loss of signal (LOS) and out-of-frequency (OOF) as shown in the figure below. The reference at the XA/XB pins is also monitored for LOS since it provides a critical reference clock for the DSPLL. There is also a Loss Of Lock (LOL) indicator which is asserted when the DSPLL loses synchronization.

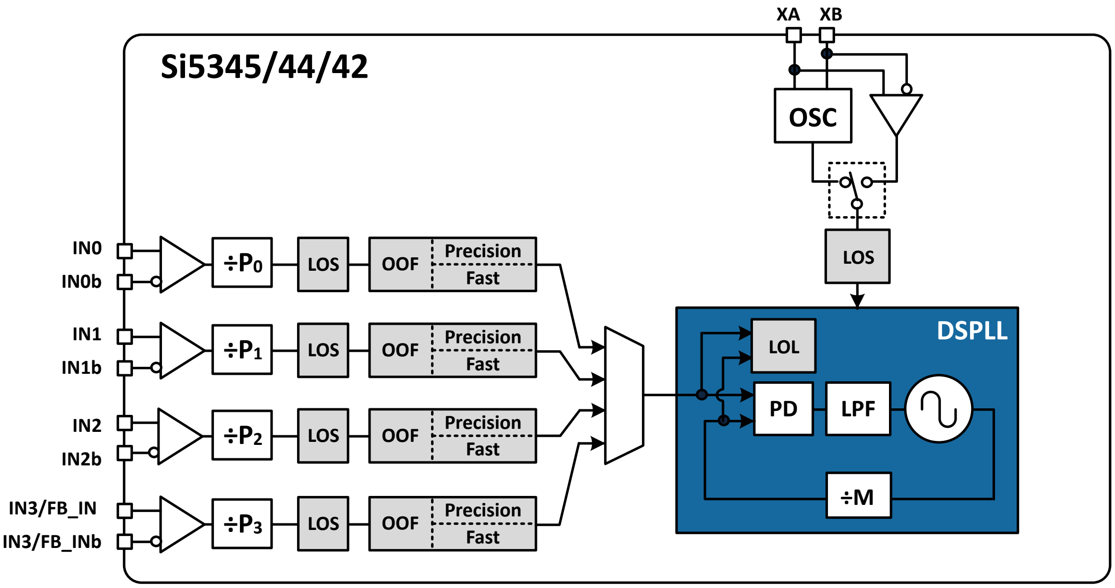


Figure 3.6. Si5345/44/42 Fault Monitors

3.8.1 Input LOS Detection

The loss of signal monitor measures the period of each input clock cycle to detect phase irregularities or missing clock edges. Each of the input LOS circuits has its own programmable sensitivity which allows ignoring missing edges or intermittent errors. Loss of signal sensitivity is configurable using the ClockBuilder Pro utility.

The LOS status for each of the monitors is accessible by reading a status register. The live LOS register always displays the current LOS state and a sticky register always stays asserted until cleared. An option to disable any of the LOS monitors is also available.

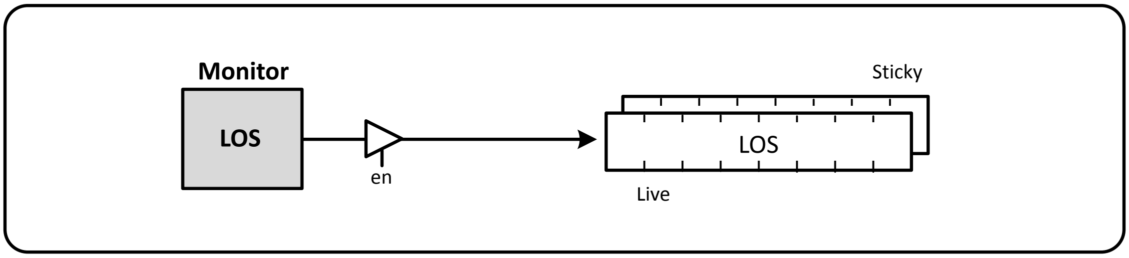


Figure 3.7. LOS Status Indicators

3.8.2 XA/XB LOS Detection

A LOS monitor is available to ensure that the external crystal or reference clock is valid. By default the output clocks are disabled when XAXB_LOS is detected. This feature can be disabled such that the device will continue to produce output clocks when XAXB_LOS is detected.

3.8.3 OOF Detection

Each input clock is monitored for frequency accuracy with respect to a OOF reference which it considers as its “0_ppm” reference. This OOF reference can be selected as either:

- XA/XB pins
- Any input clock (IN0, IN1, IN2, IN3)

The final OOF status is determined by the combination of both a precise OOF monitor and a fast OOF monitor as shown in the figure below. An option to disable either monitor is also available. The live OOF register always displays the current OOF state, and its sticky register bit stays asserted until cleared.

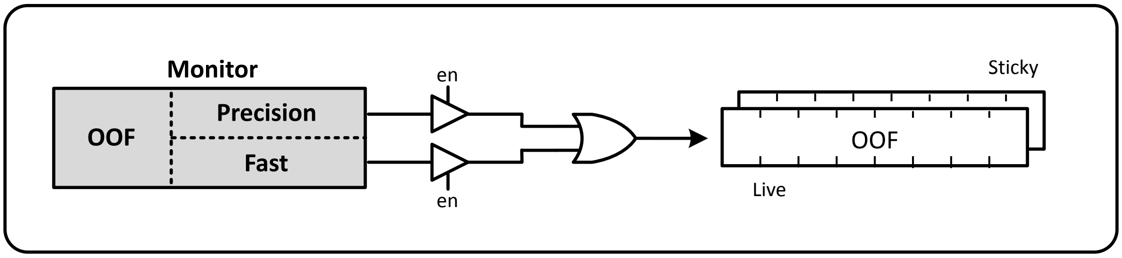


Figure 3.8. OOF Status Indicator

3.8.3.1 Precision OOF Monitor

The precision OOF monitor circuit measures the frequency of all input clocks to within ±1/16 ppm accuracy with respect to the selected OOF frequency reference. A valid input clock frequency is one that remains within the OOF frequency range which is register configurable up to ±500 ppm in steps of 1/16 ppm. A configurable amount of hysteresis is also available to prevent the OOF status from toggling at the failure boundary. An example is shown in the figure below. In this case, the OOF monitor is configured with a valid frequency range of ±6 ppm and with 2 ppm of hysteresis. An option to use one of the input pins (IN0–IN3) as the 0 ppm OOF reference instead of the XA/XB pins is available. This option is register configurable.

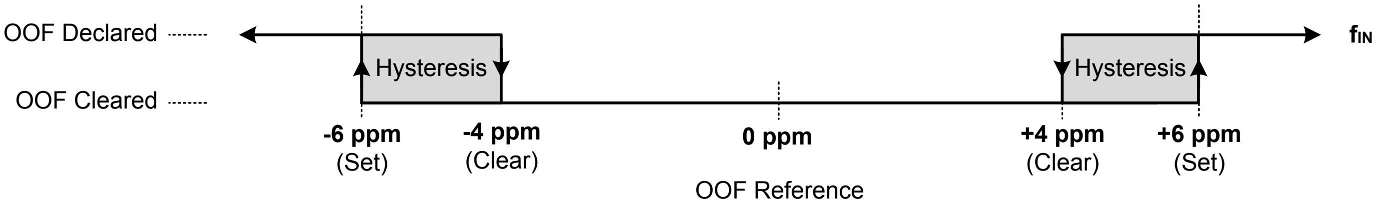


Figure 3.9. Example of Precise OOF Monitor Assertion and Deassertion Triggers

3.8.3.2 Fast OOF Monitor

Because the precision OOF monitor needs to provide 1/16 ppm of frequency measurement accuracy, it must measure the monitored input clock frequencies over a relatively long period of time. This may be too slow to detect an input clock that is quickly ramping in frequency. An additional level of OOF monitoring called the Fast OOF monitor runs in parallel with the precision OOF monitors to quickly detect a ramping input frequency. The Fast OOF monitor asserts OOF on an input clock frequency that has changed by greater than ±4000 ppm.

3.8.4 LOL Detection

The Loss Of Lock (LOL) monitor asserts a LOL register bit when the DSPLL has lost synchronization with its selected input clock.

There is also a dedicated loss of lock pin that reflects the loss of lock condition. The LOL monitor functions by measuring the frequency difference between the input and feedback clocks at the phase detector. There are two LOL frequency monitors, one that sets the LOL indicator (LOL Set) and another that clears the indicator (LOL Clear). An optional timer is available to delay clearing of the LOL indicator to allow additional time for the DSPLL to completely lock to the input clock. The timer is also useful to prevent the LOL indicator from toggling or chattering as the DSPLL completes lock acquisition. A block diagram of the LOL monitor is shown in the figure below. The live LOL register always displays the current LOL state and a sticky register always stays asserted until cleared. The LOL pin reflects the current state of the LOL monitor.

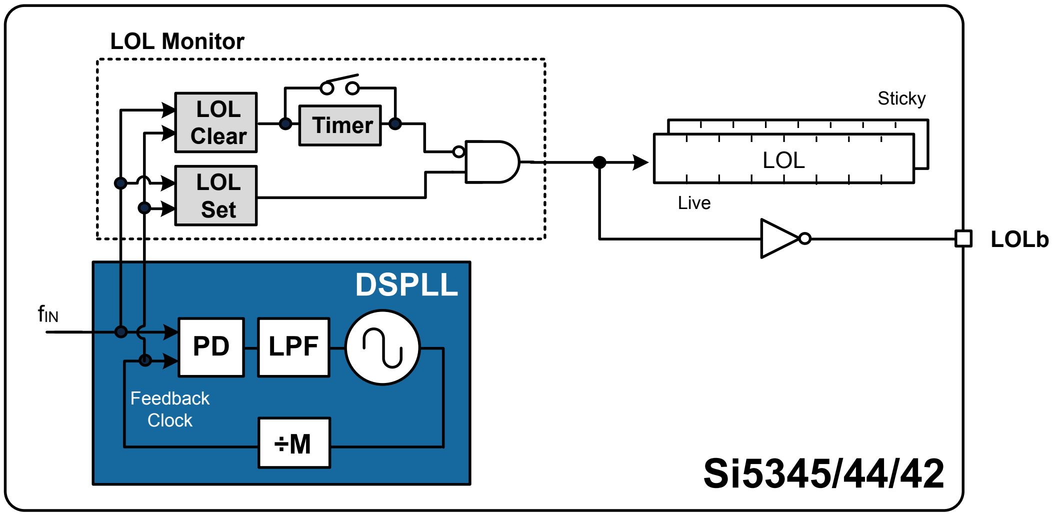


Figure 3.10. LOL Status Indicators

The LOL frequency monitors have an adjustable sensitivity which is register configurable from 0.1 ppm to 10,000 ppm. Having two separate frequency monitors allows for hysteresis to help prevent chattering of LOL status.

An example configuration where LOCK is indicated when there is less than 0.1 ppm frequency difference at the inputs of the phase detector and LOL is indicated when there's more than 1 ppm frequency difference is shown in the following figure.

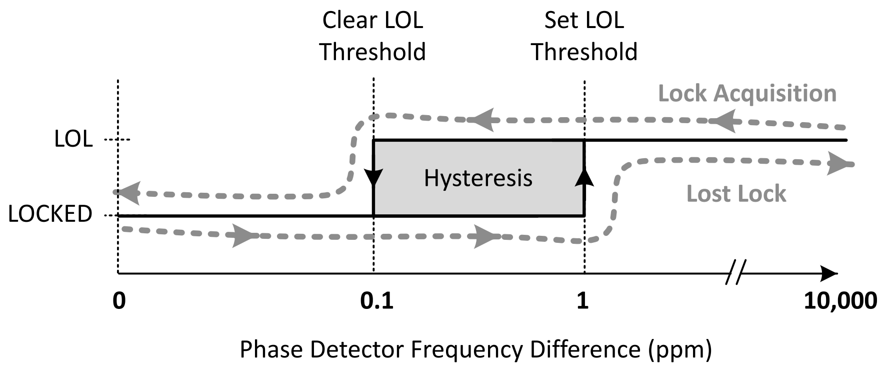


Figure 3.11. LOL Set and Clear Thresholds

Note: In this document, the terms, LVDS and LVPECL, refer to driver formats that are compatible with these signaling standards.

An optional timer is available to delay clearing of the LOL indicator to allow additional time for the DSPLL to completely lock to the input clock. The timer is also useful to prevent the LOL indicator from toggling or chattering as the DSPLL completes lock acquisition. The configurable delay value depends on frequency configuration and loop bandwidth of the DSPLL and is automatically calculated using the ClockBuilder Pro utility.

3.8.5 Interrupt Pin (INTRb)

An interrupt pin (INTRb) indicates a change in state of the status indicators (LOS, OOF, LOL, HOLD). Any of the status indicators are maskable to prevent assertion of the interrupt pin. The state of the INTRb pin is reset by clearing the status register that caused the interrupt.

3.9 Outputs

Each driver has a configurable voltage swing and common mode voltage covering a wide variety of differential signal formats. In addition to supporting differential signals, any of the outputs can be configured as single-ended LVCMOS (3.3 V, 2.5 V, or 1.8 V) providing up to 20 single-ended outputs, or any combination of differential and single-ended outputs.

3.9.1 Output Crosspoint

A crosspoint allows any of the output drivers to connect with any of the MultiSynths as shown in the figure below. The crosspoint configuration is programmable and can be stored in NVM so that the desired output configuration is ready at power up.

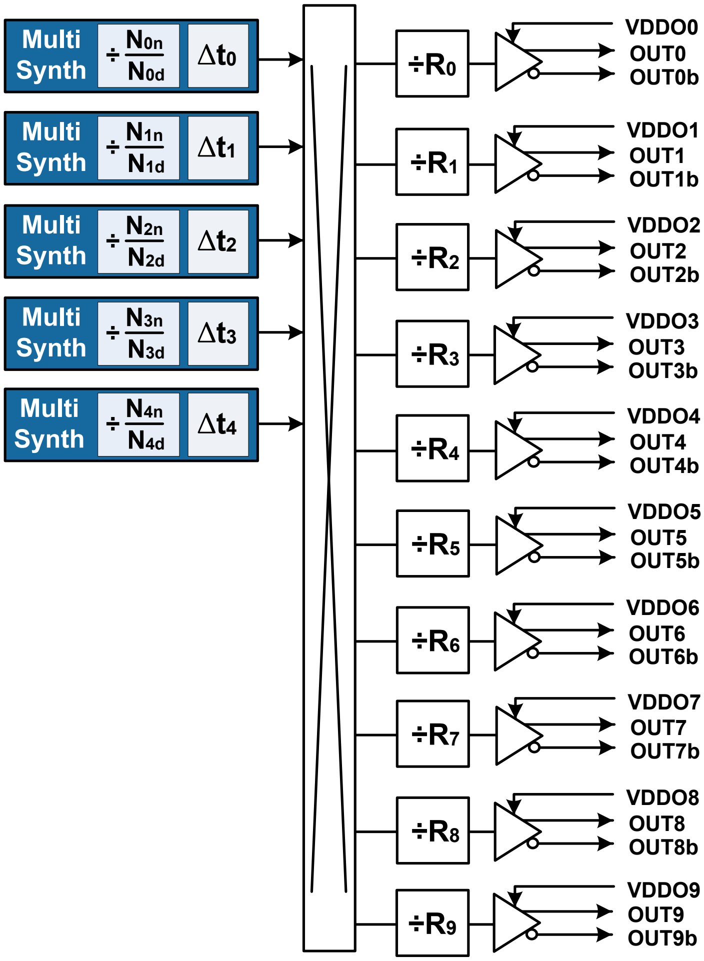


Figure 3.12. MultiSynth to Output Driver Crosspoint

3.9.2 Output Signal Format

The differential output swing and common mode voltage are both fully programmable covering a wide variety of signal formats including LVDS and LVPECL. In addition to supporting differential signals, any of the outputs can be configured as LVCMOS (3.3 V, 2.5 V, or 1.8 V) drivers providing up to 20 single-ended outputs, or any combination of differential and single-ended outputs.

3.9.3 Differential Output Terminations

The differential output drivers support both ac-coupled and dc-coupled terminations as shown in the figure below.

Note: In this document, the terms, LVDS and LVPECL, refer to driver formats that are compatible with these signaling standards.

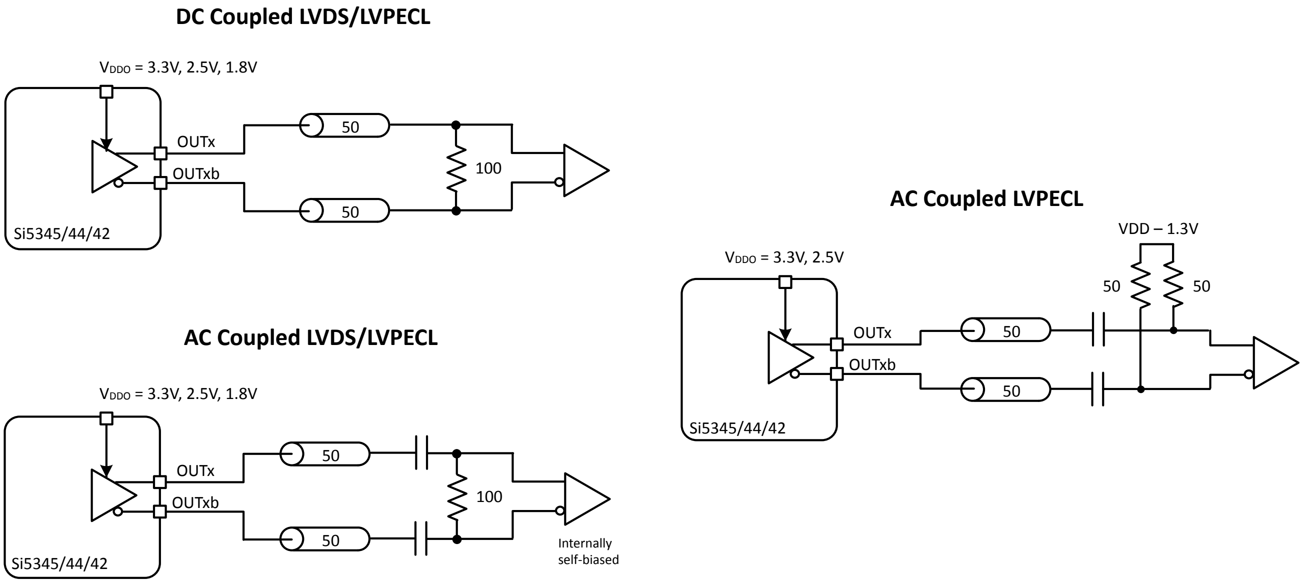


Figure 3.13. Supported Differential Output Terminations

3.9.4 LVCMOS Output Terminations

LVCMOS outputs are dc-coupled, as shown in the following figure.

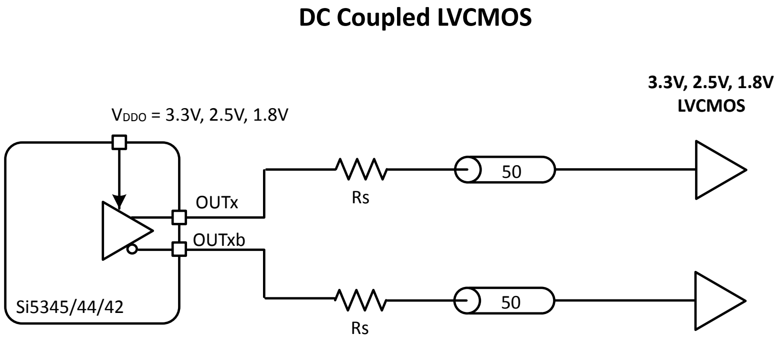


Figure 3.14. LVCMOS Output Terminations

3.9.5 Programmable Common Mode Voltage For Differential Outputs

The common mode voltage (V_{CM}) for the differential modes are programmable so that LVDS specifications can be met and for the best signal integrity with different supply voltages. When dc coupling the output driver, it is essential that the receiver have a relatively high common mode impedance so that the common mode current from the output driver is very small.

3.9.6 LVCMOS Output Impedance Selection

Each LVCMOS driver has a configurable output impedance to accommodate different trace impedances. A source termination resistor is recommended to help match the selected output impedance to the trace impedance, where Rs = Transmission line impedance – Z_O. There are three programmable output impedance selections (CMOS1, CMOS2, CMOS3) for each VDDO option as shown in the following table.

Table 3.2. Typical Output Impedance (Z_S)

VDDO	CMOS Drive Selections		
	OUTx_CMOS_DRV = 1	OUTx_CMOS_DRV = 2	OUTx_CMOS_DRV = 3
3.3 V	38 Ω	30 Ω	22 Ω
2.5 V	43 Ω	35 Ω	24 Ω
1.8 V	—	46 Ω	31 Ω

3.9.7 LVCMOS Output Signal Swing

The signal swing (V_{OL}/V_{OH}) of the LVCMOS output drivers is set by the voltage on the VDDO pins. Each output driver has its own VDDO pin allowing a unique output voltage swing for each of the LVCMOS drivers.

3.9.8 LVCMOS Output Polarity

When a driver is configured as an LVCMOS output, it generates a clock signal on both pins (OUTx and OUTxb). By default, the clock on the OUTx pin is generated with the same polarity (in phase) as the clock on the OUTxb pin. The polarity of these clocks is configurable, enabling complementary clock generation and/or inverted polarity with respect to other output drivers.

3.9.9 Output Enable/Disable

The OEb pin provides a convenient method of disabling or enabling the output drivers. When the OEb pin is held high, all outputs are disabled. When held low, the outputs are enabled. Outputs in the enabled state can be individually disabled through register control.

3.9.10 Output Driver State When Disabled

The disabled state of an output driver is configurable as disable low or disable high.

3.9.11 Synchronous Output Disable Feature

The output drivers provide a selectable synchronous disable feature. Output drivers with this feature turned on will wait until a clock period has completed before the driver is disabled. This prevents unwanted runt pulses from occurring when disabling an output. When this feature is turned off, the output clock will disable immediately without waiting for the period to complete.

3.9.12 Output Skew Control (Δt_0 – Δt_4)

The Si5345/44/42 uses independent MultiSynth dividers (N_0 – N_4) to generate up to five unique frequencies to its ten outputs through a crosspoint switch. By default, all clocks are phase-aligned. A delay path (Δt_0 – Δt_4) associated with each of these dividers is available for applications that need a specific output skew configuration. This is useful for PCB trace length mismatch compensation. The resolution of the phase adjustment is approximately 0.28 ps per step, definable in a range of ±9.14 ns. Phase adjustments are register-configurable. An example of generating two frequencies with unique configurable path delays is shown in the following figure.

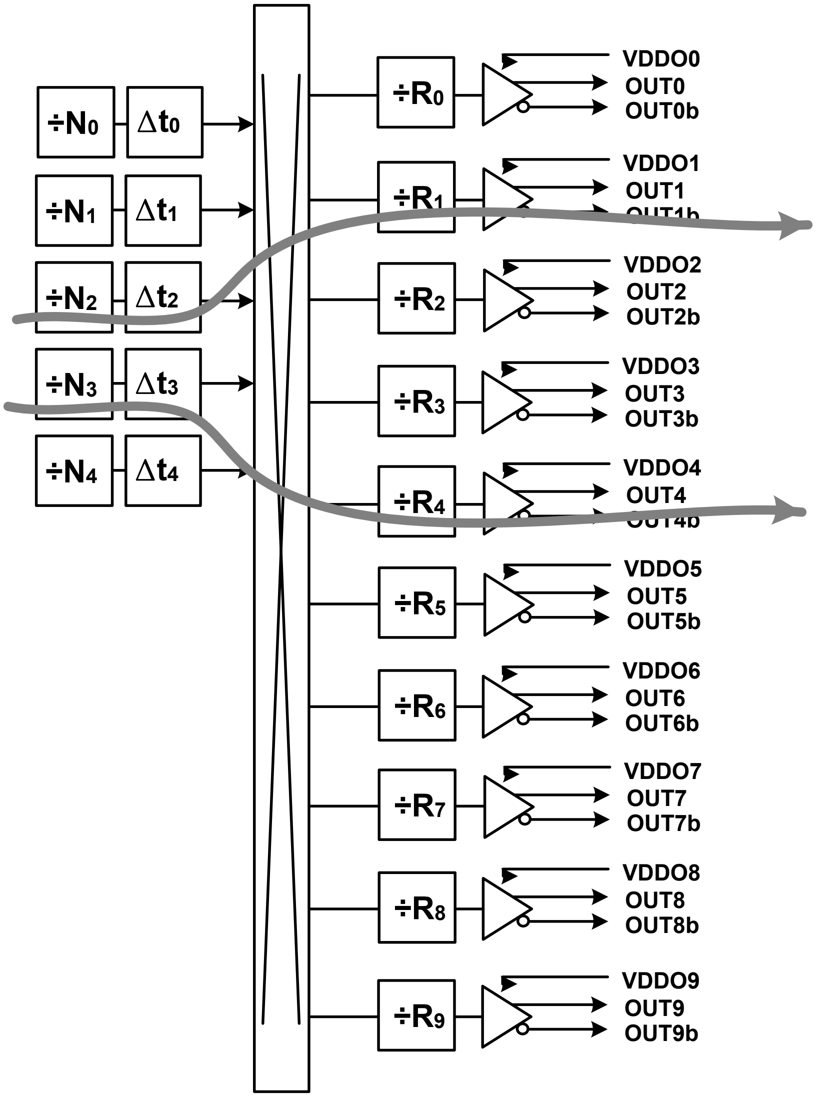


Figure 3.15. Example of Independently-Configurable Path Delays

All phase delay values are restored to their default values after power-up, hard reset, or a reset using the RSTb pin. Phase delay default values can be written to NVM, allowing a custom phase offset configuration at power-up or after power-on reset, or after a hardware reset using the RSTb pin.

3.9.13 Zero Delay Mode

A zero delay mode is available for applications that require fixed and consistent minimum delay between the selected input and outputs. The zero delay mode is configured by opening the internal feedback loop through software configuration and closing the loop externally as shown in the figure below.

This helps to cancel out the internal delay introduced by the dividers, the crosspoint, the input, and the output drivers. Any one of the outputs can be fed back to the FB_IN pins, although using the output driver that achieves the shortest trace length will help to minimize the input-to-output delay. The OUT9 and FB_IN pins are recommended for the external feedback connection. The FB_IN input pins must be terminated and ac-coupled when zero delay mode is used. A differential external feedback path connection is necessary for best performance. Note that the hitless switching feature is not available when zero delay mode is enabled.

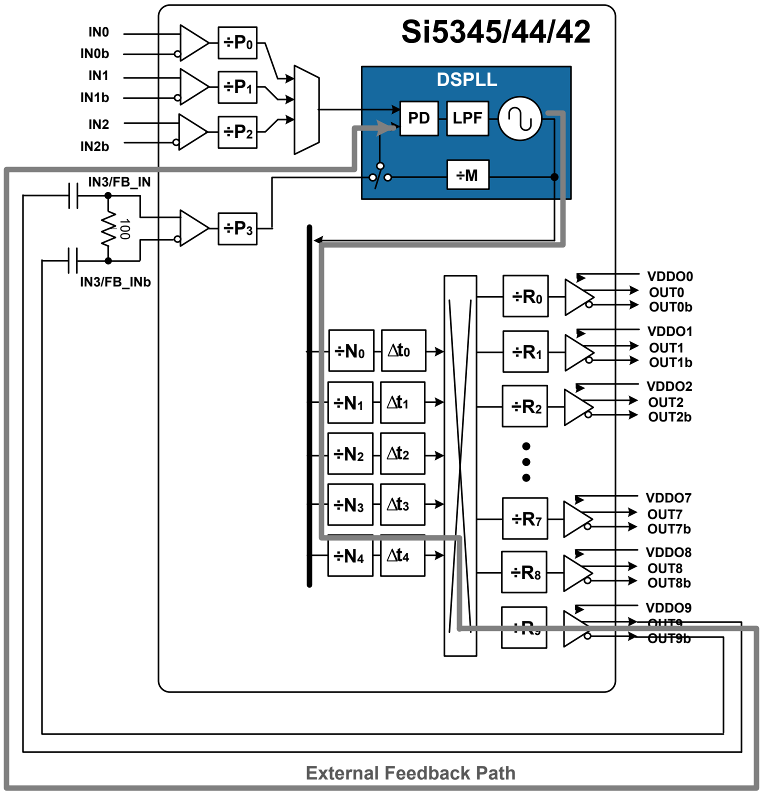


Figure 3.16. Si5345 Zero Delay Mode Setup

3.9.14 Output Divider (R) Synchronization

All the output R dividers are reset to a known state during the power-up initialization period. This ensures consistent and repeatable phase alignment across all output drivers. Resetting the device using the RSTb pin or asserting the hard reset bit will have the same result. Asserting the sync register bit provides another method of realigning the R dividers without resetting the device.

3.10 Power Management

Unused inputs and output drivers can be powered down when unused. Consult the Family Reference Manual and ClockBuilder Pro configuration utility for details.

3.11 In-Circuit Programming

The Si5345/44/42 is fully configurable using the serial interface (I^2C or SPI). At power-up the device downloads its default register values from internal non-volatile memory (NVM). Application specific default configurations can be written into NVM allowing the device to generate specific clock frequencies at power-up. Writing default values to NVM is in-circuit programmable with normal operating power supply voltages applied to its V_{DD} and V_{DDA} pins. The NVM is two time writable. Once a new configuration has been written to NVM, the old configuration is no longer accessible. Refer to the Family Reference Manual for a detailed procedure for writing registers to NVM.

3.12 Serial Interface

Configuration and operation of the Si5345/44/42 is controlled by reading and writing registers using the I^2C or SPI interface. The I2C_SEL pin selects I^2C or SPI operation. Communication with both 3.3 V and 1.8 V host is supported. The SPI mode operates in either 4-wire or 3-wire. See the Family Reference Manual for details.

3.13 Custom Factory Preprogrammed Parts

For applications where a serial interface is not available for programming the device, custom pre-programmed parts can be ordered with a specific configuration written into NVM. A factory preprogrammed part will generate clocks at power-up. Custom, factory-preprogrammed devices are available. The ClockBuilder Pro custom part number wizard can be used to quickly and easily generate a custom part number for your configuration.

In less than three minutes, you will be able to generate a custom part number with a detailed data sheet addendum matching your design’s configuration. Once you receive the confirmation email with the data sheet addendum, simply place an order with your local Silicon Labs sales representative. Samples of your preprogrammed device will typically ship in about two weeks.

3.14 Enabling Features and/or Configuration Settings Unavailable in ClockBuilder Pro for Factory Preprogrammed Devices

As with essentially all modern software utilities, ClockBuilder Pro is continually being updated and enhanced. By registering at www.silabs.com, you will be notified about changes and their impact. This update process will ultimately enable ClockBuilder Pro users to access all features and register setting values documented in this data sheet and the Family Reference Manual.

However, if you must enable or access a feature or register setting value so that the device starts up with this feature or a register setting, but the feature or register setting is not yet available in CBPro, you must contact a Silicon Labs applications engineer for assistance. One example of this type of feature or custom setting is the customizable output amplitude and common voltages for the clock outputs. After careful review of your project file and requirements, the Silicon Labs applications engineer will email back your CBPro project file with your specific features and register settings enabled using what's referred to as the manual "settings override" feature of CBPro. "Override" settings to match your request(s) will be listed in your design report file. Examples of setting "overrides" in a CBPro design report are shown in the following table.

Table 3.3. Setting Overrides

Location	Name	Type	Target	Dec Value	Hex Value
0x04535[0]	FORCE_HOLD	No NVM	N/A	1	0x1
0x0B48[0:4]	OOF_DIV_CLK_DIS	User	OPN&EVB	0	0x00

Once you receive the updated design file, simply open it in CBPro. The device will begin operation after startup with the values in the NVM file. The flowchart for this process is shown in the following figure.

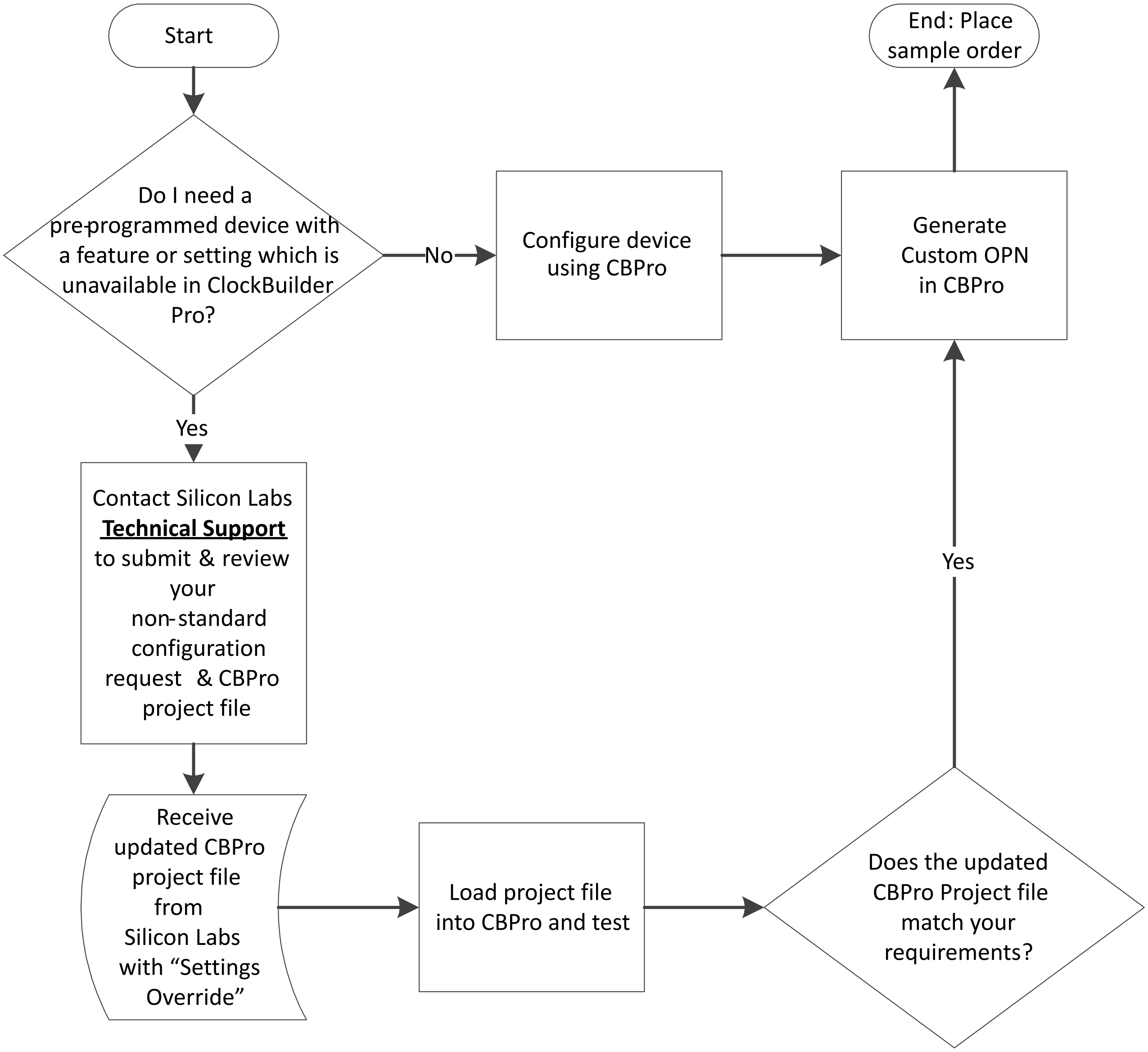


Figure 3.17. Process for Requesting Non-Standard CBPro Features

Note: Contact Silicon Labs Technical Support at www.silabs.com/support/Pages/default.aspx.

4. Register Map

The register map is divided into multiple pages where each page has 256 addressable registers. Page 0 contains frequently accessible registers, such as alarm status, resets, device identification, etc. Other pages contain registers that need less frequent access such as frequency configuration, and general device settings. A high level map of the registers is shown in “6.2. High-Level Register Map” . Refer to the Family Reference Manual for a complete list of register descriptions and settings. Silicon Labs strongly recommends using ClockBuilder Pro to create and manage register settings.

4.1 Addressing Scheme

The device registers are accessible using a 16-bit address that consists of an 8-bit page address plus an 8-bit register address. By default, the page address is set to 0x00. Changing to another page is accomplished by writing to the "Set Page Address" byte located at address 0x01 of each page.

4.2 High-Level Register Map

Table 4.1. High-Level Register Map

16-Bit Address		Content
8-bit Page Address	8-bit Register Address Range	
00	00	Revision IDs
	01	Set Page Address
	02–0A	Device IDs
	0B–15	Alarm Status
	17–1B	INTR Masks
	1C	Reset controls
	1D	FINC, FDEC Control Bits
	2B	SPI (3-Wire vs 4-Wire)
	2C–E1	Alarm Configuration
	E2–E4	NVM Controls
	FE	Device Ready Status
01	01	Set Page Address
	08–3A	Output Driver Controls
	41–42	Output Driver Disable Masks
	FE	Device Ready Status
02	01	Set Page Address
	02–05	XTAL Frequency Adjust
	08–2F	Input Divider (P) Settings
	30	Input Divider (P) Update Bits
	47–6A	Output Divider (R) Settings
	6B–72	User Scratch Pad Memory
	FE	Device Ready Status

16-Bit Address		Content
8-bit Page Address	8-bit Register Address Range	
03	01	Set Page Address
	02–37	MultiSynth Divider (N0–N4) Settings
	0C	MultiSynth Divider (N0) Update Bit
	17	MultiSynth Divider (N1) Update Bit
	22	MultiSynth Divider (N2) Update Bit
	2D	MultiSynth Divider (N3) Update Bit
	38	MultiSynth Divider (N4) Update Bit
	39–58	FINC/FDEC Settings N0–N4
	59–62	Output Delay (Δt) Settings
	FE	Device Ready Status
04	87	Zero Delay Mode Set Up
05	0E–14	Fast Lock Loop Bandwidth
	15–1F	Feedback Divider (M) Settings
	2A	Input Select Control
	2B	Fast Lock Control
	2C–35	Holdover Settings
	36	Input Clock Switching Mode Select
	38–39	Input Priority Settings
	3F	Holdover History Valid Data
06–08	00–FF	Reserved
09	01	Set Page Address
	1C	Zero Delay Mode Settings
	43	Control I/O Voltage Select
	49	Input Settings
10–FF	00–FF	Reserved

5. Electrical Specifications

Table 5.1. Recommended Operating Conditions[1]

V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, T_A = –40 to 85 °C

Parameter	Symbol	Min	Typ	Max	Unit
Ambient Temperature	T_A	–40	25	85	°C
Junction Temperature	TJ_{MAX}	—	—	125	°C
Core Supply Voltage	V_{DD}	1.71	1.80	1.89	V
	V_{DDA}	3.14	3.30	3.47	V
Clock Output Driver Supply Voltage	V_{DDO}	3.14	3.30	3.47	V
		2.37	2.50	2.62	V
		1.71	1.80	1.89	V
Status Pin Supply Voltage	V_{DDS}	3.14	3.30	3.47	V
		1.71	1.80	1.89	V

Note:

1. All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 °C unless otherwise noted.

Table 5.2. DC Characteristics

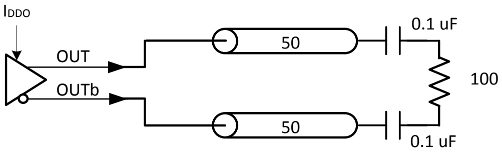
V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = –40 to 85 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Core Supply Current[1, 2, 3]	I_{DD}		—	135	260	mA
	I_{DDA}		—	120	130	mA
Output Buffer Supply Current	I_{DDOx}	LVPECL Output[4] @ 156.25 MHz	—	22	26	mA
		LVDS Output[4] @ 156.25 MHz	—	15	18	mA
		3.3 V LVCMOS Output[5] @ 156.25 MHz	—	22	30	mA
		2.5 V LVCMOS Output[5] @ 156.25 MHz	—	18	23	mA
		1.8 V LVCMOS Output[5] @ 156.25 MHz	—	12	16	mA
Total Power Dissipation[6]	P_d	Si5345[1]	—	900	1200	mW
		Si5344[2]	—	730	1000	mW
		Si5342[3]	—	670	950	mW

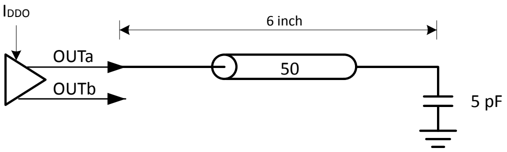
Notes:

1. Si5345 test configuration: 7 x 2.5 V LVDS outputs enabled at 156.25 MHz. Excludes power in termination resistors.
2. Si5344 test configuration: 4 x 2.5 V LVDS outputs enabled at 156.25 MHz. Excludes power in termination resistors.
3. Si5342 test configuration: 2 x 2.5 V LVDS outputs enabled at 156.25 MHz. Excludes power in termination resistors.
4. Differential outputs terminated into an AC-coupled 100 Ω load.
5. LVCMOS outputs measured into a 6 inch 50 Ω PCB trace with 5 pF load. Measurements were made in CMOS3 mode.

Differential Output Test Configuration



LVCMOS Output Test Configuration



6. Detailed power consumption for any configuration can be estimated using ClockBuilder Pro when an evaluation board (EVB) is not available. All EVBs support detailed current measurements for any configuration.

Table 5.3. Input Clock Specifications

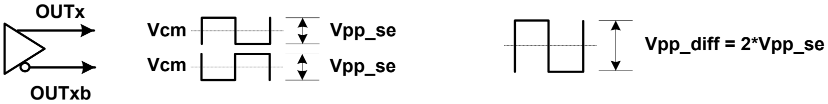
V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, T_A = –40 to 85 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Standard Input Buffer with Differential or Single-Ended - AC Coupled (IN0/IN0, IN1/IN1, IN2/IN2, IN3/IN3, FB_IN/FB_IN)						
Input Frequency Range	f_{IN}	Differential	0.008	—	750	MHz
		All Single-ended signals (including LVCMOS)	0.008	—	250	MHz
Voltage Swing[1]	V_{IN}	Differential AC-coupled f_{IN} < 250 MHz	100	—	1800	mVpp_se
		Differential AC-coupled 250 MHz < f_{IN} < 750 MHz	225	—	1800	mVpp_se
		Single-ended AC-coupled f_{IN} < 250 MHz	100	—	3600	mVpp_se
Slew Rate[2, 3]	SR		400	—	—	V/µs
Duty Cycle	DC		40	—	60	%
Input Capacitance	C_{IN}		—	0.3	—	pF
Input Resistance	R_{IN}		—	16	—	kΩ
Pulsed CMOS Input Buffer—DC Coupled (IN0, IN1, IN2, IN4)[3]						
Input Frequency	$f_{IN\_PULSED\_CMOS}$		0.008	—	250	MHz
Input Voltage	V_{IL}		–0.2	—	0.4	V
	V_{IH}		0.8	—	—	V
Slew Rate[2, 3]	SR		400	—	—	V/µs
Duty Cycle	DC		40	—	60	%
Minimum Pulse Width	PW	Pulse Input	1.6	—	—	ns
Input Resistance	R_{IN}		—	8	—	kΩ
REFCLK (Applied to XA/XB)						
REFCLK Frequency	f_{IN_REF}	Full operating range. Jitter performance may be reduced.	24.97	—	54.06	MHz
		Range for best jitter.	48	—	54	MHz
		TCXO frequency for SyncE applications. Jitter performance may be reduced.	—	40	—	MHz
Input Single-ended Voltage Swing	V_{IN_SE}		365	—	2000	mVpp_se
Input Differential Voltage Swing	V_{IN_DIFF}		365		2500	mVpp_diff
Slew Rate[2, 3]	SR		400	—	—	V/µs

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Duty Cycle	DC		40	—	60	%

Note:

1. Voltage swing is specified as single-ended mVpp.



2. Imposed for jitter performance.
3. Rise and fall times can be estimated using the following simplified equation: tr/tf$_{80-20}$ = ((0.8 – 0.2) x $V_{IN\_Vpp\_se}$) / SR. Pulsed CMOS mode is intended primarily for single-ended LVCMOS input clocks ≤ 1 MHz that must be dc-coupled because they have a duty cycle significantly less than 50%. A typical application example is a low-frequency video frame sync pulse. Since the input thresholds (V_{IL}, V_{IH}) of this buffer are non-standard (0.4 and 0.8 V, respectively) refer to the input attenuator circuit for dc-coupled pulsed LVCMOS in the Family Reference Manual. Otherwise, for standard LVCMOS input clocks, use the Standard Differential or Single-Ended ac-coupled input mode.

Table 5.4. Control Input Pin Specifications

V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, V_{DDS} = 3.3 V ±5%, 1.8 V ±5%, T_A = –40 to 85 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Si5345 Control Input Pins (I2C_SEL, IN_SEL[1:0], RSTb, OEb, A1, SCLK, A0/CSb, FINC, FDEC, SDA/SDIO)						
Input Voltage	V_{IL}		—	—	0.3 × V_{DDIO}[1]	V
	V_{IH}		0.7 × V_{DDIO}[1]	—	—	V
Input Capacitance	C_{IN}		—	2	—	pF
Input Resistance	R_{IN}		—	20	—	kΩ
Minimum Pulse Width	PW	RSTb, FINC and FDEC	100	—	—	ns
Update Rate	T_{UR}	FINC and FDEC	1	—	—	µs
Si5344/42 Control Input Pins (I2C_SEL, IN_SEL[1:0], RSTb, OEb, A1, SCLK, A0/CSb, SDA/SDIO)						
Input Voltage	V_{IL}		—	—	0.3 × V_{DDIO}[1]	V
	V_{IH}		0.7 × V_{DDIO}[1]	—	—	V
Input Capacitance	C_{IN}		—	2	—	pF
Input Resistance	R_{IN}		—	20	—	kΩ
Minimum Pulse Width	PW	RSTb	100	—	—	ns

Note:

1. V_{DDIO} is determined by the IO_VDD_SEL bit. It is selectable as V_{DDA} or V_{DD}. See the Family Reference Manual for more details on the proper register settings.

Table 5.5. Differential Clock Output Specifications

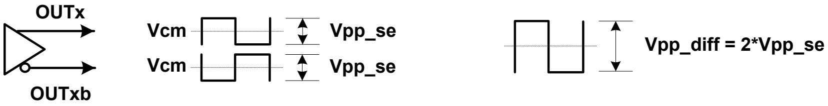
V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = –40 to 85 °C

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
Si5342/44/45							
Output Frequency	f_{OUT}	MultiSynth not used		0.0001	—	720	MHz
				733.33	—	800.00	MHz
				825	—	1028	MHz
		MultiSynth used		0.0001	—	720	MHz
Duty Cycle	DC	f_{OUT} < 400 MHz		48	—	52	%
		400 MHz < f_{OUT} < 1028 MHz		45	—	55	%
Output-Output Skew Using Same MultiSynth	T_{SKS}	Outputs on same MultiSynth (Measured at 712.5 MHz)		—	—	65	ps
Output-Output Skew Between MultiSynths	T_{SKD}	Outputs from different MultiSynths (Measured at 712.5 MHz)		—	—	90	ps
OUT-OUTb Skew	TSK_OUT	Measured from the positive to negative output pins		—	0	50	ps
Output Voltage Swing[1]	VOUT	V_{DDO} = 3.3 V, 2.5 V, 1.8 V	LVDS	350	430	510	mVpp_se
		V_{DDO} = 3.3 V, 2.5 V	LVPECL	640	750	900	mVpp_se
Common Mode Voltage[1, 2] (100 Ω load line-to-line)	VCM	V_{DDO} = 3.3 V	LVDS	1.10	1.2	1.3	V
			LVPECL	1.90	2.0	2.1	V
		V_{DDO} = 2.5 V	LVPECL LVDS	1.1	1.2	1.3	V
		V_{DDO} = 1.8 V	sub-LVDS	0.8	0.9	1.0	V
Rise and Fall Times (20% to 80%)	tR/tF			—	100	150	ps
Differential Output Impedance	ZO			—	100	—	Ω
Power Supply Noise Rejection[2]	PSRR	10 kHz sinusoidal noise		—	–101	—	dBc
		100 kHz sinusoidal noise		—	–96	—	dBc
		500 kHz sinusoidal noise		—	–99	—	dBc
		1 MHz sinusoidal noise		—	–97	—	dBc
Output-output Crosstalk[3]	XTALK	Si5345		—	–72	—	dBc
		Si5342/44		—	–88	—	dBc

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit

Notes:

1. Output amplitude and common-mode settings are programmable through register settings and can be stored in NVM. Each output driver can be programmed independently. Note that the maximum LVDS single-ended amplitude can be up to 110 mV higher than the TIA/EIA-644 maximum. Refer to the Si5345/44/42 Family Reference Manual for more suggested output settings. Not all combinations of voltage amplitude and common mode voltages settings are possible.



2. Measured for 156.25 MHz carrier frequency. 100 mVpp sinewave noise added to VDDO = 3.3 V and noise spur amplitude measured.
3. Measured across two adjacent outputs, both in LVDS mode, with the victim running at 155.52 MHz and the aggressor at 156.25 MHz. Refer to “AN862: Optimizing Si534x Jitter Performance in Next Generation Internet Infrastructure Systems” for guidance on crosstalk optimization. Note that all active outputs must be terminated when measuring crosstalk.

Table 5.6. LVCMOS Clock Output Specifications

V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = –40 to 85 °C

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
Output Frequency	f_{OUT}			0.0001	—	250	MHz
Duty Cycle	DC	f_{OUT} <100 MHz		48	—	52	%
		100 MHz < f_{OUT} < 250 MHz		45	—	55	%
Output-to-Output Skew	T_{SK}	When outputs are on same MultSynth. F_{OUT} = 156.25 MHz		—	30	140	ps
Output Voltage High[1, 2, 3]	V_{OH}	V_{DDO} = 3.3 V					
		OUTx_CMOS_DRV = 1	I_{OH} = –10 mA	V_{DDO} x 0.85	—	—	V
		OUTx_CMOS_DRV = 2	I_{OH} = –12 mA	V_{DDO} x 0.85	—	—	V
		OUTx_CMOS_DRV = 3	I_{OH} = –17 mA	V_{DDO} x 0.85	—	—	V
		V_{DDO} = 2.5 V					
		OUTx_CMOS_DRV = 1	I_{OH} = –6 mA	V_{DDO} x 0.85	—	—	V
		OUTx_CMOS_DRV = 2	I_{OH} = –8 mA	V_{DDO} x 0.85	—	—	V
		OUTx_CMOS_DRV = 3	I_{OH} = –11 mA	V_{DDO} x 0.85	—	—	V
		V_{DDO} = 1.8 V					
		OUTx_CMOS_DRV = 2	I_{OH} = –4 mA	V_{DDO} x 0.85	—	—	V
		OUTx_CMOS_DRV = 3	I_{OH} = –5 mA	V_{DDO} x 0.85	—	—	V
Output Voltage Low[1, 2, 3]	V_{OL}	V_{DDO} = 3.3 V					
		OUTx_CMOS_DRV = 1	I_{OL} = 10 mA	—	—	V_{DDO} x 0.15	V
		OUTx_CMOS_DRV = 2	I_{OL} = 12 mA	—	—	V_{DDO} x 0.15	V
		OUTx_CMOS_DRV = 3	I_{OL} = 17 mA	—	—	V_{DDO} x 0.15	V
		V_{DDO} = 2.5 V					
		OUTx_CMOS_DRV = 1	I_{OL} = 6 mA	—	—	V_{DDO} x 0.15	V
		OUTx_CMOS_DRV = 2	I_{OL} = 8 mA	—	—	V_{DDO} x 0.15	V
		OUTx_CMOS_DRV = 3	I_{OL} = 11 mA	—	—	V_{DDO} x 0.15	V
		V_{DDO} = 1.8 V					
		OUTx_CMOS_DRV = 2	I_{OL} = 4 mA	—	—	V_{DDO} x 0.15	V
		OUTx_CMOS_DRV = 3	I_{OL} = 5 mA	—	—	V_{DDO} x 0.15	V
LVCMOS Rise and Fall Times[3] (20% to 80%)	tr/tf	V_{DDO} = 3.3V		—	400	600	ps
		V_{DDO} = 2.5 V		—	450	600	ps
		V_{DDO} = 1.8 V		—	550	750	ps

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit

Note:

1. Driver strength is a register programmable setting and stored in NVM. Options are OUTx_CMOS_DRV = 1, 2, 3. Refer to the Family Reference Manual for more details on register settings.
2. I_{OL}/I_{OH} is measured at V_{OL}/V_{OH} as shown in the dc test configuration.
3. A series termination resistor (Rs) is recommended to help match the source impedance to a 50 Ω PCB trace. A 5 pF capacitive load is assumed. The LVCMOS outputs were set to OUTx_CMOS_DRV = 3, at 156.25 MHz.

AC Test Configuration

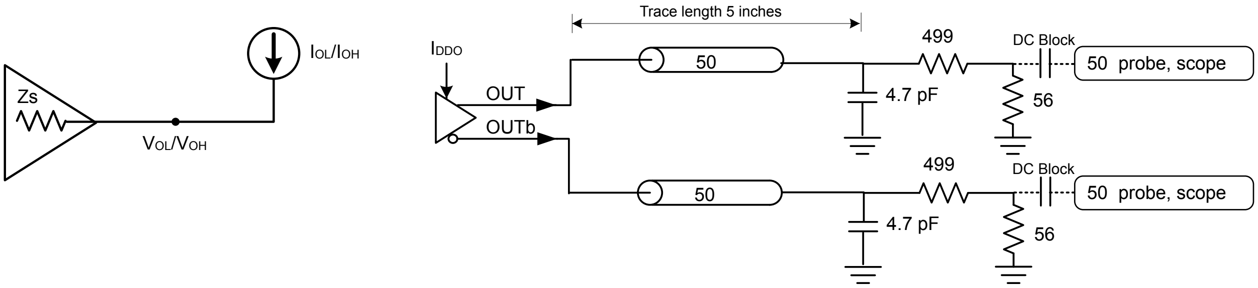


Table 5.7. Output Status Pin Specifications

V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, V_{DDS} = 3.3 V ±5%, 1.8 V ±5%, T_A = –40 to 85 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Si5345 Status Output Pins (LOLb, INTRb, SDA/SDIO[1], SDO)						
Output Voltage	V_{OH}	I_{OH} = –2 mA	V_{DDIO}[2] x 0.85	—	—	V
	V_{OL}	I_{OL} = 2 mA	—	—	V_{DDIO}[2] x 0.15	V
Si5344/42 Status Output Pins (INTRb, SDA/SDIO1[1], SDO)						
Output Voltage	V_{OH}	I_{OH} = –2 mA	V_{DDIO}[2] x 0.85	—	—	V
	V_{OL}	I_{OL} = 2 mA	—	—	V_{DDIO}[2] x 0.15	V
Si5344 Status Output Pins (LOLb, LOS_XAXBb) **Si5342 Status Output Pins (LOLb, LOS_XAXBb, LOS0b, LOS1b, LOS2b, LOS3b)**						
Output Voltage	V_{OH}	I_{OH} = –2 mA	V_{DDS} x 0.85	—	—	V
	V_{OL}	I_{OL} = 2 mA	—	—	V_{DDS} x 0.15	V

Notes:

1. The V_{OH} specification does not apply to the open-drain SDA/SDIO output when the serial interface is in I^2C mode or is unused with I2C_SEL pulled high. VOL remains valid in all cases.
2. V_{DDIO} is determined by the IO_VDD_SEL bit. It is selectable as V_{DDA} or V_{DD}. See the Family Reference Manual for more details on the proper register settings.

Table 5.8. Performance Characteristics

V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, T_A = –40 to 85 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
VCO Frequency Range	F_{VCO}		13.5	—	14.4	GHz
PLL Loop Bandwidth Programming Range[1]	f_{BW}		0.1	—	4000	Hz
Initial Start-Up Time	t_{START}	Time from power-up to when the device generates free-running clocks	—	30	45	ms
PLL Lock Time[2]	t_{ACQ}	f_{IN} = 19.44 MHz	—	280	300	ms
Output Delay Adjustment	t_{DELAY_frac}	f_{VCO} = 14 GHz	—	0.28	—	ps
	t_{DELAY_int}		—	71.4	—	ps
	t_{RANGE}		—	±9.14	—	ns
POR to Serial Interface Ready[3]	t_{RDY}		—	—	15	ms
Jitter Peaking	J_{PK}	Measured with a frequency plan running a 25 MHz input, 25 MHz output, and a Loop Bandwidth of 4 Hz	—	—	0.1	dB
Jitter Tolerance	J_{TOL}	Compliant with G.8262 Options 1 and 2 Carrier Frequency = 10.3125 GHz Jitter Modulation Frequency = 10 Hz	—	3180	—	UI pk-pk
Maximum Phase Transient During a Hitless Switch	t_{SWITCH}	Only valid for a single automatic switch between two input clocks at same frequency.	—	—	2.0	ns
		Only valid for a single manual switch between two input clocks at same frequency.	—	—	1.3	ns
Pull-in Range	ω_P		—	500	—	ppm

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input-to-Output Delay Variation	$t_{IODELAY}$	Measured between a common 2 MHz input and 2 MHz output with different MultiSynths on the same unit. DSPLL BW = 4 kHz	—	—	1.8	ns
		Measured between a common 2 MHz input and 2 MHz output with different MultiSynths between units. DSPLL bandwidth = 4 kHz	—	—	2.0	ns
	t_{ZDELAY}	Delay between reference and feedback input with both clocks at 10 MHz and same slew rate. Ref clock rise time must be <200 ps.	—	110	—	ps
RMS Phase Jitter[4]	J_{GEN}	Integer Mode 12 kHz to 20 MHz	—	90	145	fs rms
		Fractional Mode 12 kHz to 20 MHz	—	120	170	fs rms

Note:

1. Actual loop bandwidth might be lower; please refer to CBPro for actual value for your frequency plan.
2. Lock Time can vary significantly depending on several parameters, such as bandwidths, LOL tresholds, etc. For this case, lock time was measured with nominal and fastlock bandwidths set to 100 Hz, LOL set/clear thresholds of 6/0.6 ppm respectively, using IN0 as clock reference by removing the reference and enabling it again, then measuring the delta time between the first rising edge of the clock reference and the LOL indicator deassertion.
3. Measured as time from valid VDD/VDDA rails (90% of their value) to when the serial interface is ready to respond to commands.
4. Jitter generation test conditions: f_{IN} = 19.44 MHz, f_{OUT} = 156.25 MHz LVPECL, loop bandwidth = 100 Hz, F_{XTAL} = 48 MHz.

Table 5.9. I^2C Timing Specifications (SCL,SDA)

Parameter	Symbol	Test Condition	Standard Mode 100 kbps		Fast Mode 400 kbps		Unit
			Min	Max	Min	Max	
SCL Clock Frequency	f_{SCL}		—	100	—	400	kHz
SMBus Timeout	—	When Timeout is Enabled	25	35	25	35	ms
Hold time (Repeated) START condition	$t_{HD:STA}$		4.0	—	0.6	—	µs
Low Period of the SCL Clock	t_{LOW}		4.7	—	1.3	—	µs
HIGH Period of the SCL Clock	t_{HIGH}		4.0	—	0.6	—	µs
Setup Time for a Repeated START Condition	$t_{SU:STA}$		4.7	—	0.6	—	µs

Parameter	Symbol	Test Condition	Standard Mode 100 kbps		Fast Mode 400 kbps		Unit
			Min	Max	Min	Max	
Data Hold Time	$t_{HD:DAT}$		100	—	100	—	ns
Data Setup Time	$t_{SU:DAT}$		250	—	100	—	ns
Rise Time of both SDA and SCL Signals	t_r		—	1000	20	300	ns
Fall Time of both SDA and SCL Signals	t_f		—	300	—	300	ns
Setup Time for STOP Condition	$t_{SU:STO}$		4.0	—	0.6	—	µs
Bus Free Time between a STOP and START Condition	t_{BUF}		4.7	—	1.3	—	µs
Data Valid Time	$t_{VD:DAT}$		—	3.45	—	0.9	µs
Data Valid Acknowledge Time	$t_{VD:ACK}$		—	3.45	—	0.9	µs

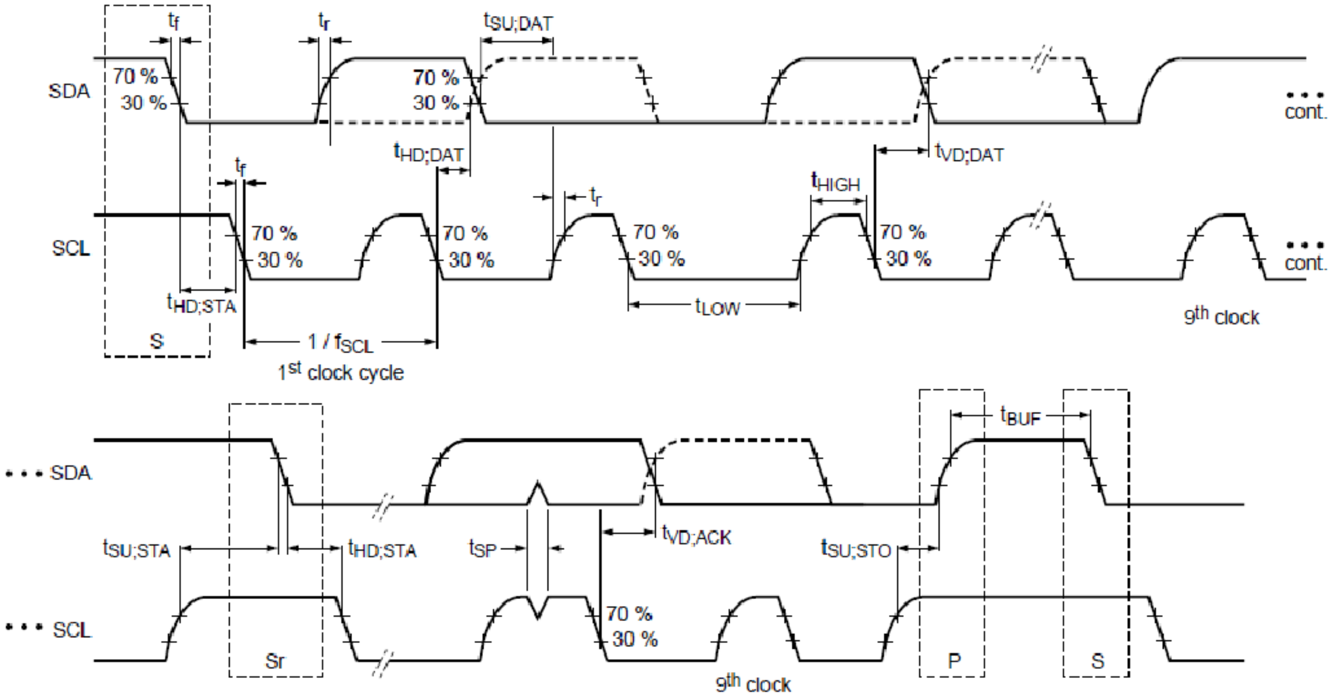


Figure 5.1. I^{2}C Serial Port Timing Standard and Fast Modes

Table 5.10. SPI Timing Specifications (4-Wire)

V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3V ±5%, T_A = –40 to 85 °C

Parameter	Symbol	Min	Typ	Max	Unit
SCLK Frequency	f_{SPI}	—	—	20	MHz
SCLK Duty Cycle	T_{DC}	40	—	60	%
SCLK Period	T_C	50	—	—	ns
Delay Time, SCLK Fall to SDO Active	T_{D1}	—	12.5	18	ns
Delay Time, SCLK Fall to SDO	T_{D2}	—	10	15	ns
Delay Time, CSb Rise to SDO Tri-State	T_{D3}	—	10	15	ns
Setup Time, CSb to SCLK	T_{SU1}	5	—	—	ns
Hold Time, SCLK Fall to CSb	T_{H1}	5	—	—	ns
Setup Time, SDI to SCLK Rise	T_{SU2}	5	—	—	ns
Hold Time, SDI to SCLK Rise	T_{H2}	5	—	—	ns
Delay Time Between Chip Selects (CSb)	T_{CS}	2	—	—	T_C

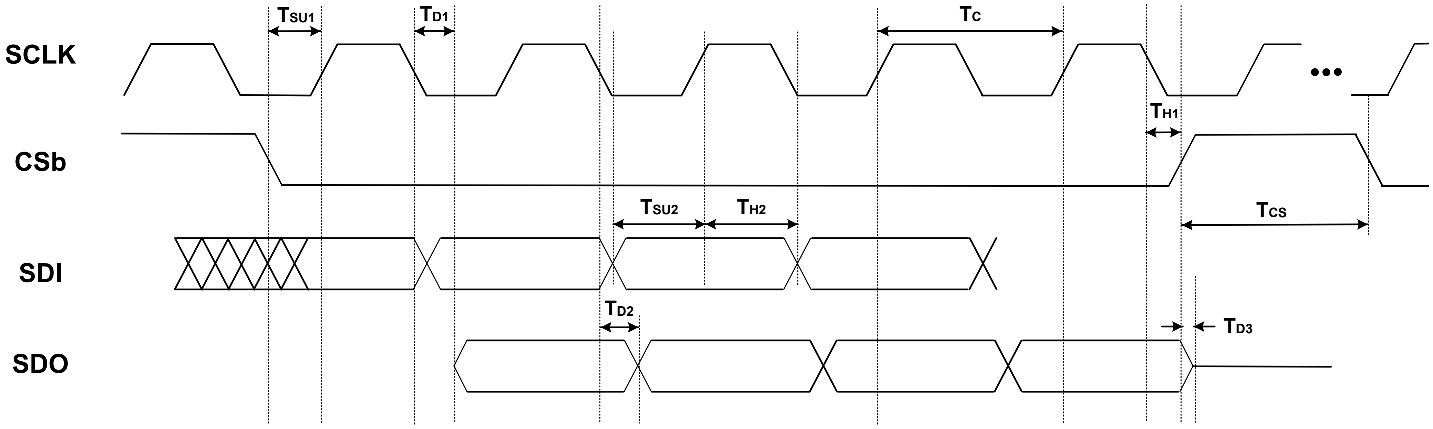


Figure 5.2. 4-Wire SPI Serial Interface Timing

Table 5.11. SPI Timing Specifications (3-Wire)

V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3V ±5%, T_A = –40 to 85 °C

Parameter	Symbol	Min	Typ	Max	Unit
SCLK Frequency	f_{SPI}	—	—	20	MHz
SCLK Duty Cycle	T_{DC}	40	—	60	%
SCLK Period	T_C	50	—	—	ns
Delay Time, SCLK Fall to SDIO Turn-on	T_{D1}	—	12.5	20	ns
Delay Time, SCLK Fall to SDIO Next-bit	T_{D2}	—	10	15	ns
Delay Time, CSb Rise to SDIO Tri-State	T_{D3}	—	10	15	ns
Setup Time, CSb to SCLK	T_{SU1}	5	—	—	ns
Hold Time, CSb to SCLK Fall	T_{H1}	5	—	—	ns
Setup Time, SDI to SCLK Rise	T_{SU2}	5	—	—	ns
Hold Time, SDI to SCLK Rise	T_{H2}	5	—	—	ns
Delay Time Between Chip Selects (CSb)	T_{CS}	2	—	—	T_C

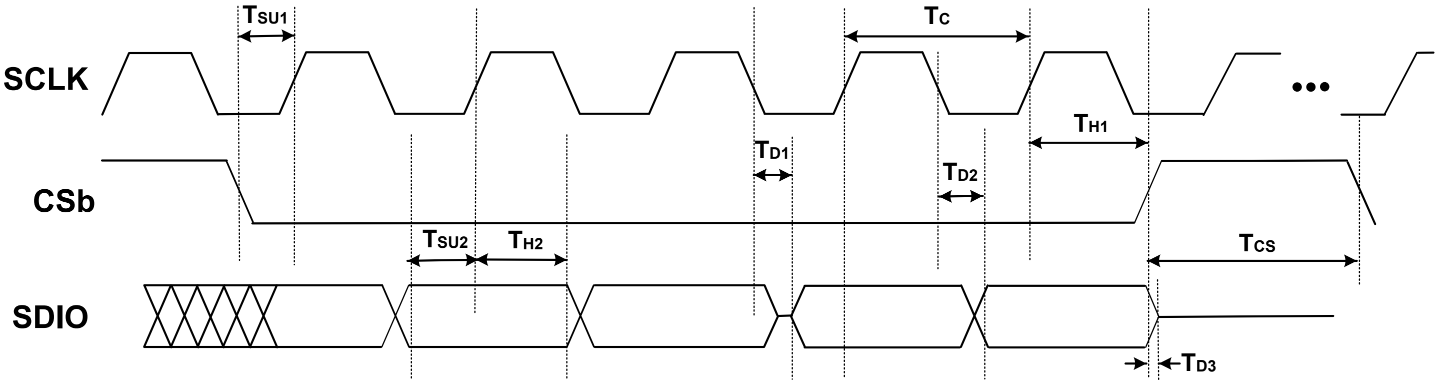


Figure 5.3. 3-Wire SPI Serial Interface Timing

Table 5.12. Crystal Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal Frequency Range	f_{XTAL}	Full operating range. Jitter performance may be reduced.	24.97	—	54.06	MHz
		Range for best jitter.	48	—	54	MHz
Load Capacitance	C_L		—	8	—	pF
Crystal Drive Level	d_L		—	—	200	μW
Equivalent Series Resistance Shunt Capacitance	r_{ESR} C_O	Refer to the Si5345/44/42 Reference Manual to determine ESR and shunt capacitance.				

Note:

1. Refer to the Si5345/44/42 Reference Manual for recommended 48 to 54 MHz crystals. The Si5345/44/42 are designed to work with crystals that meet these specifications.

Table 5.13. Thermal Characteristics

Parameter	Symbol	Test Condition [1]	Value	Unit
Si5345-64QFN				
Thermal Resistance Junction to Ambient	θ_{JA}	Still Air	22	°C/W
		Air Flow 1 m/s	19.4	°C/W
		Air Flow 2 m/s	18.3	°C/W
Thermal Resistance Junction to Case	θ_{JC}		9.5	°C/W
Thermal Resistance Junction to Board	θ_{JB}		9.4	°C/W
	Ψ_{JB}		9.3	°C/W
Thermal Resistance Junction to Top Center	Ψ_{JT}		0.2	°C/W
Si5344, Si5342-44QFN				
Thermal Resistance Junction to Ambient	θ_{JA}	Still Air	22.3	°C/W
		Air Flow 1 m/s	19.4	°C/W
		Air Flow 2 m/s	18.4	°C/W
Thermal Resistance Junction to Case	θ_{JC}		10.9	°C/W
Thermal Resistance Junction to Board	θ_{JB}		9.3	°C/W
	Ψ_{JB}		9.2	°C/W
Thermal Resistance Junction to Top Center	Ψ_{JT}		0.23	°C/W

Note:

1. Based on PCB Dimension: 3" x 4.5" PCB Thickness: 1.6 mm, PCB Land/Via: 36, Number of Cu Layers: 4

Table 5.14. Absolute Maximum Ratings [1, 2, 3]

Parameter	Symbol	Test Condition	Value	Unit
DC Supply Voltage	V_{DD}		–0.5 to 3.8	V
	V_{DDA}		–0.5 to 3.8	V
	V_{DDO}		–0.5 to 3.8	V
	V_{DDS}		–0.5 to 3.8	V
Input Voltage Range	V_{I1} [4]	IN0–IN3/FB_IN	–0.85 to 3.8	V
	V_{I2}	IN_SEL1, IN_SEL0, RSTb, OEb, I2C_SEL, FINC, FDEC, SDI, SCLK, A0/CSb, A1, SDA/SDIO	–0.5 to 3.8	V
	V_{I3}	XA/XB	–0.5 to 2.7	V
Latch-up Tolerance	LU		JESD78 Compliant	
ESD Tolerance	HBM	100 pF, 1.5 kΩ	2.0	kV
Storage Temperature Range	T_{STG}		–55 to 150	°C
Maximum Junction Temperature in Operation	T_{JCT}		125	°C
Soldering Temperature (Pb-free profile)[5]	T_{PEAK}		260	°C
Soldering Temperature Time at T_{PEAK} (Pb-free profile)[5]	T_P		20–40	s

Note:

1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. 64-QFN and 44-QFN packages are RoHS-6 compliant.
3. Moisture sensitivity level is MSL2. For more packaging information, go to the Silicon Labs RoHS information page.
4. The minimum voltage at these pins can be as low as –1.0 V when an ac input signal of 8 kHz or greater is applied. See Table 5.3 Input Clock Specifications on page 25 for single-ended ac-coupled f_{IN} < 250 MHz.
5. The device is compliant with JEDEC J-STD-020.

6. Typical Application Schematic

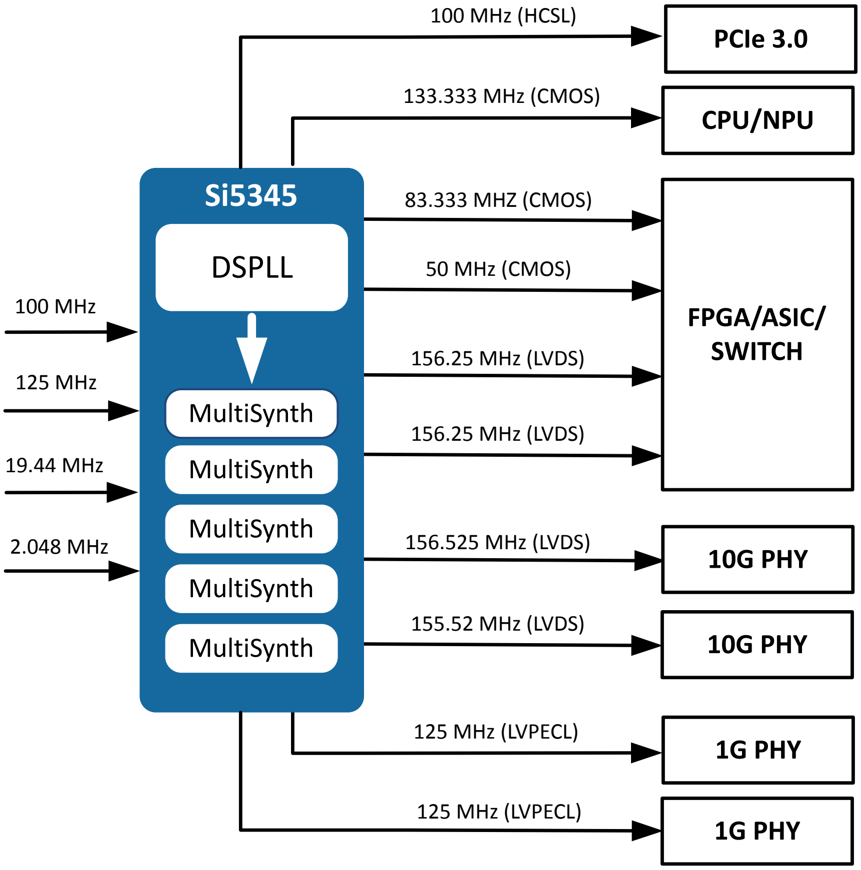


Figure 6.1. 10G Ethernet Data Center Switch and Compute Blade Schematic

7. Detailed Block Diagrams

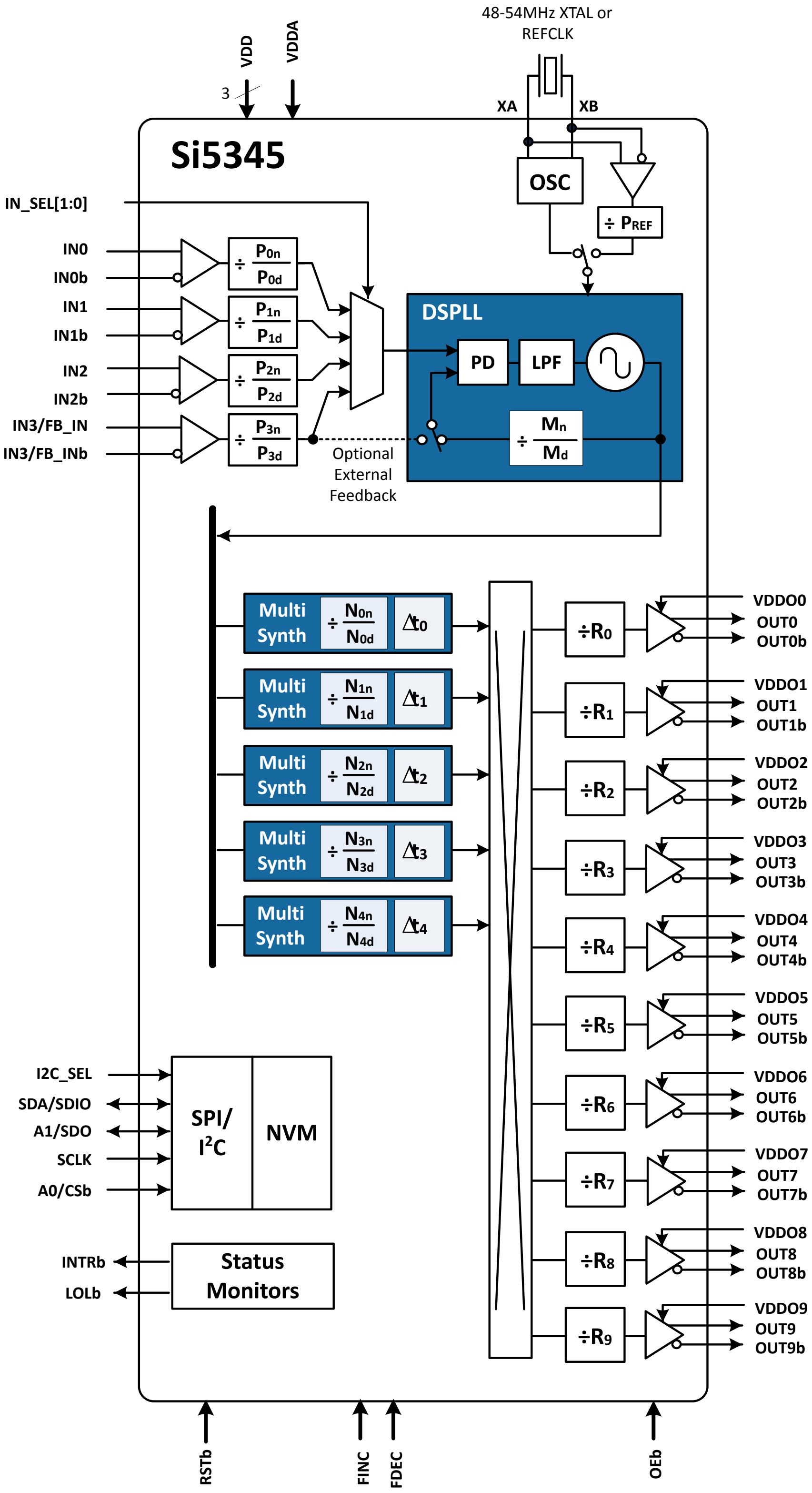


Figure 7.1. Si5345 Block Diagram

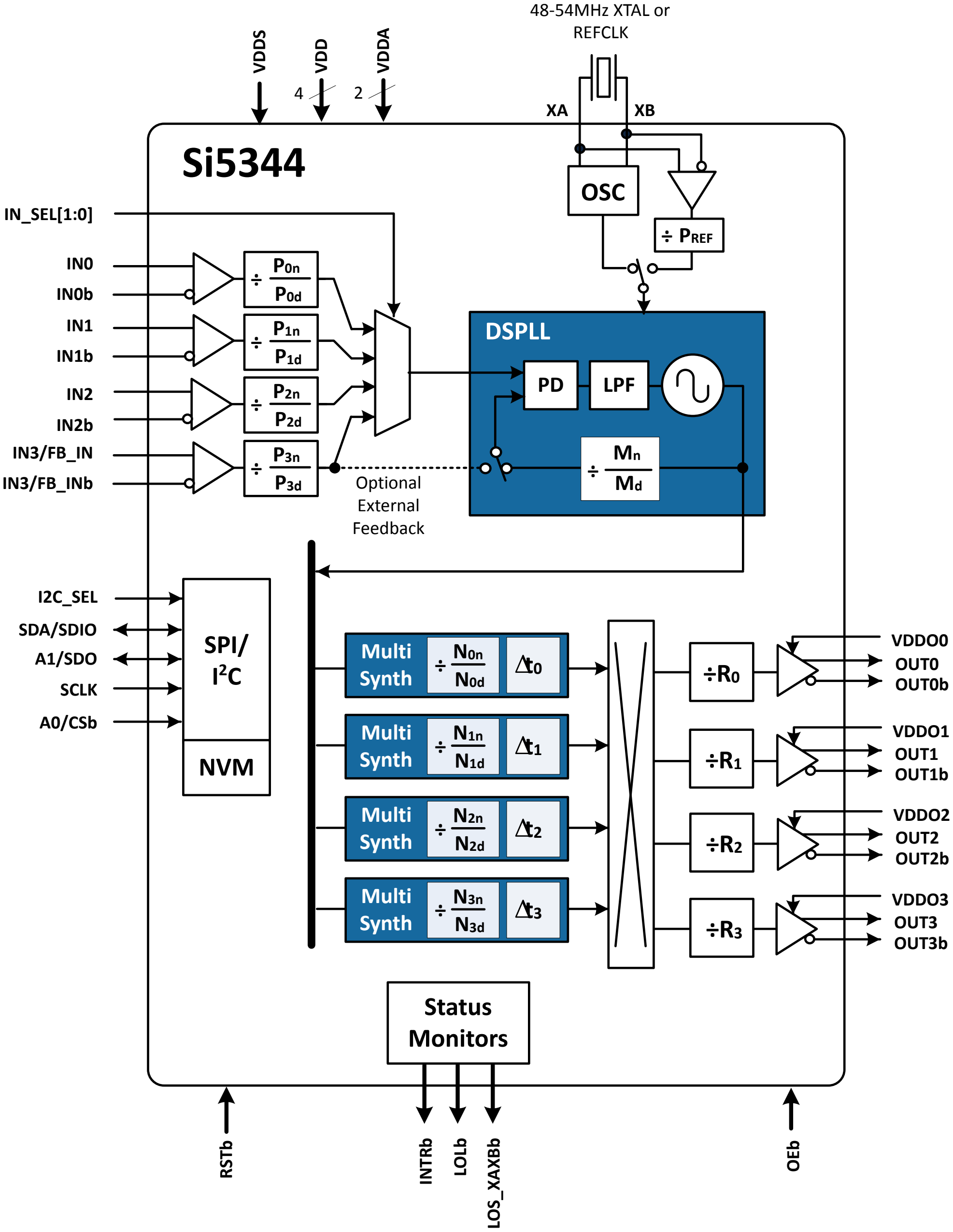


Figure 7.2. Si5344 Block Diagram

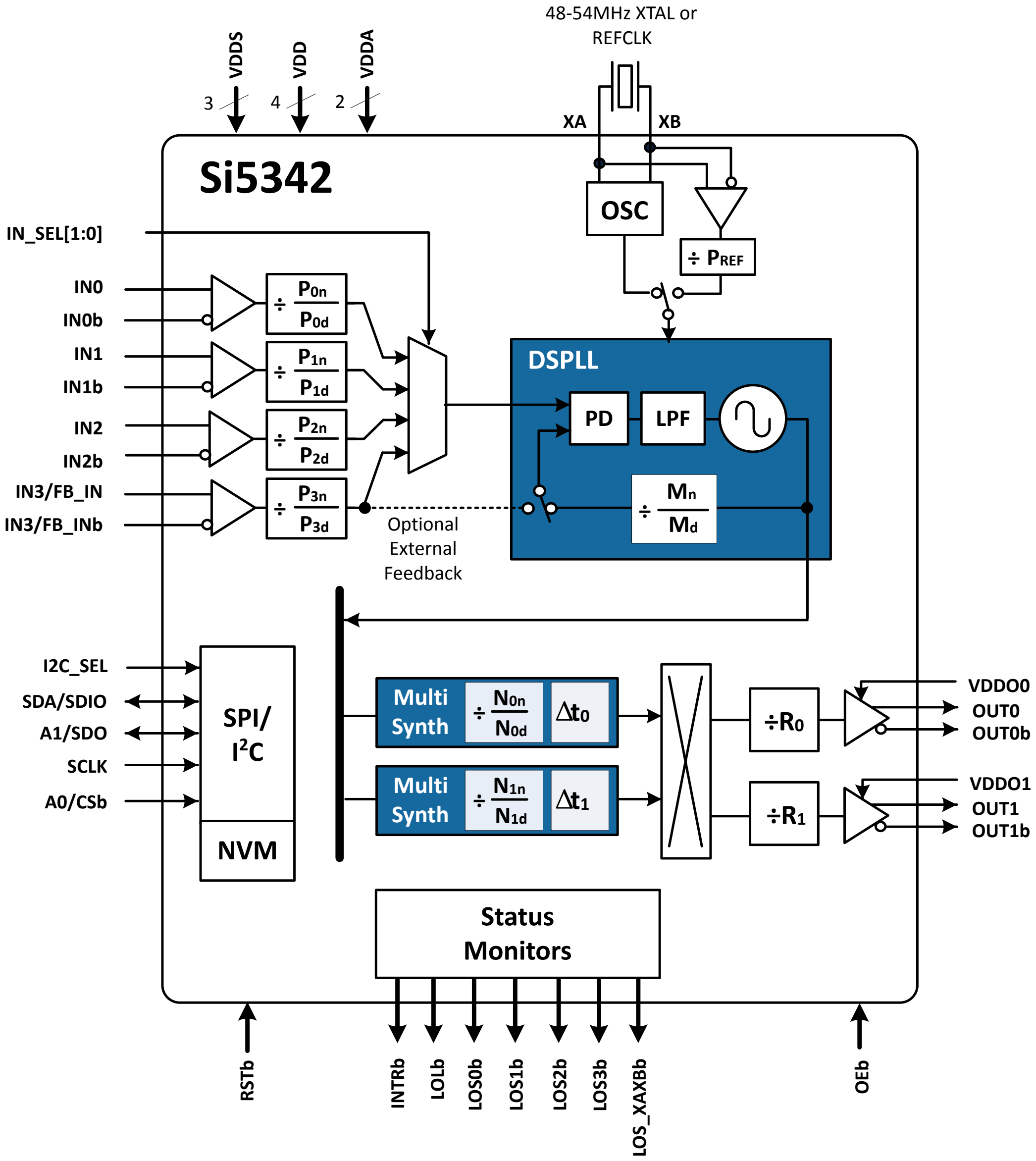
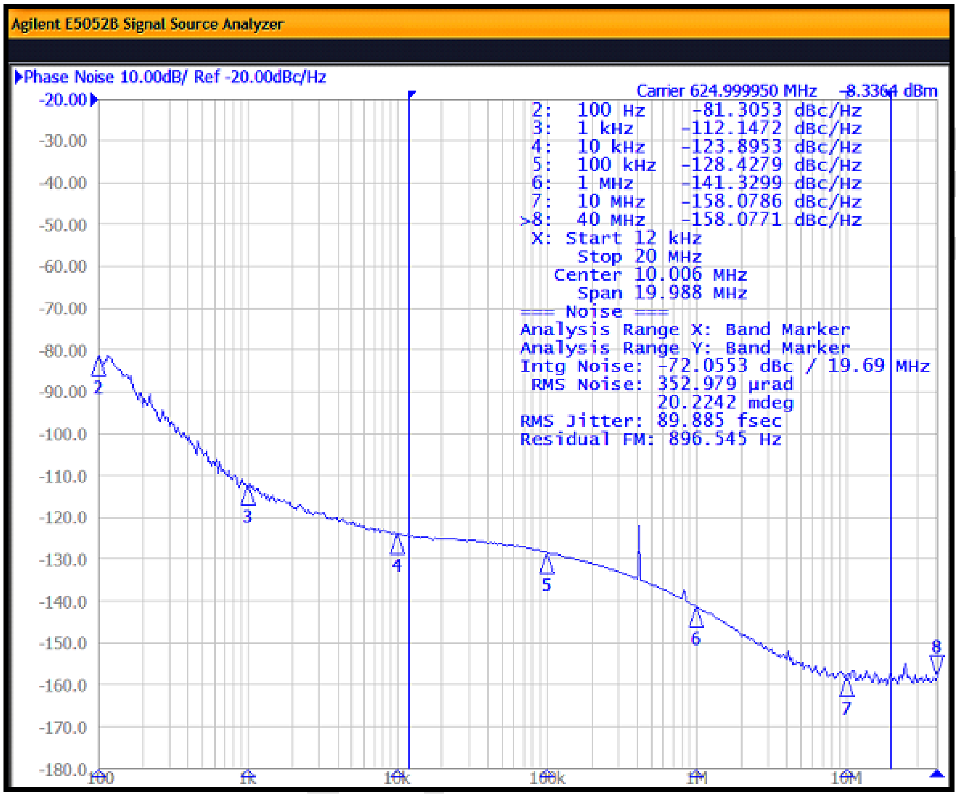


Figure 7.3. Si5342 Block Diagram

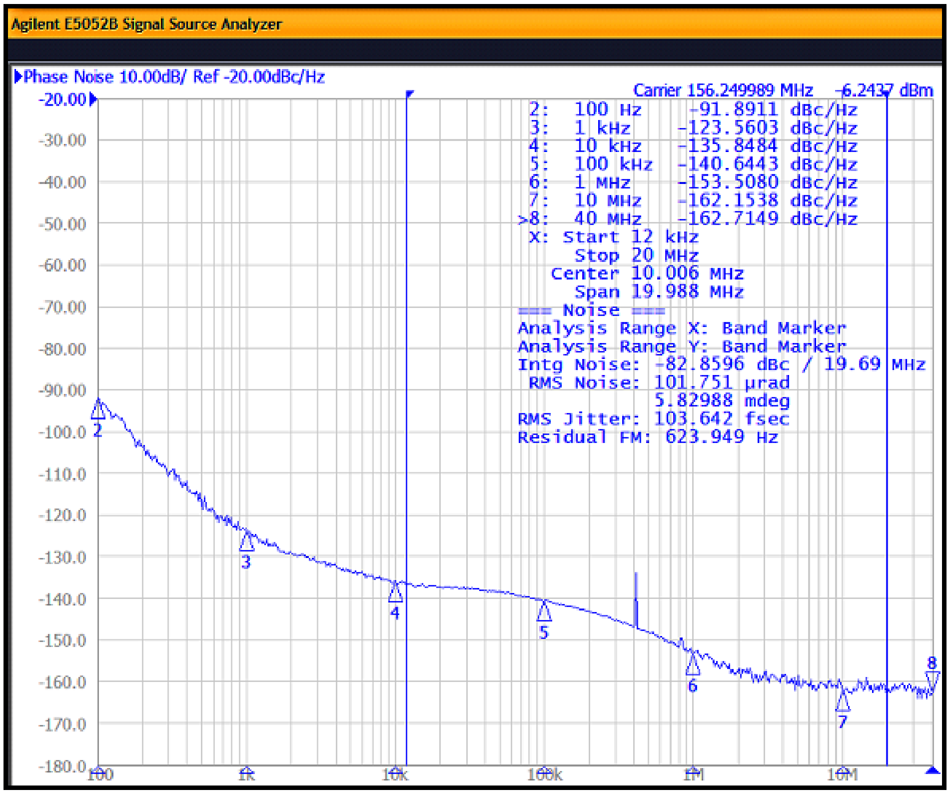
8. Typical Operating Characteristics

The phase noise plots below were taken under the following conditions: V_{DD} = 1.8 V; V_{DDA} = 3.3 V; V_{DDS} = 3.3 V, 1.8 V; T_A = 25 °C.



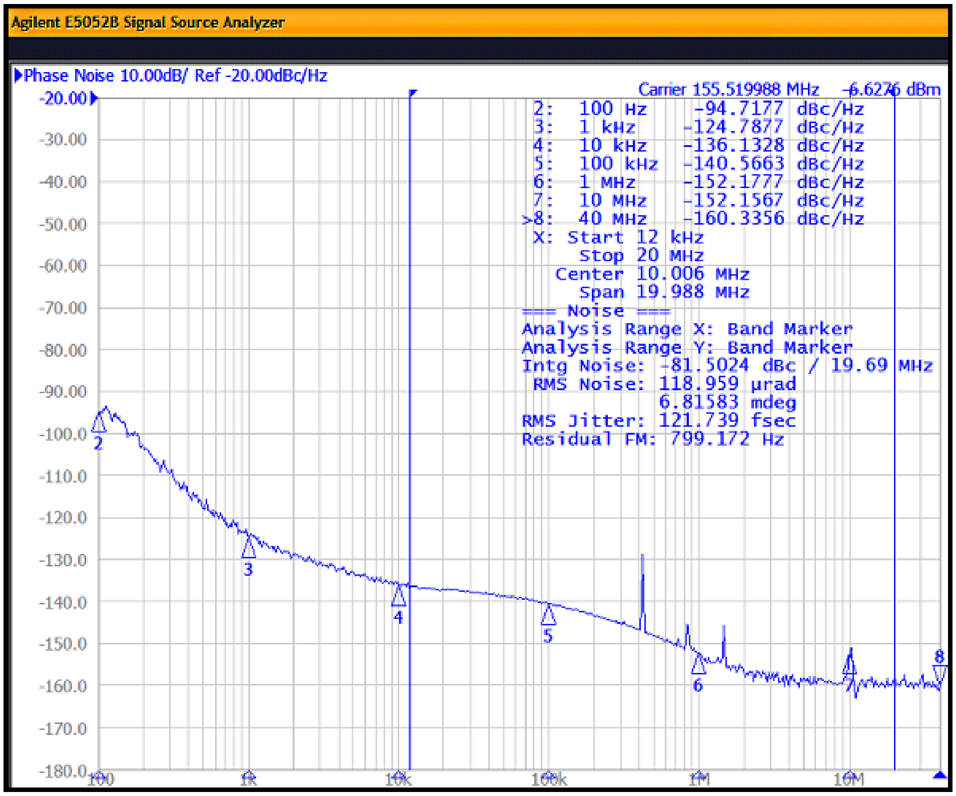
```
Carrier 624.999950 MHz    -8.3364 dBm
  2:  100 Hz      -81.3053 dBc/Hz
  3:  1 kHz      -112.1472 dBc/Hz
  4:  10 kHz     -123.8953 dBc/Hz
  5:  100 kHz    -128.4279 dBc/Hz
  6:  1 MHz      -141.3299 dBc/Hz
  7:  10 MHz     -158.0786 dBc/Hz
 >8:  40 MHz     -158.0771 dBc/Hz
  X: Start 12 kHz
         Stop 20 MHz
       Center 10.006 MHz
         Span 19.988 MHz
=== Noise ===
Analysis Range X: Band Marker
Analysis Range Y: Band Marker
Intg Noise: -72.0553 dBc / 19.69 MHz
 RMS Noise: 352.979 µrad
            20.2242 mdeg
RMS Jitter: 89.885 fsec
Residual FM: 896.545 Hz
```

Figure 8.1. Input = 25 MHz; Output = 625 MHz, 2.5 V LVDS



```
 2:  100 Hz     -91.8911 dBc/Hz
 3:  1 kHz     -123.5603 dBc/Hz
 4:  10 kHz    -135.8484 dBc/Hz
 5:  100 kHz   -140.6443 dBc/Hz
 6:  1 MHz     -153.5080 dBc/Hz
 7:  10 MHz    -162.1538 dBc/Hz
>8:  40 MHz    -162.7149 dBc/Hz
 X: Start 12 kHz
        Stop 20 MHz
     Center 10.006 MHz
        Span 19.988 MHz
=== Noise ===
Analysis Range X: Band Marker
Analysis Range Y: Band Marker
Intg Noise: -82.8596 dBc / 19.69 MHz
 RMS Noise: 101.751 µrad
            5.82988 mdeg
RMS Jitter: 103.642 fsec
Residual FM: 623.949 Hz
```

Figure 8.2. Input = 25 MHz; Output = 156.25 MHz, 2.5 V LVDS

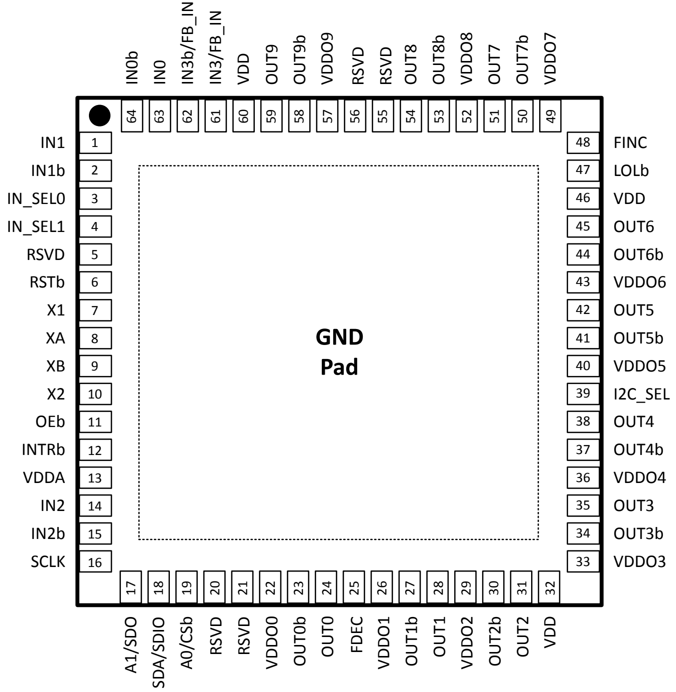


```
 2:  100 Hz     -94.7177 dBc/Hz
 3:  1 kHz     -124.7877 dBc/Hz
 4:  10 kHz    -136.1328 dBc/Hz
 5:  100 kHz   -140.5663 dBc/Hz
 6:  1 MHz     -152.1777 dBc/Hz
 7:  10 MHz    -152.1567 dBc/Hz
>8:  40 MHz    -160.3356 dBc/Hz
 X: Start 12 kHz
        Stop 20 MHz
     Center 10.006 MHz
        Span 19.988 MHz
=== Noise ===
Analysis Range X: Band Marker
Analysis Range Y: Band Marker
Intg Noise: -81.5024 dBc / 19.69 MHz
 RMS Noise: 118.959 µrad
            6.81583 mdeg
RMS Jitter: 121.739 fsec
Residual FM: 799.172 Hz
```

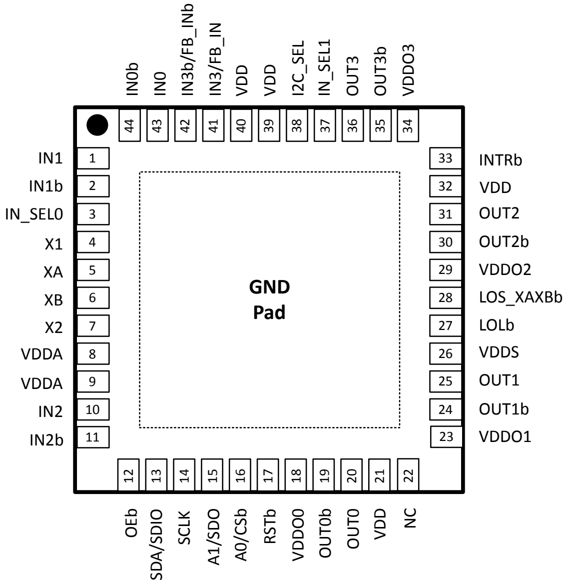
Figure 8.3. Input = 25 MHz; Output = 155.52 MHz, 2.5 V LVDS

9. Pin Descriptions

Si5345
Top View



Si5344 44QFN
Top View



Si5342 44QFN
Top View

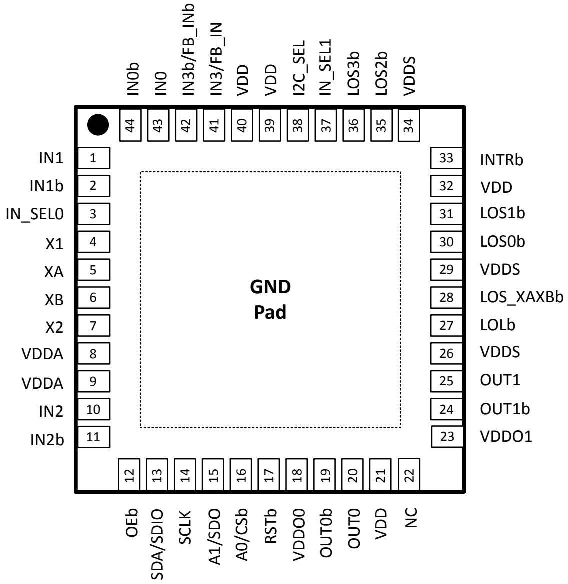


Table 9.1. Si5345/44/42 Pin Descriptions

Pin Name	Pin Number			Pin Type[1]	Function
	Si5345	Si5344	Si5342		
Inputs					
XA	8	5	5	I	**Crystal Input.** Input pins for external crystal (XTAL). Alternatively these pins can be driven with an external reference clock (REFCLK). An internal register bit selects XTAL or REFCLK mode. Default is XTAL mode.
XB	9	6	6	I	
X1	7	4	4	I	**XTAL Shield.** Connect these pins directly to the XTAL ground pins. X1, X2 and the XTAL ground pins should be separated from the PCB ground plane. Refer to the Si5345/44/42 Family Reference Manual for layout guidelines. These pins should be left disconnected when connecting XA/XB pins to an external reference clock (REFCLK).
X2	10	7	7	I	
IN0	63	43	43	I	**Clock Inputs.** These pins accept an input clock for synchronizing the device. They support both differential and single-ended clock signals. Refer to 3.7.6 Input Configuration and Terminations for input termination options. These pins are high-impedance and must be terminated externally. The negative side of the differential input must be grounded through a capacitor when accepting a single-ended clock.
IN0b	64	44	44	I	
IN1	1	1	1	I	
IN1b	2	2	2	I	
IN2	14	10	10	I	
IN2b	15	11	11	I	
IN3/FB_IN	61	41	41	I	**Clock Input 3/External Feedback Input.** By default these pins are used as the fourth clock input (IN3/IN3b). They can also be used as the external feedback input (FB_IN/FB_INb) for the optional zero delay mode. See 3.9.13 Zero Delay Mode for details on the optional zero delay mode.
IN3b/FB_INb	62	42	42	I	

Table 9.2. Si5345/44/42 Pin Descriptions

Pin Name	Pin Number			Pin Type[1]	Function
	Si5345	Si5344	Si5342		
Outputs					
OUT0	24	20	20	O	**Output Clocks.** These output clocks support a programmable signal swing and common mode voltage. Desired output signal format is configurable using register control. Termination recommendations are provided in 3.9.3 Differential Output Terminations and 3.9.4 LVCMOS Output Terminations. Unused outputs should be left unconnected.
OUT0b	23	19	19	O	
OUT1	28	25	25	O	
OUT1b	27	24	24	O	
OUT2	31	31	—	O	
OUT2b	30	30	—	O	
OUT3	35	36	—	O	
OUT3b	34	35	—	O	
OUT4	38	—	—	O	
OUT4b	37	—	—	O	
OUT5	42	—	—	O	
OUT5b	41	—	—	O	
OUT6	45	—	—	O	
OUT6b	44	—	—	O	
OUT7	51	—	—	O	
OUT7b	50	—	—	O	
OUT8	54	—	—	O	
OUT8b	53	—	—	O	
OUT9	59	—	—	O	
OUT9b	58	—	—	O	
Serial Interface					
I2C_SEL	39	38	38	I	**I^2C Select[2].** This pin selects the serial interface mode as I^2C (I2C_SEL = 1) or SPI (I2C_SEL = 0). This pin is internally pulled up by a ~ 20 kΩ resistor to the voltage selected by the IO_VDD_SEL register bit.
SDA/SDIO	18	13	13	I/O	**Serial Data Interface[2]** This is the bidirectional data pin (SDA) for the I^2C mode, or the bidirectional data pin (SDIO) in the 3-wire SPI mode, or the input data pin (SDI) in 4-wire SPI mode. When in I^2C mode, this pin must be pulled-up using an external resistor of at least 1 kΩ. No pull-up resistor is needed when is SPI mode. Tie low when unused.
A1/SDO	17	15	15	I/O	**Address Select 1/Serial Data Output[2]** In I^2C mode, this pin functions as the A1 address input pin and does not have an internal pull-up or pull-down resistor. In 4-wire SPI mode this is the serial data output (SDO) pin and drives high to the voltage selected by the IO_VDD_SEL bit. Leave disconnected when unused.

Pin Name	Pin Number			Pin Type[1]	Function
	Si5345	Si5344	Si5342		
SCLK	16	14	14	I	**Serial Clock Input**[2] This pin functions as the serial clock input for both I^{2}C and SPI modes. When in I^{2}C mode, this pin must be pulled-up using an external resistor of at least 1 kΩ. No pull-up resistor is needed when in SPI mode. Tie high or low when unused.
A0/CSb	19	16	16	I	**Address Select 0/Chip Select**[2] This pin functions as the hardware controlled address A0 in I^{2}C mode. In SPI mode, this pin functions as the chip select input (active low). This pin is internally pulled-up by a ~20 kΩ resistor and can be left unconnected when not in use.
Control/Status					
INTRb	12	33	33	O	**Interrupt**[2] This pin is asserted low when a change in device status has occurred. It should be left unconnected when not in use.
RSTb	6	17	17	I	**Device Reset**[2] Active low input that performs power-on reset (POR) of the device. Resets all internal logic to a known state and forces the device registers to their default values. Clock outputs are disabled during reset. This pin is internally pulled-up and can be left unconnected when not in use.
OEb	11	12	12	I	**Output Enable**[2] This pin disables all outputs when held high. This pin is internally pulled low and can be left unconnected when not in use.
LOLb	47	—	—	O	**Loss Of Lock (Si5345)**[2] This output pin indicates when the DSPLL is locked (high) or out-of-lock (low). It can be left unconnected when not in use.
	—	27	27	O	**Loss Of Lock (Si5344/42)**[3] This output pin indicates when the DSPLL is locked (high) or out-of-lock (low). It can be left unconnected when not in use.
LOS0b	—	—	30	O	**Loss Of Signal for IN0**[3] This pin indicate a loss of clock at the IN0 pin when low.
LOS1b	—	—	31	O	**Loss Of Signal for IN1**[3] This pin indicate a loss of clock at the IN1 pin when low.
LOS2b	—	—	35	O	**Loss Of Signal for IN2**[3] This pin indicate a loss of clock at the IN2 pin when low.
LOS3b	—	—	36	O	**Loss Of Signal for IN3**[3] This pin indicate a loss of clock at the IN3 pin when low.
LOS_XAXBb	—	28	28	O	**Loss Of Signal on XA/XB Pins**[3] This pin indicates a loss of signal at the XA/XB pins when low.

Pin Name	Pin Number			Pin Type[1]	Function
	Si5345	Si5344	Si5342		
FINC	48	—	—	I	**Frequency Increment Pin**[2] This pin is used to step-up the output frequency of a selected output. The affected output and its frequency change step size is register configurable. This pin is internally pulled low and can be left unconnected when not in use.
FDEC	25	—	—	I	**Frequency Decrement Pin**[2] This pin is used to step-down the output frequency of a selected output. The affected output driver and its frequency change step size is register configurable. This pin is internally pulled low and can be left unconnected when not in use.
IN_SEL0	3	3	3	I	**Input Reference Select**[2] The IN_SEL[1:0] pins are used in manual pin controlled mode to select the active clock input as shown in Table 3.1 Manual Input Selection Using IN_SEL[1:0] Pins on page 8. These pins are internally pulled low.
IN_SEL1	4	37	37	I	
RSVD	5	—	—	—	**Reserved** These pins are connected to the die. Leave disconnected.
	20	—	—	—	
	21	—	—	—	
	55	—	—	—	
	56	—	—	—	
NC	—	22	22		**No Connect** These pins are not connected to the die. Leave disconnected.
Power					
VDD	32	21	21	P	**Core Supply Voltage** The device operates from a 1.8 V supply. A 1.0 μF bypass capacitor should be placed very close to this pin. See the Si5345/44/42 Family Reference Manual for power supply filtering recommendations.
	46	32	32	P	
	60	39	39	P	
	—	40	40	P	
VDDA	13	8	8	P	**Core Supply Voltage 3.3 V** This core supply pin requires a 3.3 V power source. A 1 μF bypass capacitor should be placed very close to this pin. See the Si5345/44/42 Family Reference Manual for power supply filtering recommendations.
	—	9	9	P	
VDDS	—	26	26	P	**Status Output Voltage** The voltage on this pin determines VOL/VOH on the Si5342/44 LOL_A and LOL_B outputs. Connect to either 3.3 V or 1.8 V. A 1.0 μF bypass capacitor should be placed very close to this pin.
	—	—	29	P	
	—	—	34	P	

Pin Name	Pin Number			Pin Type[1]	Function
	Si5345	Si5344	Si5342		
VDDO0	22	18	18	P	**Output Clock Supply Voltage** Supply voltage (3.3 V, 2.5 V, 1.8 V) for OUTn, OUTn outputs. For unused outputs, leave VDDO pins unconnected. An alternative option is to connect the VDDO pin to a power supply and disable the output driver to minimize current consumption.
VDDO1	26	23	23	P	
VDDO2	29	29	—	P	
VDDO3	33	34	—	P	
VDDO4	36	—	—	P	
VDDO5	40	—	—	P	
VDDO6	43	—	—	P	
VDDO7	49	—	—	P	
VDDO8	52	—	—	P	
VDDO9	57	—	—	P	
GND PAD	—	—	—	P	**Ground Pad** This pad provides connection to ground and must be connected for proper operation. Use as many vias as practical, and keep the via length to an internal ground plane as short as possible.

Note:

1. I = Input, O = Output, P = Power.
2. The IO_VDD_SEL control bit (0x0943 bit 0) selects 3.3 V or 1.8 V operation.
3. The voltage on the VDDS pin(s) determines 3.3 V or 1.8 V operation.
4. Refer to the Family Reference Manual for more information on register setting names.
5. All status pins except I2C and SPI are push-pull.

10. Package Outlines

10.1 Si5345 9x9 mm 64-QFN Package Diagram

The following figure illustrates the package details for the Si5345. The table lists the values for the dimensions shown in the illustration.

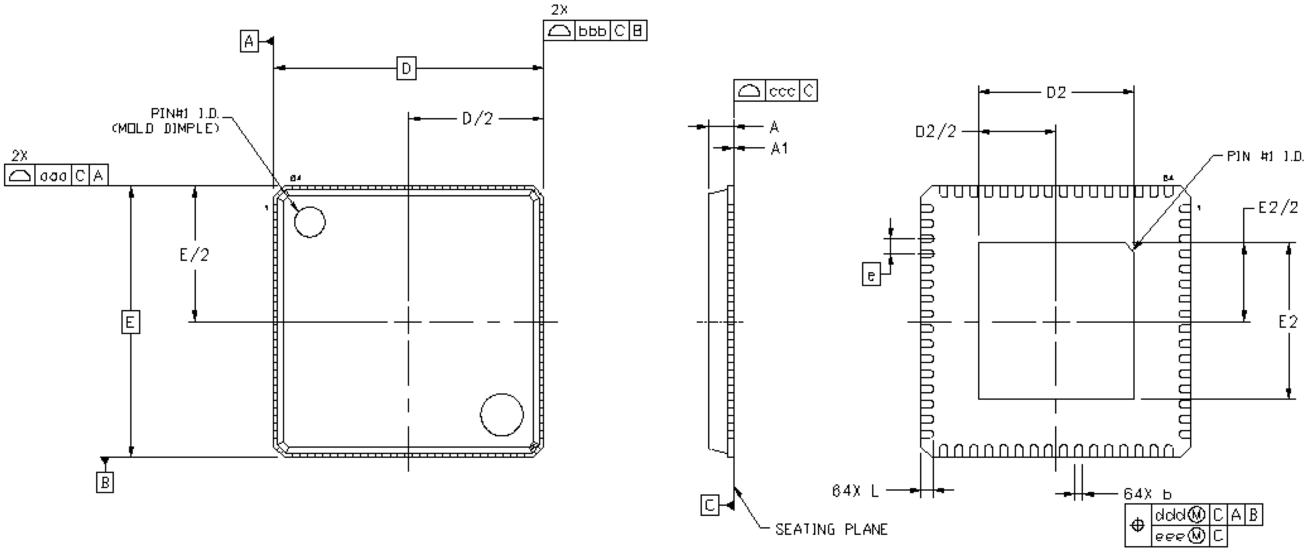


Figure 10.1. 64-Pin Quad Flat No-Lead (QFN)

Table 10.1. Package Dimensions

Dimension	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D		9.00 BSC	
D2	5.10	5.20	5.30
e		0.50 BSC	
E		9.00 BSC	
E2	5.10	5.20	5.30
L	0.30	0.40	0.50
aaa	—	—	0.10
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.10

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

10.2 Si5344 and Si5342 7x7 mm 44-QFN Package Diagram

The following figure illustrates the package details for the Si5344 and Si5342. The table lists the values for the dimensions shown in the illustration.

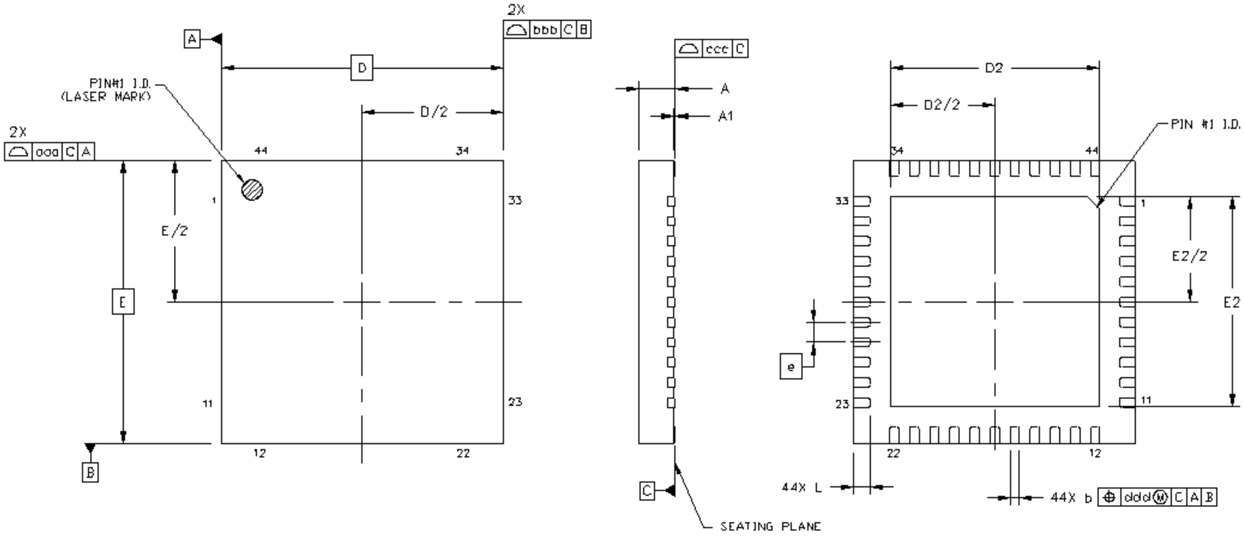


Figure 10.2. 44-Pin Quad Flat No-Lead (QFN)

Table 10.2. Package Dimensions

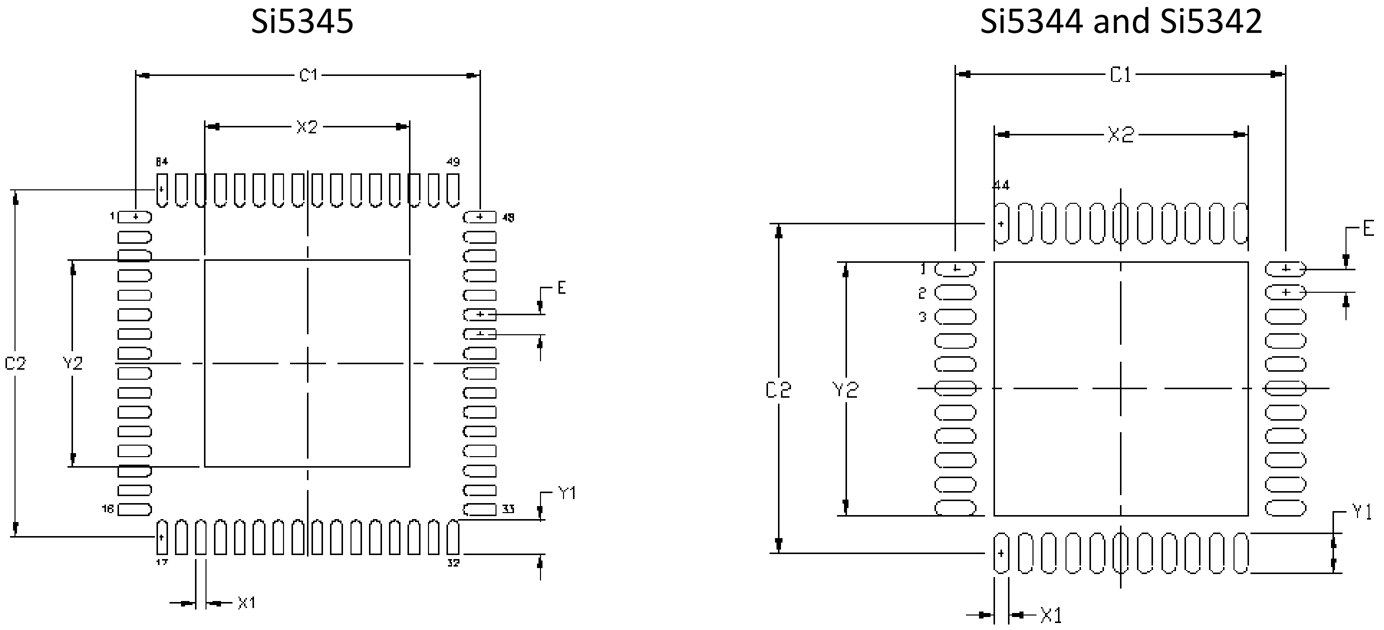
Dimension	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D	7.00 BSC		
D2	5.10	5.20	5.30
e	0.50 BSC		
E	7.00 BSC		
E2	5.10	5.20	5.30
L	0.30	0.40	0.50
aaa	—	—	0.10
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.10

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

11. PCB Land Pattern

The following figure illustrates the PCB land pattern details for the devices. The table lists the values for the dimensions shown in the illustration.



Si5345

Si5344 and Si5342

Figure 11.1. PCB Land Pattern

Table 11.1. PCB Land Pattern Dimensions

Dimension	Si5345 (Max)	Si5344/42 (Max)
C1	8.90	6.90
C2	8.90	6.90
E	0.50	0.50
X1	0.30	0.30
Y1	0.85	0.85
X2	5.30	5.30
Y2	5.30	5.30

Notes:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition is calculated based on a fabrication Allowance of 0.05 mm.

Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

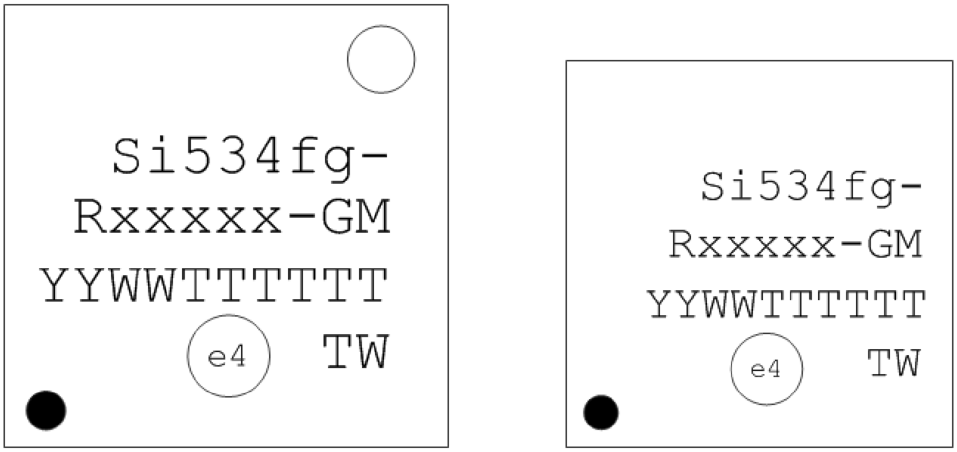
Stencil Design

1. A stainless steel, laser-cut and electropolished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
4. A 3x3 array of 1.25 mm square openings on 1.80 mm pitch should be used for the center ground pad.

Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

12. Top Marking



64-QFN 44-QFN

Figure 12.1. Si5345/44/42 Top Marking

Table 12.1. Top Marking Explanation

Line	Characters	Description
1	Si534fg-	Base part number and Device Grade for Any-frequency, Any-output, Jitter Cleaning Clock (single PLL): f = 5: 10-output Si5345: 64-QFN f = 4: 4-output Si5344: 44-QFN f = 2: 2-output Si5342: 44-QFN g = Device Grade (A, B, C, D). See 2. Ordering Guide for more information. – = Dash character.
2	Rxxxxx-GM	R = Product revision. (Refer to 2. Ordering Guide for latest revision). xxxxx = Customer specific NVM sequence number. Optional NVM code assigned for custom, factory pre-programmed devices. Characters are not included for standard, factory default configured devices. See 2. Ordering Guide for more information. -GM = Package (QFN) and temperature range (–40 to +85 °C)
3	YYWWTTTTTT	YYWW = Characters correspond to the year (YY) and work week (WW) of package assembly. TTTTTT = Manufacturing trace code.
4	Circle w/ 1.6 mm (64-QFN) or 1.4 mm (44-QFN) diameter	Pin 1 indicator; left-justified
	e4 TW	Pb-free symbol; Center-Justified TW = Taiwan; Country of Origin (ISO Abbreviation)

13. Device Errata

Log in or register at www.silabs.com to access the device errata document.

14. Document Change List

14.1 Revision 1.0

July 15, 2016

- Initial release.

14.2 Revision 1.1

August 7, 2017

- Refer to AN1006 for a list of changes from Rev B to Rev D.
- Updated block diagram on the front page.

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