Signetics

FAST 74F160A,74F161A 74F162A,74F163A Counters

'F160A, 'F162A BCD Decade Counter
'F161A, 'F163A 4-Bit Binary Counter
Product Specification

FAST Products

FEATURES

- **Synchronous counting and loading**
- **Two count enable inputs for n-bit cascading**
- **Positive edge-triggered clock**
- **Asynchronous Master Reset ('F160A, 'F161A)**
- **Synchronous Reset ('F162A, 'F163A)**
- **High speed synchronous expansion**
- **Typical count rate of 130MHz**

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F160A,74F161A 74F162A,74F163A	130MHz	46mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic Dip	N74F160AN, N74F161AN, N74F162AN, N74F163AN
16-Pin Plastic SO	N74F160AD, N74F161AD, N74F162AD, N74F163AD

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0 - D_3	Data inputs	1.0/1.0	20µA/0.6mA
CEP	Count Enable Parallel input	1.0/1.0	20µA/0.6mA
CET	Count Enable Trickle input	1.0/2.0	20µA/1.2mA
CP	Clock input (active rising edge)	1.0/1.0	20µA/0.6mA
$\overline{PE}$	Parallel Enable input (active Low)	1.0/2.0	20µA/1.2mA
$\overline{MR}$	Asynchronous Master Reset input (active Low) for 'F160A and 'F161A	1.0/1.0	20µA/0.6mA
$\overline{SR}$	Synchronous Reset input (active Low) for 'F162A and 'F163A	1.0/1.0	20µA/0.6mA
TC	Terminal count output	50/33	1.0mA/20mA
Q_0 - Q_3	Flip-flop outputs	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

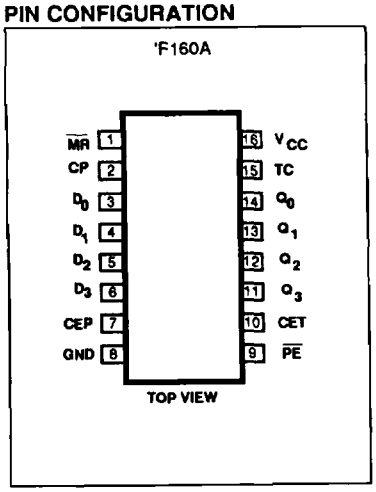
DESCRIPTION

Synchronous presettable decade ('F160A, 'F162A) and 4-bit binary('F161A, 'F163A) counters feature an internal carry look-ahead and can be used for high-speed counting. Synchronous operation is provided by having all flip-flops clocked simultaneously on the positive-going edge of the clock. The clock input is buffered.

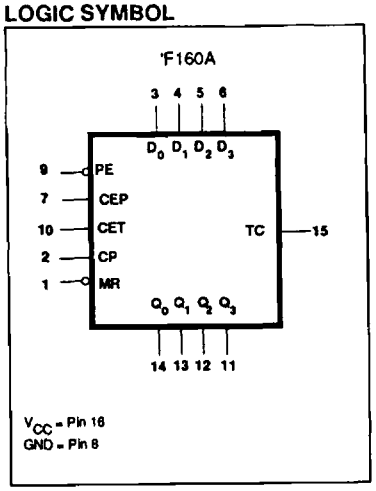
The outputs of the counters may be preset to High or Low level. A Low level at the Parallel Enable ($\overline{PE}$) input disables the counting action and causes the data at the D_0-D_3 inputs to be loaded into the counter on the positive-going edge of the clock (provided that the setup and hold requirements for $\overline{PE}$ are met). Preset takes place regardless of the levels at Count Enable (CEP, CET) inputs.

A Low level at the Master Reset ($\overline{MR}$) input sets all the four outputs of the flip-flops (Q_0-Q_3) in 'F160A and 'F161A to Low levels, regardless of the levels at CP,$\overline{PE}$,CET and CEP inputs (thus providing an asynchronous clear function). For the 'F162A/'F163A the clear function is synchronous. A Low level at the Synchronous Reset ($\overline{SR}$) input sets all four outputs of the flip-flops (Q_0-Q_3) to Low levels after the next positive-going transition on the clock (CP) input (provided that the setup and hold time requirements for $\overline{SR}$ are met). This action occurs regardless of the levels at $\overline{PE}$, CET, and CEP inputs. The synchronous reset feature enables the designer to modify the maximum count with only one external NAND gate (see Figure A). The carry look-ahead simpli-

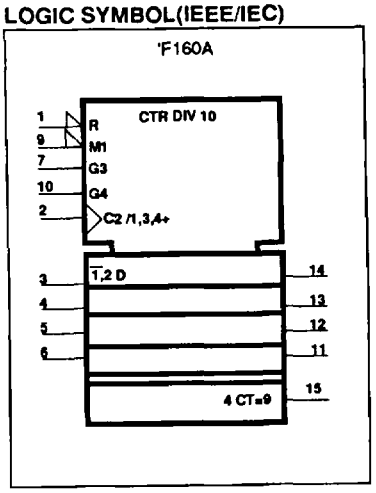
PIN CONFIGURATION



LOGIC SYMBOL

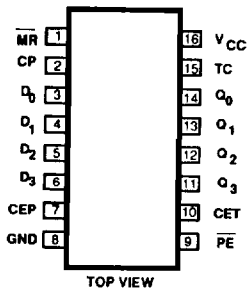


LOGIC SYMBOL(IEEE/IEC)



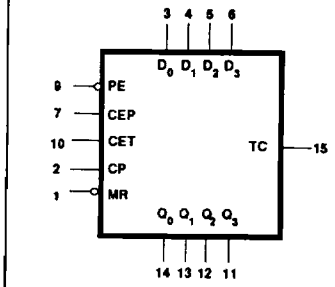
PIN CONFIGURATION

'F161A



LOGIC SYMBOL

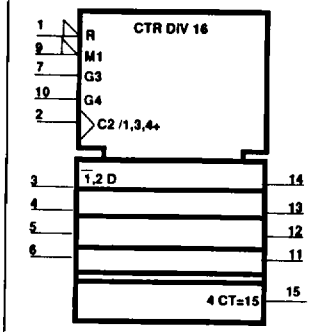
'F161A



V_{CC} = Pin 16
GND = Pin 8

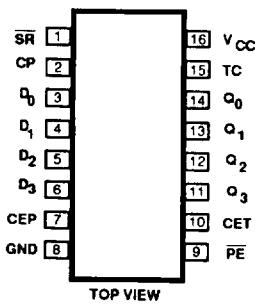
LOGIC SYMBOL(IEEE/IEC)

'F161A



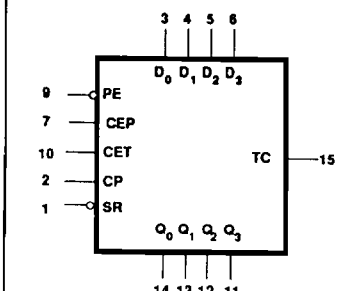
PIN CONFIGURATION

'F162A



LOGIC SYMBOL

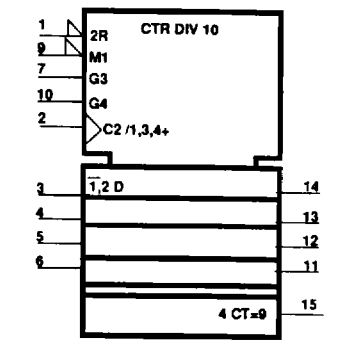
'F162A



V_{CC} = Pin 16
GND = Pin 8

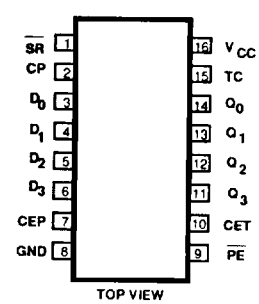
LOGIC SYMBOL(IEEE/IEC)

'F162A



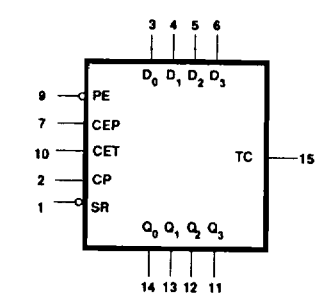
PIN CONFIGURATION

'F163A



LOGIC SYMBOL

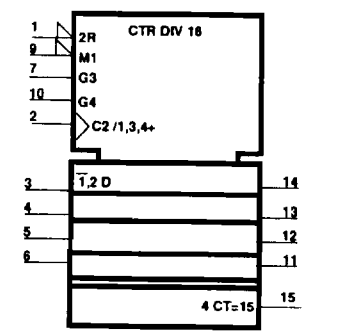
'F163A



V_{CC} = Pin 16
GND = Pin 8

LOGIC SYMBOL(IEEE/IEC)

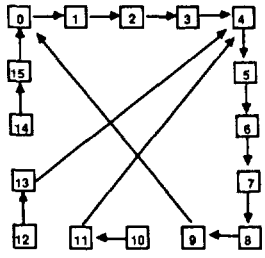
'F163A



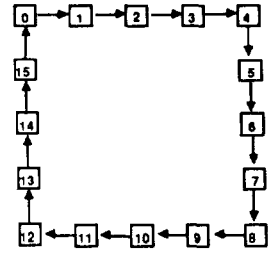
fies serial cascading of the counters. Both Count Enable (CEP and CET) inputs must be High to count. The CET input is fed forward to enable the TC output. The TC output thus enabled will produce a High output pulse of a duration approximately equal to the High level output of Q_0. This pulse can be used to enable the next cascaded stage (see Figure B). The TC output is subjected to decoding spikes due to internal race conditions. Therefore, it is not recommended for use as clock or asynchronous reset for flip-flops, registers, or counters.

STATE DIAGRAM

Logic equations: Count Enable=CEP•CET•$\overline{PE}$
$TC=Q_0 \cdot \overline{Q}_1 \cdot \overline{Q}_2 \cdot Q_3 \cdot CET$
'F160A, 'F162A



Logic equations: Count Enable=CEP•CET•$\overline{PE}$
$TC=Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot CET$
'F161A,'F163A



APPLICATIONS

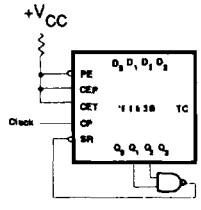


Fig. A Maximum count modifying scheme
Terminal count = 6

H H = Enable count
or
L L = Disable count

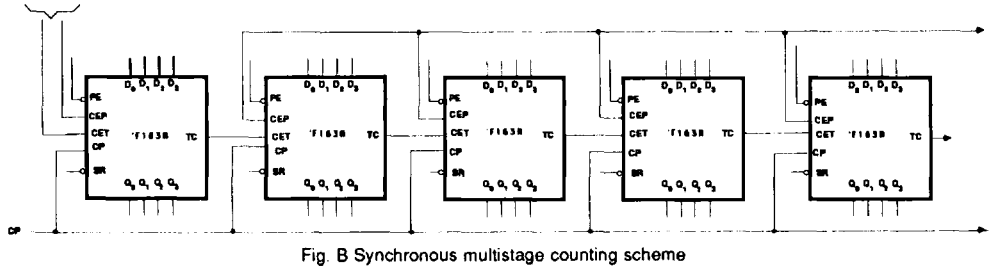


Fig. B Synchronous multistage counting scheme

MODE SELECT-FUNCTION TABLE for 'F160A, 'F161A

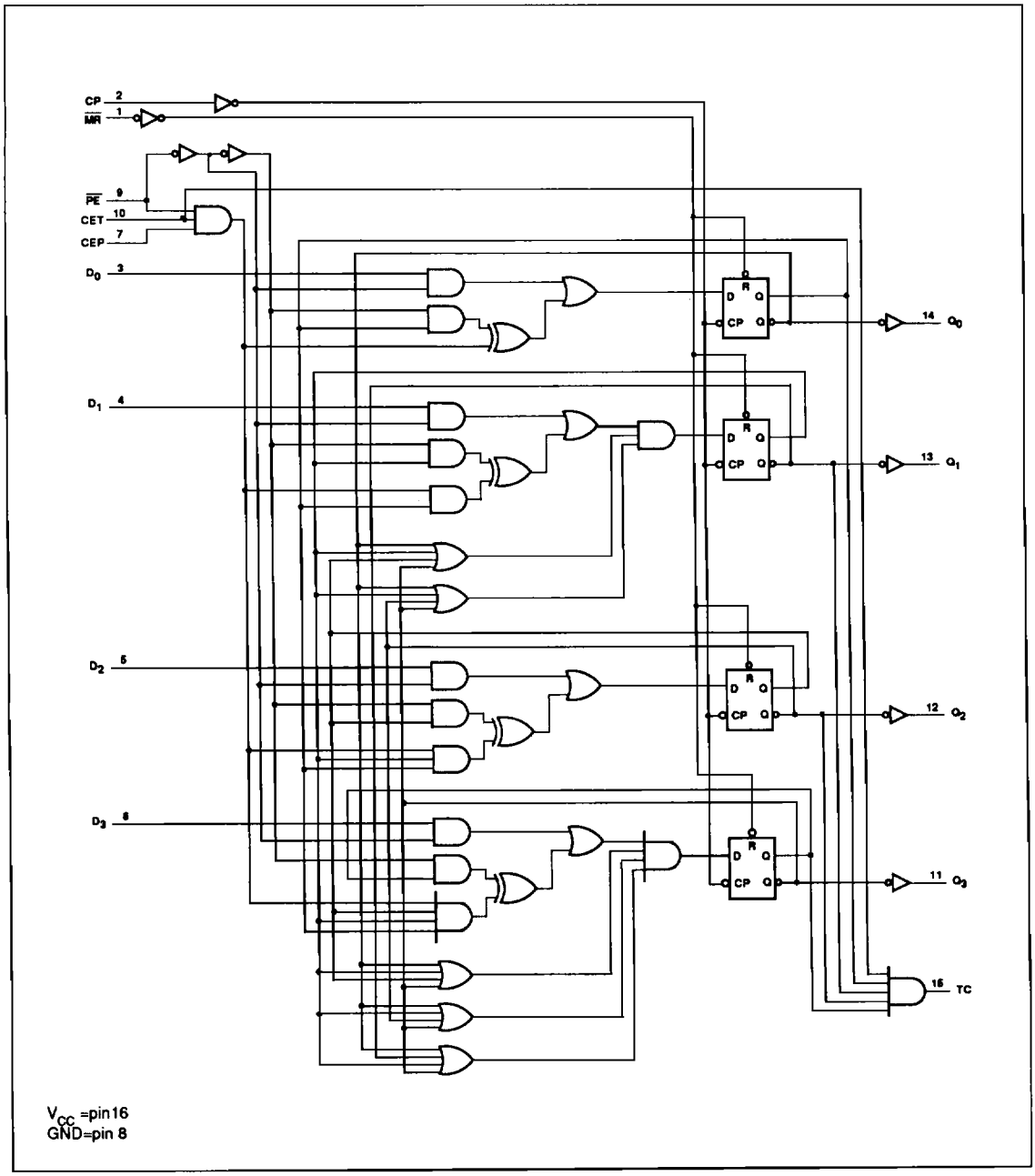
INPUTS						OUTPUTS		OPERATING MODE
$\overline{MR}$	CP	CEP	CET	$\overline{PE}$	D_n	Q_n	TC	
L	X	X	X	X	X	L	L	Reset (clear)
H	↑	X	X	l	l	L	L	Parallel load
H	↑	X	X	l	h	H	(1)	
H	↑	h	h	h	X	count	(1)	Count
H	X	l	X	h	X	q_n	(1)	Hold (do nothing)
H	X	X	l	h	X	q_n	L	

MODE SELECT-FUNCTION TABLE for 'F162A, 'F163A

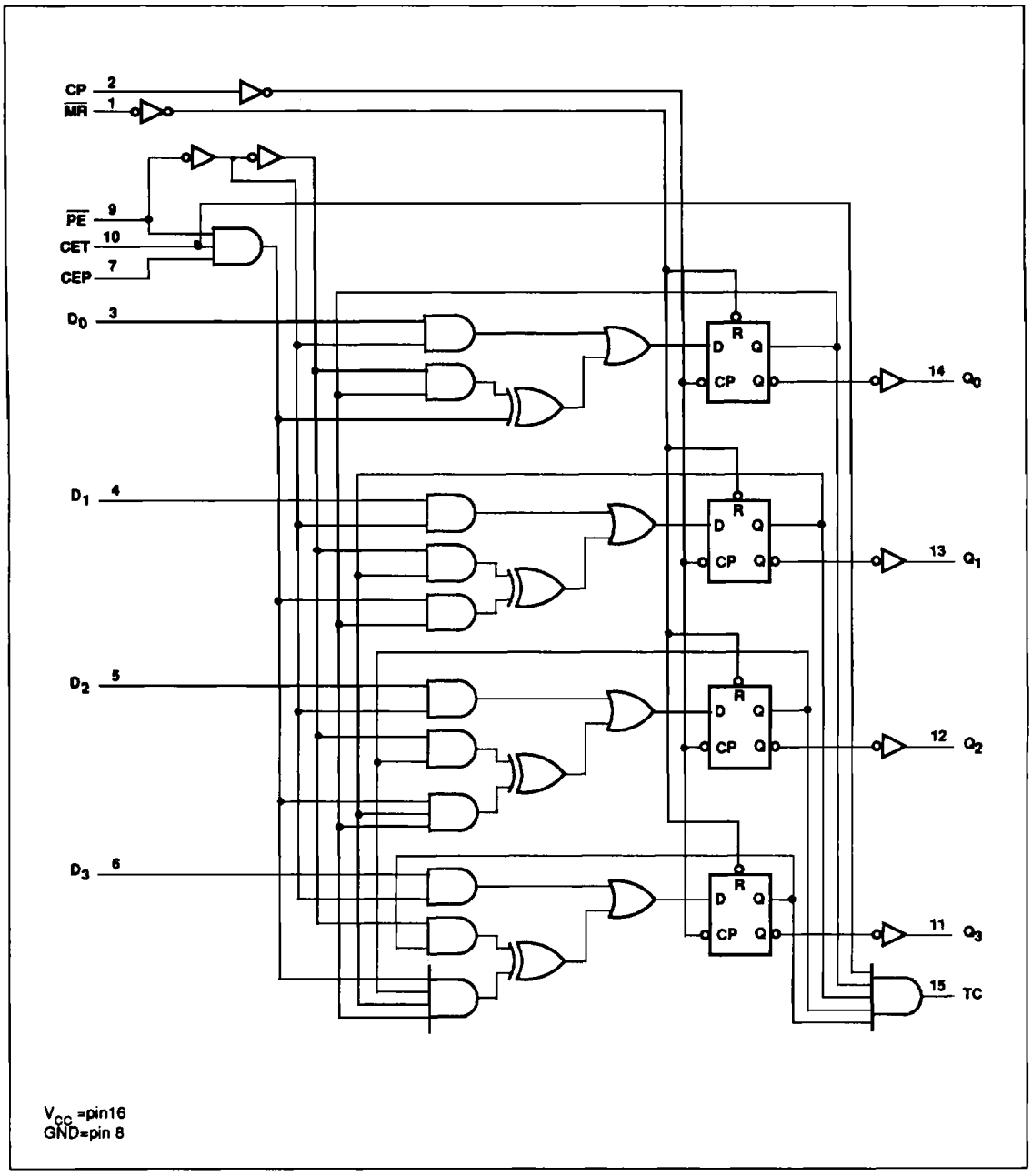
INPUTS						OUTPUTS		OPERATING MODE
$\overline{SR}$	CP	CEP	CET	$\overline{PE}$	D_n	Q_n	TC	
l	↑	X	X	X	X	L	L	Reset (clear)
h	↑	X	X	l	l	L	L	Parallel load
h	↑	X	X	l	h	H	(2)	
h	↑	h	h	h	X	count	(2)	Count
h	X	l	X	h	X	q_n	(2)	Hold (do nothing)
h	X	X	l	h	X	q_n	L	

H = High voltage level
h = High voltage level one setup prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one setup prior to the Low-to-High clock transition
q_n = Lower case letters indicate the state of the referenced output prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition
(1) = The TC output is High when CET is High and the counter is at Terminal Count (HLLH for 'F160A and HHHH for 'F161A)
(2) = The TC output is High when CET is High and the counter is at Terminal Count (HLLH for 'F162A and HHHH for 'F163A)

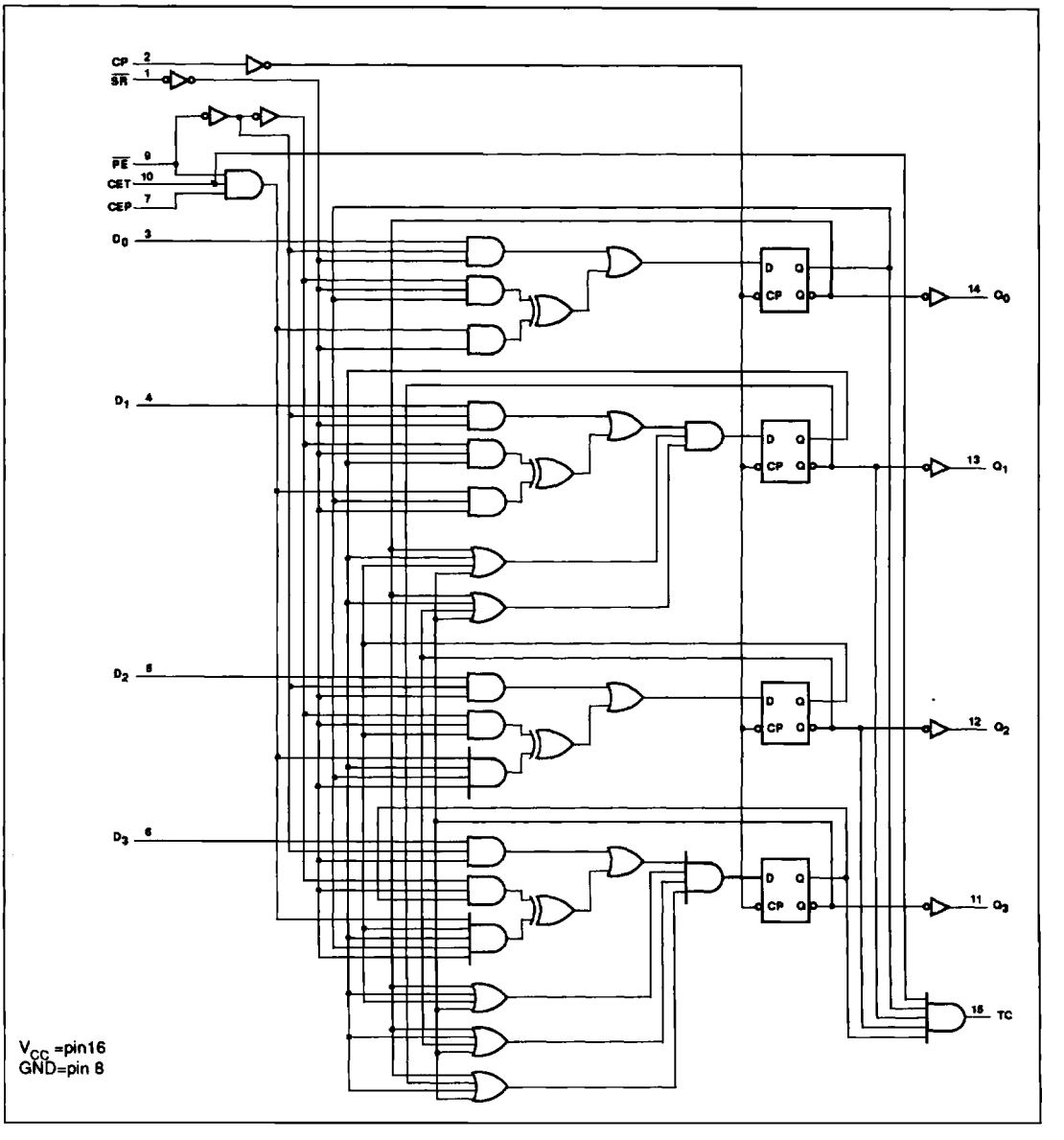
LOGIC DIAGRAM for 'F160A



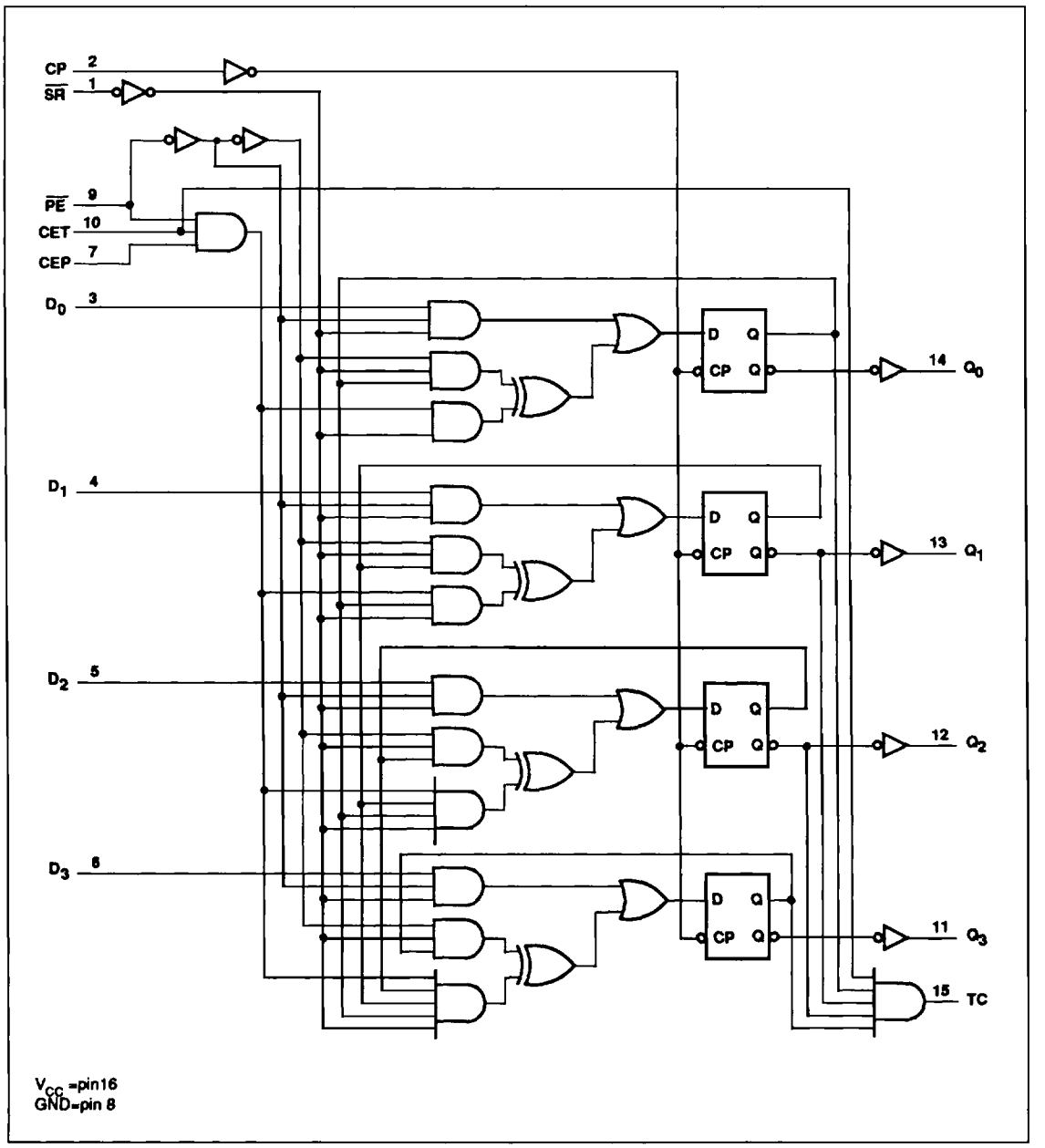
LOGIC DIAGRAM for 'F161A



LOGIC DIAGRAM for 'F162A



LOGIC DIAGRAM for 'F163A



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	CET, $\overline{PE}$	V_{CC} = MAX, V_I = 0.5V				-1.2	mA
		others					-0.6	mA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			42	55	mA
		I_{CCL}				49	65	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS for 74F160A and 74F162A

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency		Waveform 1	100	130		90		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n ($\overline{PE}$=High)		Waveform 1	2.0 4.0	4.5 7.0	7.0 10.0	2.0 4.0	8.0 11.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to Q_n ($\overline{PE}$= Low)		Waveform 1	2.0 4.0	4.5 6.0	7.5 8.5	2.0 4.0	8.5 9.5	ns
t_{PLH} t_{PHL}	Propagation delay CP to TC		Waveform 1	4.5 4.5	8.0 7.5	10.5 9.5	4.5 4.5	11.5 10.0	ns
t_{PLH} t_{PHL}	Propagation delay CET to TC		Waveform 2	1.5 2.5	4.0 5.0	6.5 7.0	1.5 2.5	7.0 7.5	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	'F160A	Waveform 3	6.5	9.0	12.0	6.5	13.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to TC	'F160A	Waveform 3	6.0	8.0	10.0	5.5	11.0	ns

AC SETUP REQUIREMENTS for 74F160A and 74F162A

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
t_s(H) t_s(L)	Setup time, High or Low D_n to CP		Waveform 6	5.0 5.0			5.0 5.0		ns
t_h(H) t_h(L)	Hold time, High or Low D_n to CP		Waveform 6	0 0			0 0		ns
t_s(H) t_s(L)	Setup time, High or Low $\overline{PE}$ or $\overline{SR}$ to CP		Waveform 5 or 6	11.0 7.0			11.0 7.0		ns
t_h(H) t_h(L)	Hold time, High or Low $\overline{PE}$ or $\overline{SR}$ to CP		Waveform 5 or 6	0 0			0 0		ns
t_s(H) t_s(L)	Setup time, High or Low CET or CEP to CP		Waveform 4	11.0 6.0			11.0 7.5		ns
t_h(H) t_h(L)	Hold time, High or Low CET or CEP to CP		Waveform 4	0 0			0 0		ns
t_w(H) t_w(L)	CP pulse width (Load) High or Low		Waveform 1	4.0 5.0			4.0 6.0		ns
t_w(H) t_w(L)	CP pulse width (Count) High or Low		Waveform 1	4.0 5.5			4.0 6.5		ns
t_w(L)	$\overline{MR}$ pulse width,Low	'F160A	Waveform 3	5.0			5.0		ns
t_{REC}	Recovery time, $\overline{MR}$ to CP	'F160A	Waveform 3	5.0			6.0		ns

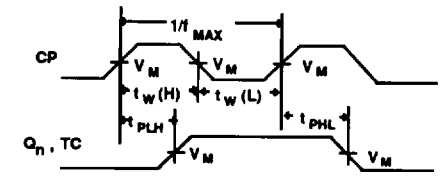
AC ELECTRICAL CHARACTERISTICS for 74F161A and 74F163A

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency		Waveform 1	100	130		90		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n ($\overline{PE}$=High)		Waveform 1	2.0 4.0	4.0 6.5	6.5 10.0	2.0 4.0	7.0 11.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to Q_n ($\overline{PE}$= Low)		Waveform 1	2.0 3.5	4.5 5.5	6.5 8.5	2.0 3.5	7.5 9.5	ns
t_{PLH} t_{PHL}	Propagation delay CP to TC		Waveform 1	5.0 4.5	7.5 7.5	10.5 10.5	5.0 4.0	11.5 11.5	ns
t_{PLH} t_{PHL}	Propagation delay CET to TC		Waveform 2	1.5 2.5	3.5 5.0	6.5 7.5	1.5 2.5	7.0 8.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	'F161A	Waveform 3	6.0	8.5	12.0	5.5	13.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to TC	'F161A	Waveform 3	5.0	8.5	10.0	5.0	11.0	ns

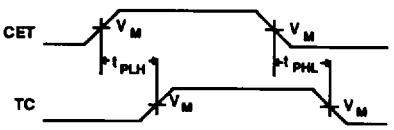
AC SETUP REQUIREMENTS for 74F161A and 74F163A

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
t_s(H) t_s(L)	Setup time, High or Low D_n to CP		Waveform 6	5.0 5.0			5.0 5.0		ns
t_h(H) t_h(L)	Hold time, High or Low D_n to CP		Waveform 6	0 0			0 0		ns
t_s(H) t_s(L)	Setup time, High or Low $\overline{PE}$ or $\overline{SR}$ to CP		Waveform 5 or 6	9.0 6.5			9.5 7.0		ns
t_h(H) t_h(L)	Hold time, High or Low $\overline{PE}$ or $\overline{SR}$ to CP		Waveform 5 or 6	0 0			0 0		ns
t_s(H) t_s(L)	Setup time, High or Low CET or CEP to CP		Waveform 4	10.5 6.0			10.5 7.0		ns
t_h(H) t_h(L)	Hold time, High or Low CET or CEP to CP		Waveform 4	0 0			0 0		ns
t_w(H) t_w(L)	CP pulse width (Load) High or Low		Waveform 1	4.0 5.0			4.0 5.5		ns
t_w(H) t_w(L)	CP pulse width (Count) High or Low		Waveform 1	4.0 6.0			4.0 7.0		ns
t_w(L)	$\overline{MR}$ pulse width,Low	'F161A	Waveform 3	4.5			4.5		ns
t_{REC}	Recovery time, $\overline{MR}$ to CP	'F161A	Waveform 3	6.0			6.5		ns

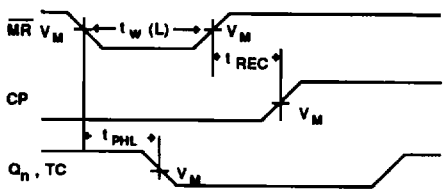
AC WAVEFORMS



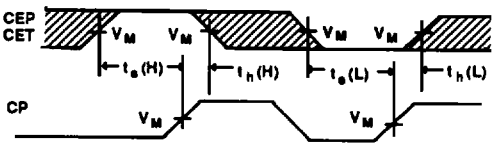
Waveform 1.
Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



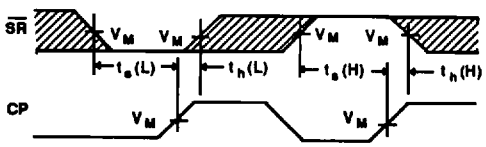
Waveform 2.
Propagation Delay, CET Input to TC Output



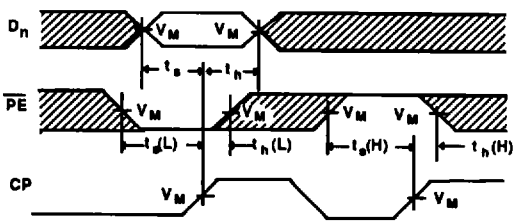
Waveform 3.
Master Reset pulse width, Master Reset to Output Delay and Master Reset to Recovery Time



Waveform 4.
CEP and CET Reset Setup and Hold Times



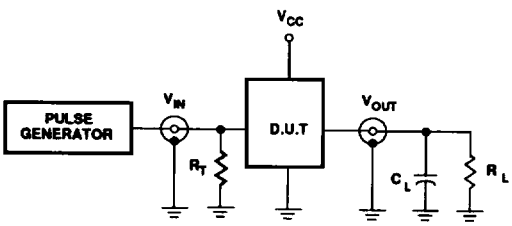
Waveform 5.
Synchronous Reset Setup and Hold Times



Waveform 6.
Parallel Data and Parallel Enable Setup and Hold Times

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



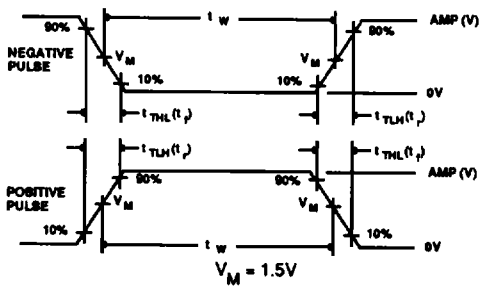
Test Circuit For Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns