

Low Voltage Automotive Fast 128K x 8 SRAM

Features

- 131072 x 8 bit static CMOS RAM
- 35 and 55 ns Access Time
- Common data inputs and data outputs
- Three-state outputs
- Typ. operating supply current  
35 ns: 45mA  
55 ns: 30mA
- Standby current <100µA at 125°C
- TTL/CMOS-compatible
- Power supply voltage 3.3 V
- Operating temperature range  
-40 °C to 85 °C  
-40 °C to 125 °C
- CECC 90000 Quality Standard
- ESD protection > 2000 V (MIL STD 883C M3015.7)
- Latch-up immunity >100 mA
- Package: SOP32 (300/330 mil)

Description

The UL62H1708A is a static RAM manufactured using a CMOS process technology with the following operating modes:

- Read                      - Standby
- Write                     - Data Retention

The memory array is based on a 6-Transistor cell.

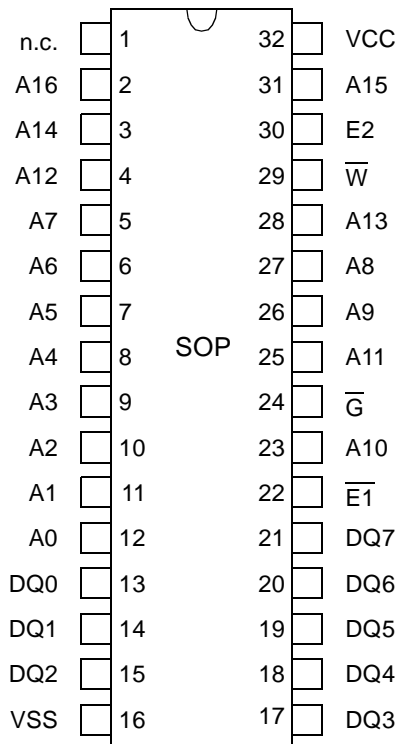
The circuit is activated by the rising edge of E2 (at E1 = L), or the falling edge of E1 (at E2 = H). The address and control inputs open simultaneously. According to the information of  $\overline{W}$  and  $\overline{G}$ , the data inputs, or outputs, are active. During the active state (E1 = L and E2 = H) each address change leads to a new Read or Write cycle. In a Read cycle, the data outputs are activated by the falling edge of  $\overline{G}$ , afterwards the data word will be available at the outputs DQ0-DQ7. After the address change, the data

outputs go High-Z until the new information is available. The data outputs have no preferred state. If the memory is driven by CMOS levels in the active state, and if there is no change of the address, data input and control signals  $\overline{W}$  or  $\overline{G}$ , the operating current ( $I_O = 0$  mA) drops to the value of the operating current in the Standby mode. The Read cycle is finished by the falling edge of E2 or  $\overline{W}$ , or by the rising edge of E1, respectively.

Data retention is guaranteed down to 2 V. With the exception of E1 and E2, all inputs consist of NOR gates, so that no pull-up/pull-down resistors are required.

Pin Configuration

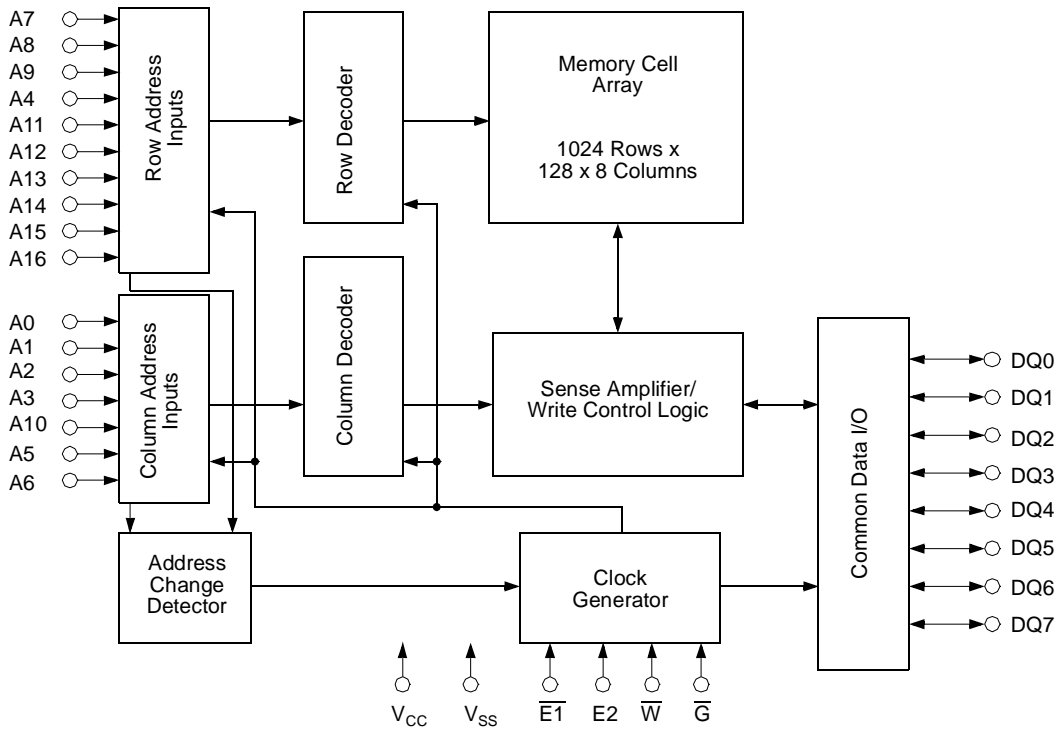
Pin Description



Top View

Signal Name	Signal Description
A0 - A16	Address Inputs
DQ0 - DQ7	Data In/Out
E1	Chip Enable 1
E2	Chip Enable 2
G-bar	Output Enable
W-bar	Write Enable
VCC	Power Supply Voltage
VSS	Ground
n.c.	not connected

Block Diagram



Truth Table

Operating Mode	$\overline{E1}$	E2	$\overline{W}$	$\overline{G}$	DQ0 - DQ7
Standby/not selected	*	L	*	*	High-Z
	H	*	*	*	High-Z
Internal Read	L	H	H	H	High-Z
Read	L	H	H	L	Data Outputs Low-Z
Write	L	H	L	*	Data Inputs High-Z

\* H or L

Characteristics

All voltages are referenced to  $V_{SS} = 0$  V (ground).

All characteristics are valid in the power supply voltage range and in the operating temperature range specified.

Dynamic measurements are based on a rise and fall time of  $\leq 5$  ns, measured between 10 % and 90 % of  $V_I$ , as well as input levels of  $V_{IL} = 0$  V and  $V_{IH} = 2.5$  V. The timing reference level of all input and output signals is 1.5 V, with the exception of the  $t_{dis}$ -times and  $t_{en}$ -times, in which cases transition is measured  $\pm 200$  mV from steady-state voltage.

Maximum Ratings	Symbol	Min.	Max.	Unit	
Power Supply Voltage	$V_{CC}$	-0.3	4.6	V	
Input Voltage	$V_I$	-0.5	$V_{CC} + 0.5$	V	
Output Voltage	$V_O$	-0.5	$V_{CC} + 0.5$	V	
Power Dissipation	$P_D$	-	1	W	
Operating Temperature	K-Type A-Type	$T_a$	-40	85	$^{\circ}C$
			-40	125	
Storage Temperature	$T_{stg}$	-65	150	$^{\circ}C$	
Output Short-Circuit Current at $V_{CC} = 3.3$ V and $V_O = 0$ V**	$ I_{OS} $		100	mA	

\*\* Not more than 1 output should be shorted at the same time. Duration of the short circuit should not exceed 30 s.

Recommended Operating Conditions	Symbol	Conditions	Min.	Max.	Unit
Power Supply Voltage	$V_{CC}$		3.0	3.6	V
Input Low Voltage*	$V_{IL}$		-0.3	0.8	V
Input High Voltage	$V_{IH}$		2.0	$V_{CC} + 0.3$	V

\* -2 V at Pulse Width 10 ns

Electrical Characteristics	Symbol	Conditions	Min.	Max.	Unit
Supply Current - Operating Mode	$I_{CC(OP)}$	$V_{CC} = 3.6\text{ V}$ $V_{IL} = 0.8\text{ V}$ $V_{IH} = 2.0\text{ V}$ $t_{cW} = 35\text{ ns}$ $t_{cW} = 55\text{ ns}$ $t_{cW} = 70\text{ ns}$		90 70 60	mA mA mA
Supply Current - Standby Mode (CMOS level)	$I_{CC(SB)}$	$V_{CC} = 3.6\text{ V}$ $V_{E1} = V_{E2} = V_{CC} - 0.2\text{ V}$		100	$\mu\text{A}$
Supply Current - Standby Mode (TTL level)	$I_{CC(SB)1}$	$V_{CC} = 3.6\text{ V}$ $V_{E1} = V_{E2} = 2.0\text{ V}$ K-Type A-Type		10 20	mA mA
Output High Voltage	$V_{OH}$	$V_{CC} = 3.0\text{ V}$ $I_{OH} = -0.5\text{ mA}$	2.2		V
Output Low Voltage	$V_{OL}$	$V_{CC} = 3.0\text{ V}$ $I_{OL} = 0.5\text{ mA}$		0.4	V
Input High Leakage Current	$I_{IH}$	$V_{CC} = 3.6\text{ V}$ $V_{IH} = 3.6\text{ V}$		2	$\mu\text{A}$
Input Low Leakage Current	$I_{IL}$	$V_{CC} = 3.6\text{ V}$ $V_{IL} = 0\text{ V}$	-2		$\mu\text{A}$
Output High Current	$I_{OH}$	$V_{CC} = 3.0\text{ V}$ $V_{OH} = 2.0\text{ V}$		-0.5	mA
Output Low Current	$I_{OL}$	$V_{CC} = 3.0\text{ V}$ $V_{OL} = 0.4\text{ V}$	0.5		mA
Output Leakage Current High at Three-State Outputs	$I_{OHZ}$	$V_{CC} = 3.6\text{ V}$ $V_{OH} = 3.6\text{ V}$		2	$\mu\text{A}$
Low at Three-State Outputs	$I_{OLZ}$	$V_{CC} = 3.6\text{ V}$ $V_{OL} = 0\text{ V}$	-2		$\mu\text{A}$

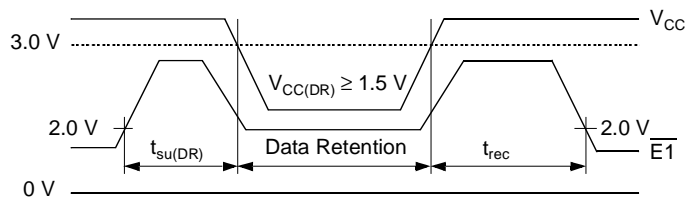
Switching Characteristics Read Cycle	Symbol		35		55		Unit
	Alt.	IEC	Min.	Max.	Min.	Max.	
Read Cycle Time	$t_{RC}$	$t_{cR}$	35		55		ns
Address Access Time to Data Valid	$t_{AA}$	$t_{a(A)}$		35		55	ns
Chip Enable Access Time to Data Valid	$t_{ACE}$	$t_{a(E)}$		35		55	ns
$\overline{G}$ LOW to Data Valid	$t_{OE}$	$t_{a(G)}$		15		25	ns
$\overline{E1}$ HIGH or E2 LOW to Output in High-Z	$t_{HZCE}$	$t_{dis(E)}$		12		15	ns
$\overline{G}$ HIGH to Output in High-Z	$t_{HZOE}$	$t_{dis(G)}$		12		15	ns
$\overline{E1}$ LOW or E2 HIGH to Output in Low-Z	$t_{LZCE}$	$t_{en(E)}$	3		3		ns
$\overline{G}$ LOW to Output in Low-Z	$t_{LZOE}$	$t_{en(G)}$	0		0		ns
Output Hold Time from Address Change	$t_{OH}$	$t_{v(A)}$	3		3		ns
$\overline{E1}$ LOW or E2 HIGH to Power-Up Time	$t_{PU}$		0		0		ns
$\overline{E1}$ HIGH or E2 LOW to Power-Down Time	$t_{PD}$			35		55	ns

Switching Characteristics Write Cycle	Symbol		35		55		Unit
	Alt.	IEC	Min.	Max.	Min.	Max.	
Write Cycle Time	$t_{WC}$	$t_{cW}$	35		55		ns
Write Pulse Width	$t_{WP}$	$t_{w(W)}$	20		35		ns
Write Setup Time	$t_{WP}$	$t_{su(W)}$	20		35		ns
Address Setup Time	$t_{AS}$	$t_{su(A)}$	0		0		ns
Address Valid to End of Write	$t_{AW}$	$t_{su(A-WH)}$	20		40		ns
Chip Enable Setup Time	$t_{CW}$	$t_{su(E)}$	25		40		ns
Pulse Width Chip Enable to End of Write	$t_{CW}$	$t_{w(E)}$	25		40		ns
Data Setup Time	$t_{DS}$	$t_{su(D)}$	15		25		ns
Data Hold Time	$t_{DH}$	$t_{h(D)}$	0		0		ns
Address Hold from End of Write	$t_{AH}$	$t_{h(A)}$	0		0		ns
$\overline{W}$ LOW to Output in High-Z	$t_{HZWE}$	$t_{dis(W)}$		15		20	ns
$\overline{G}$ HIGH to Output in High-Z	$t_{HZOE}$	$t_{dis(G)}$		12		15	ns
$\overline{W}$ HIGH to Output in Low-Z	$t_{LZWE}$	$t_{en(W)}$	0		0		ns
$\overline{G}$ LOW to Output in Low-Z	$t_{LZOE}$	$t_{en(G)}$	0		0		ns

Data Retention Mode

Data Retention Characteristics	Symbol		Conditions	Min.	Typ.	Max.	Unit
	Alt.	IEC					
Data Retention Supply Voltage		$V_{CC(DR)}$		1.5		3.6	V
Data Retention Supply Current		$I_{CC(DR)}$	$V_{CC(DR)} = 2\text{ V}$ $V_{\overline{E1}} = V_{E2} = V_{CC(DR)} - 0.2\text{ V}$			30	$\mu\text{A}$
Data Retention Setup Time	$t_{CDR}$	$t_{su(DR)}$	See Data Retention Waveforms (below)	0			ns
Operating Recovery Time	$t_R$	$t_{rec}$		$t_{cR}$			ns

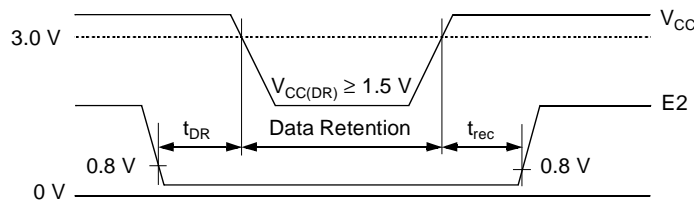
Data Retention Mode  $\overline{E1}$  - controlled



$$V_{E2(DR)} \geq V_{CC(DR)} - 0.2\text{ V or } V_{E2(DR)} \leq 0.2\text{ V}$$

$$V_{CC(DR)} - 0.2\text{ V} \leq V_{\overline{E1}(DR)} \leq V_{CC(DR)} + 0.2\text{ V}$$

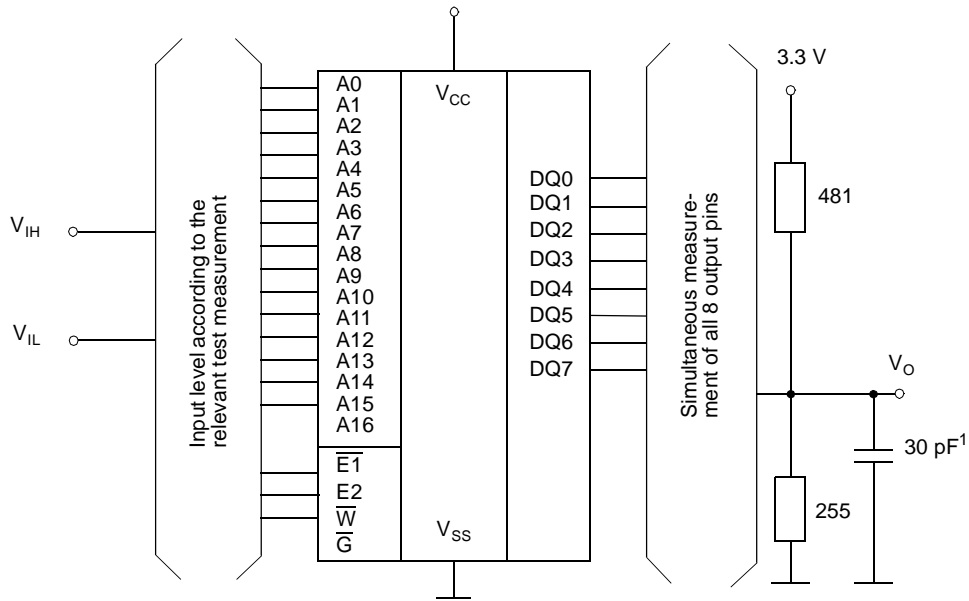
Data Retention Mode E2 - controlled



$$V_{E1(DR)} \geq V_{CC(DR)} - 0.2\text{ V or } V_{E1(DR)} \leq 0.2\text{ V}$$

$$V_{E2(DR)} \leq 0.2\text{ V}$$

Test Configuration for Functional Check

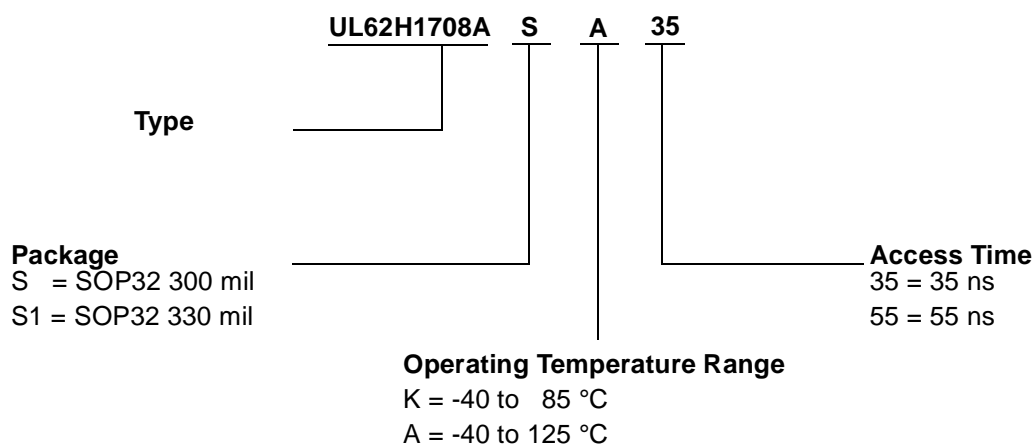


1) In measurement of  $t_{dis(E)}$ ,  $t_{dis(W)}$ ,  $t_{en(E)}$ ,  $t_{en(W)}$ ,  $t_{en(G)}$  the capacitance is 5 pF.

Capacitance	Conditions	Symbol	Min.	Max.	Unit
Input Capacitance	$V_{CC} = 3.3\text{ V}$ $V_I = V_{SS}$	$C_i$		7	pF
Output Capacitance	$f = 1\text{ MHz}$ $T_a = 25\text{ }^\circ\text{C}$	$C_o$		7	pF

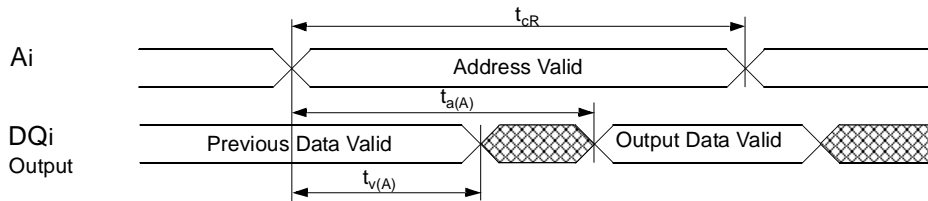
All pins not under test must be connected with ground by capacitors.

IC Code Numbers

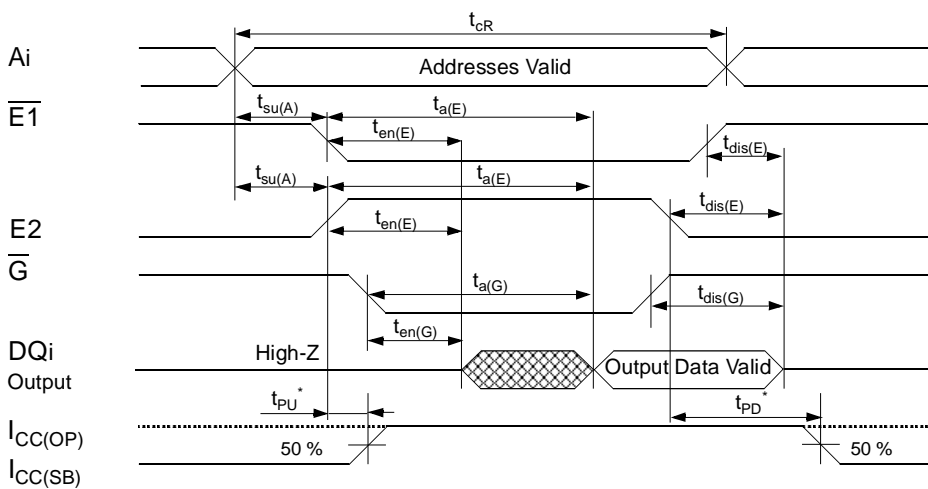


The date of manufacture is given by the last 4 digits of the mark, the first 2 digits indicating the year, and the last 2 digits the calendar week.

Read Cycle 1:  $\overline{A}_i$ -controlled (during Read Cycle :  $\overline{E1} = \overline{G} = V_{IL}, \overline{W} = E2 = V_{IH}$ )

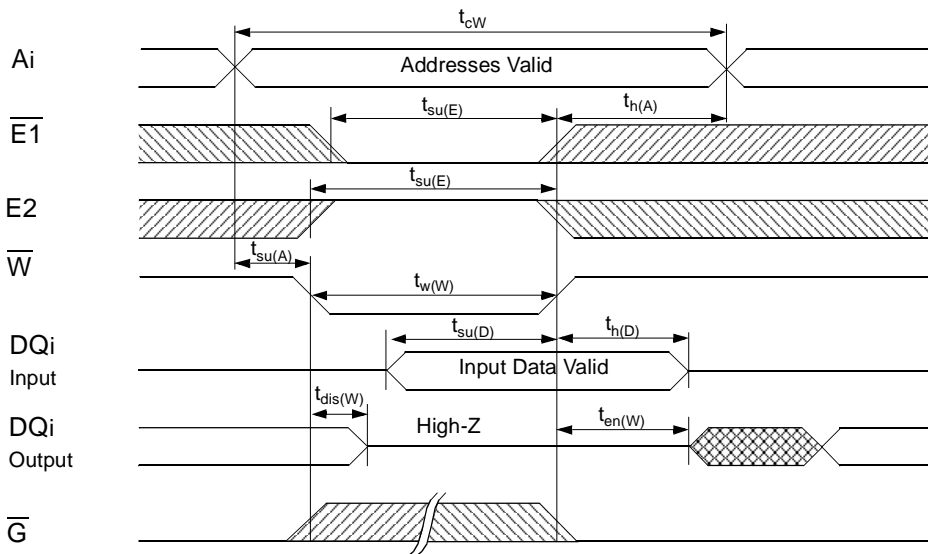


Read Cycle 2:  $\overline{G}$ -,  $\overline{E1}$ , E2-controlled (during Read Cycle:  $\overline{W} = V_{IH}$ )

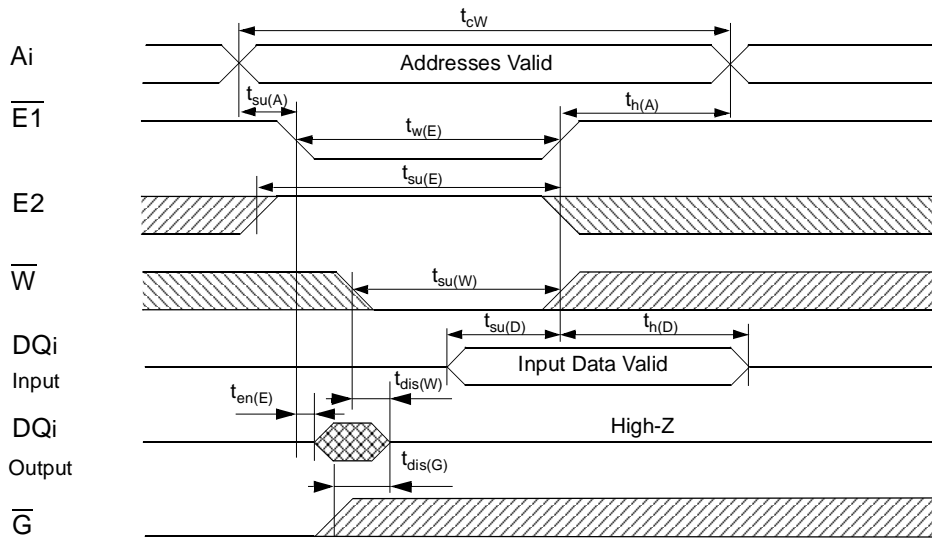


\* The same applies to  $\overline{E1}$

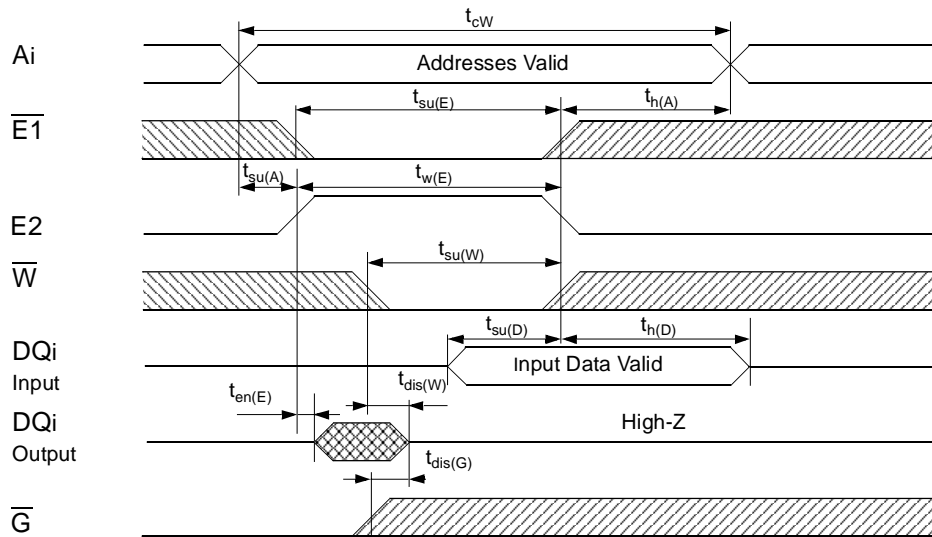
Write Cycle1:  $\overline{W}$ -controlled



Write Cycle 2:  $\overline{E1}$ -controlled



Write Cycle 3 (E2-controlled)



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