M51C67
HIGH-SPEED CHMOS 16,384 x 1 BIT STATIC RAM

Military

	M51C67-35	-45	-55
Max Access Time (ns)	35	45	55
Max Active Current (mA)	100	100	100
Max Standby Current (mA)	10	10	10

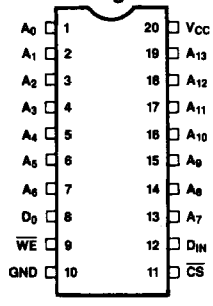
- **Double Metal CHMOS III Technology**
- **Completely Static Memory–No Clock**
- **Equal Access and Cycle Times**
- **Single +5V Supply**
- **Power Down**
- **0.8–2.0V Output Timing Reference**
- **High Density 20-Pin Package**
- **Directly TTL Compatible–All Inputs and Output**
- **Separate Data Input and Output**
- **Three-State Output**
- **M2147H Upgrade**
- **Military Temperature Range: −55°C to +125°C (T_C)**

The Intel M51C67 is a 16,384-bit static random access memory organized as 16,384 words by 1 bit. This memory is fabricated using Intel's high performance double metal CHMOS III technology, with a full CHMOS 6T cell. This state of the art technology with HMOS III scaled transistors brings high performance to CMOS Static RAMs. Intel's CHMOS III process also provides superior radiation tolerance for applications with stringent radiation requirements. Contact your local sales office for the latest information. The design of the M51C67 offers a 4× density improvement over the industry standard M2147H with compatible performance. The M51C67 offers the automatic power-down feature pioneered by the Intel M2147H.

$\overline{CS}$ controls the power-down feature. In no more than a cycle time after $\overline{CS}$ goes high (deselecting the M51C67), the part automatically reduces its power requirements and remains in this low power standby mode as long as $\overline{CS}$ remains high. This device feature results in system power savings as great as 90% in larger systems where the majority of devices are deselected.

The M51C67 is placed in a 20-pin 300 mil package configured with the industry standard 16K x 1 pinout. It is directly TTL compatible in all respects: inputs, output; and a single +5V supply. The data is read out nondestructively and has the same polarity as the input data. A data input and a separate three-state output are used.

Pin Configuration



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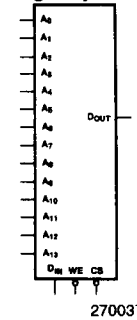
Logic Symbol



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Pin Names

A_0–A_{13}	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
D_{IN}	Data Input
D_{OUT}	Data Output

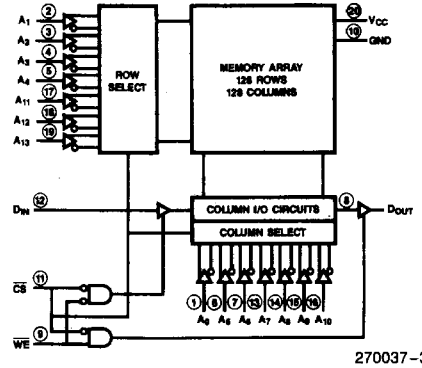

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Figure 1. M51C67 Block Diagram

Truth Table

$\overline{CS}$	$\overline{WE}$	Mode	Output	Power
H	X	Not Selected	High Z	Standby
L	L	Write	High Z	Active
L	H	Read	D_{OUT}	Active

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Order Number: 270037-005

ABSOLUTE MAXIMUM RATINGS*

Case Temperature Under Bias . . . −65°C to +135°C
Storage Temperature Cerdip . . . . −65°C to +150°C
Voltage on Any Pin with Respect to Ground . . . . . −0.5V(1) to +7V
D.C. Continuous Output Current . . . . . 20 mA
Power Dissipation 1.0W

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

Operating Conditions

Symbol	Description	Min	Max	Unit
T_C	Case Temperature (Instant On)	−55	+125	°C
V_{CC}	Digital Supply Voltage	4.50	5.50	V

D.C. AND OPERATING CHARACTERISTICS (Over Specified Operating Conditions)

Symbol	Parameter	Min	Max	Unit	Test Conditions
I_{LI}	Input Load Current (All Input Pins)		5	µA	V_{CC} = Max, V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current		20	µA	$\overline{CS}$ = V_{IH}, V_{CC} = Max V_{OUT} = GND to 4.5V
I_{CC}	Operating Current		100	mA	V_{CC} = Max, $\overline{CS}$ = V_{IL} Outputs Open, T_{cycle} = Min
I_{SB}	Standby Current		10	mA	V_{CC} = Min to Max, $\overline{CS}$ = V_{IH}
V_{IL}	Input Low Voltage	−0.5(1)	0.8	V	(Note 4)
V_{IH}	Input High Voltage	2.2	6.0	V	
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 12 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = −8 mA

NOTES:
1. During transitions, the inputs may undershoot to −2.0V for periods less than 20 ns.

CAPACITANCE T_C = 25°C, f = 1.0 MHz

Symbol	Parameter	Max	Unit	Conditions
C_{in}	Input Capacitance	5	pF	V_{in} = 0V
C_{out}	Output Capacitance	7	pF	V_{out} = 0V

A.C. TEST CONDITIONS

Input Pulse Levels . . . . . GND to 3.0V
Input Rise and Fall Times . . . . . 5 ns
Input Timing Reference Level 1.5V
Output Timing Reference Levels 0.8V–2.0V
Output Load . . . . . See Figures 2, 3

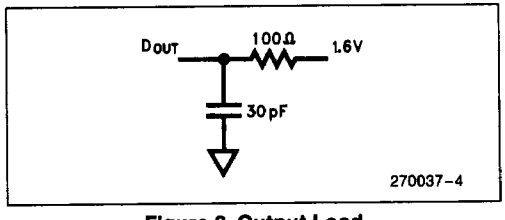

Figure 2. Output Load

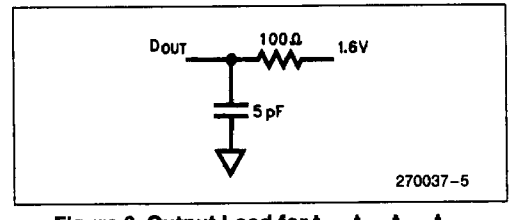

Figure 3. Output Load for t_{Hz}, t_{Lz}, t_{wz}, t_{ow}

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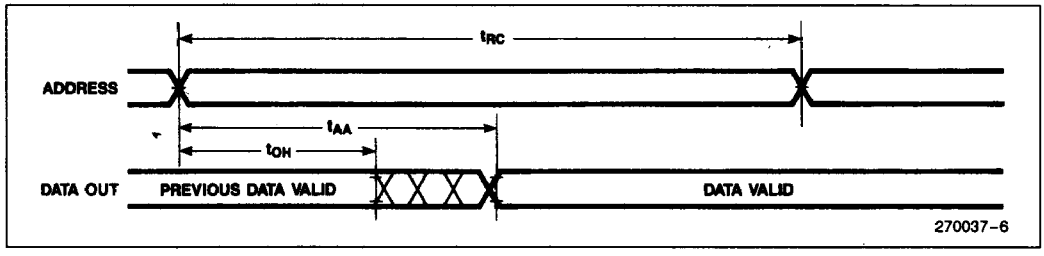
A.C. CHARACTERISTICS (Over Specified Operating Conditions)

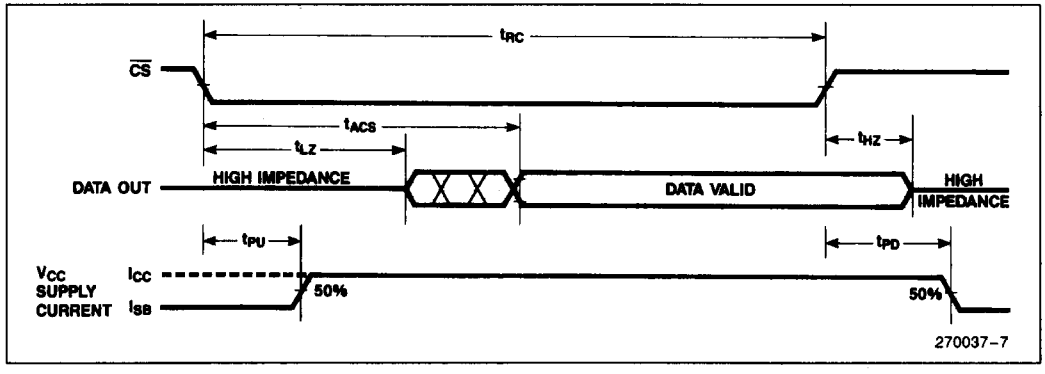
READ CYCLE

Symbol	Parameter	M51C67-35		M51C67-45		M51C67-55		Unit
		Min	Max	Min	Max	Min	Max	
t_{RC}(1)	Read Cycle Time	35		45		55		ns
t_{AA}	Address Access Time		35		45		55	ns
t_{ACS}	Chip Select Access Time		35		45		55	ns
t_{OH}	Output Hold from Address Change	0		0		0		ns
t_{LZ}(2, 3)	Chip Selection to Output in Low Z	0		0		0		ns
t_{HZ}(2, 3)	Chip Deselection to Output in High Z	0	25	0	25	0	25	ns
t_{PU}	Chip Selection to Power Up Time	0		0		0		ns
t_{PD}	Chip Deselection to Power Down Time		35		35		35	ns

READ CYCLE NO. 1 (4, 5)



READ CYCLE NO. 2 (4, 6)



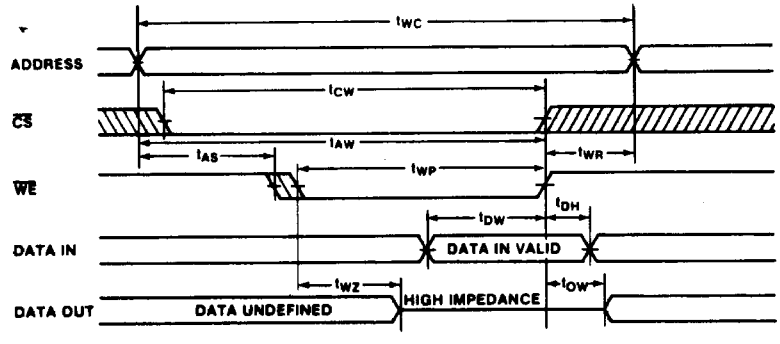
NOTES:
1. All Read Cycle timings are referenced from the last valid address to the first transitioning address.
2. At any given temperature and voltage condition, t_{HZ} max. is less than t_{LZ} min. both for a given device and from device to device.
3. Transition is measured at ±500 mV from steady state voltage with specified loading in Figure 3.
4. $\overline{WE}$ is high for Read Cycles.
5. Device is continuously selected, $\overline{CS}$ = V_{IL}.
6. Addresses valid prior to or coincident with $\overline{CS}$ transition low.

A.C. CHARACTERISTICS (Continued)

WRITE CYCLE

Symbol	Parameter	M51C67-35		M51C67-45		M51C67-55		Units
		Min	Max	Min	Max	Min	Max	
t_{WC}(1)	Write Cycle Time	35		45		55		ns
t_{CW}	Chip Selection to End of Write	30		35		45		ns
t_{AW}	Address Valid to End of Write	30		35		45		ns
t_{AS}	Address Setup Time	5		5		5		ns
t_{WP}	Write Pulse Width	25		30		40		ns
t_{WR}	Write Recovery Time	0		0		0		ns
t_{DW}	Data Valid to End of Write	25		25		25		ns
t_{DH}	Data Hold Time	5		5		5		ns
t_{WZ}(2)	Write Enabled to Output in High Z	0	20	0	25	0	25	ns
t_{OW}(2)	Output Active from End of Write	0		0		0		ns

WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED) (3)



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NOTES:
1. All Write Cycle timings are referenced from the last valid address to the first transitioning address.
2. Transition is measured at ±500 mV from steady-state voltage with specified loading in Figure 3.

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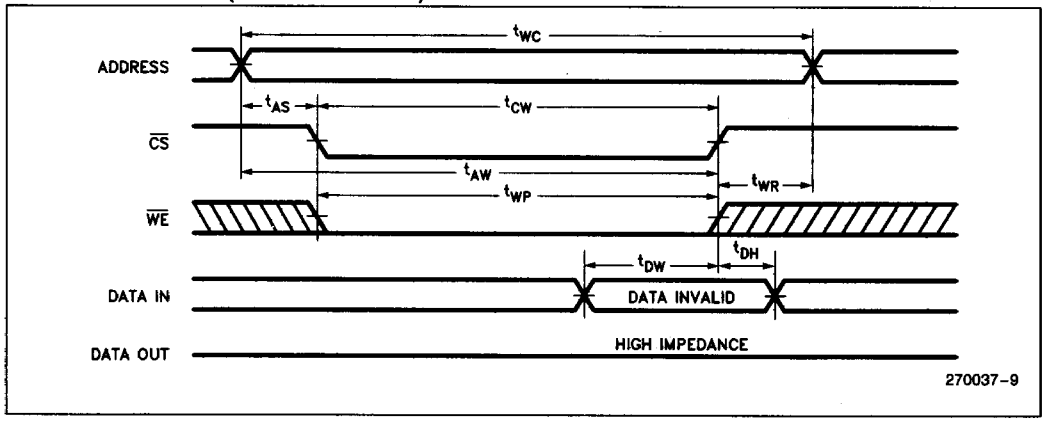
A.C. CHARACTERISTICS (Continued)

WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED) (3)



NOTE:
3. $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.