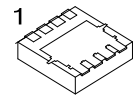
13.3A, 30V N-CHANNEL POWER MOSFET



DFN-8(3x3)

■ DESCRIPTION

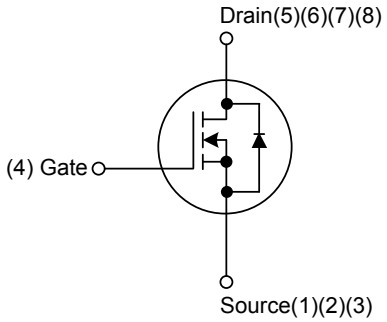
The UTC **UNA03R085M** is an N-channel MOSFET, it uses UTC's advanced technology to provide the customers with a minimum on state resistance, high switch speed and low gate charge.

The UTC **UNA03R085M** is suitable for notebook battery power management and DC-DC buck converters.

■ FEATURES

* $R_{DS(ON)}$ < 8.5mΩ @ V_{GS}=10V, I_D=13.3A
  $R_{DS(ON)}$ < 14mΩ @ V_{GS}=4.5V, I_D=10.6A
* High switch speed
* Low gate charge

■ SYMBOL



■ ORDERING INFORMATION

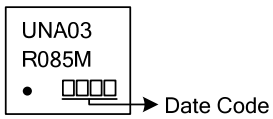
Ordering Number	Package	Pin Assignment								Packing
		1	2	3	4	5	6	7	8	
UNA03R085MG-K08-3030-R	DFN-8(3×3)	S	S	S	G	D	D	D	D	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

UNA03R085MG-K08-3030-R

(1)Packing Type	(1) R: Tape Reel
(2)Package Type	(2) K08-3030: DFN-8(3×3)
(3)Green Package	(3) G: Halogen Free and Lead Free

■ MARKING



■ ABSOLUTE MAXIMUM RATINGS (T_A=25°C, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	30	V
Gate-Source Voltage		V_{GSS}	±20	V
Drain Current	Continuous (Package limited) T_C=25°C	I_D	16	A
	Continuous T_A=25°C (Note 1a)		13.3	A
	Pulsed	I_{DM}	40	A
Single Pulse Avalanche Energy (Note 2)		E_{AS}	58	mJ
Power Dissipation	T_C=25°C	P_D	29	W
	T_A=25°C (Note 1a)		2.3	W
Junction Temperature		T_J	-55~+150	°C
Storage Temperature Range		T_{STG}	-55~+150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ THERMAL RESISTANCES CHARACTERISTICS

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient (Note 1a)	θ_{JA}	53	°C/W
Junction-to-Case	θ_{JC}	4.3	°C/W

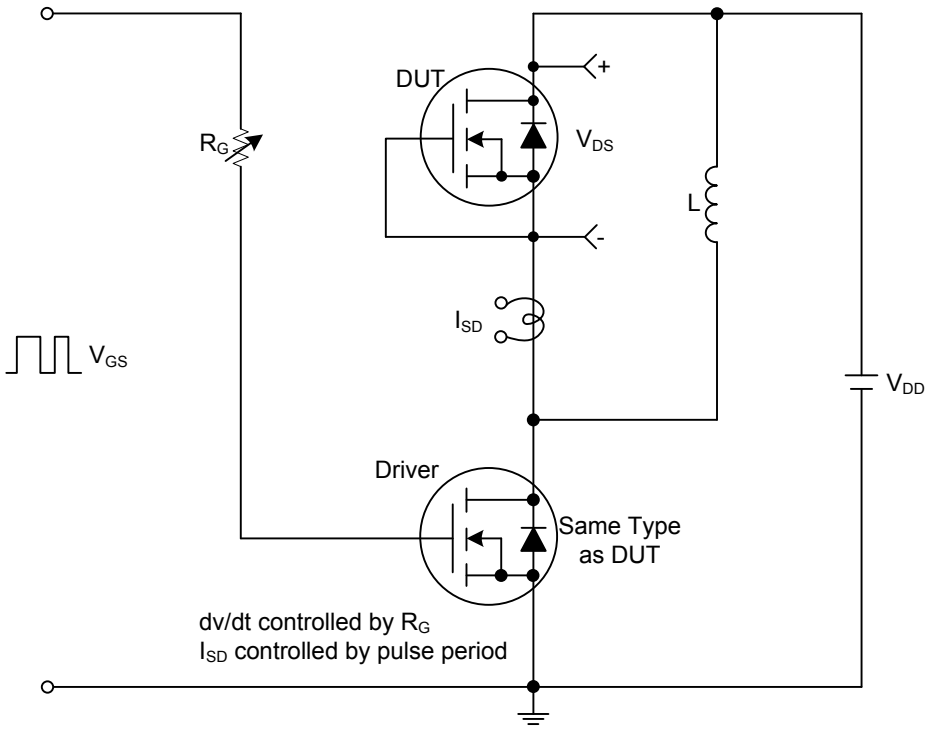
Notes: 1. θ_{JA} is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. θ_{JC} is guaranteed by design while θ_{CA} is determined by the user's board design.
a. 50°C/W when mounted on a 1 in^2 pad of 2 oz copper.
b.125°C/W when mounted on a minimum pad of 2 oz copper.
2. E_{AS} of 58mJ is based on starting T_J=25°C, L=1mH, I_{AS}=10.8A, V_{DD}=27V, V_{GS}=10V. 100% test at L=0.1mH, I_{AS}=21A.

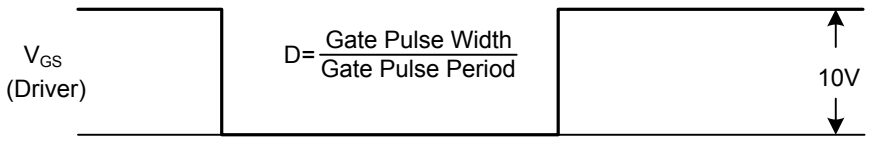
■ ELECTRICAL CHARACTERISTICS (T_J=25°C, unless otherwise specified)

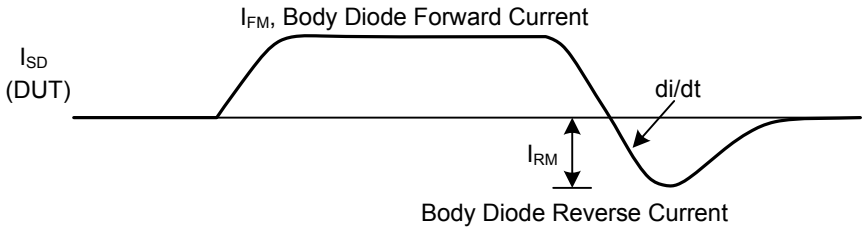
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=1mA, V_{GS}=0V	30			V
Breakdown Voltage Temperature Coefficient	$\frac{\Delta BV_{DSS}}{\Delta T_J}$	I_D=250uA, Referenced to 25°C		16		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=24V, V_{GS}=0V			1	μA
		V_{DS}=24V, V_{GS}=0V, T_J=125°C			250	μA
Gate-Source Leakage Current Forward	I_{GSS}	V_{GS}=20V, V_{DS}=0V			100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS}=V_{GS}, I_D=250uA	1.2	1.9	3.0	V
Gate Threshold Voltage Temperature Coefficient	$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	I_D=250uA, Referenced to 25°C		-6		mV/°C
Static Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=13.3A		7.2	8.5	mΩ
		V_{GS}=4.5V, I_D=10.6A		9.5	14	mΩ
Forward Transconductance	g_{FS}	V_{DD}=5V, I_D=13.3A		60		S
DYNAMIC PARAMETERS						
Input Capacitance	C_{ISS}	V_{GS}=0V, V_{DS}=15V, f=1.0MHz		1260	1680	pF
Output Capacitance	C_{OSS}			480	635	pF
Reverse Transfer Capacitance	C_{RSS}			65	100	pF
Gate Resistance	R_G			0.9	2.4	Ω
SWITCHING PARAMETERS						
Total Gate Charge	Q_G	V_{GS}=0V~4.5V, V_{DD}=15V, I_D=13.3A		4	10	nC
Gate to Source Charge	Q_{GS}			21	33	nC
Gate to Drain Charge	Q_{GD}			3	10	nC
Turn-ON Delay Time	$t_{D(ON)}$	V_{GS}=10V, V_{DD}=15V, I_D=13.3A, R_{GEN}=6Ω		9	18	ns
Rise Time	t_R			4	10	ns
Turn-OFF Delay Time	$t_{D(OFF)}$			21	33	ns
Fall-Time	t_F			3	10	ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS						
Maximum Body-Diode Continuous Current (Note)	I_S				1.9	A
Source to Drain Diode Forward Voltage	V_{SD}	V_{GS}=0V, I_S=13.3A (Note 2)		0.86	1.2	V
		V_{GS}=0V, I_S=1.9A (Note 2)		0.75	1.2	V
Reverse Recovery Time	t_{rr}	I_F=13.3A, di/dt=100A/μs		24	38	ns
Reverse Recovery Charge	Q_{rr}			7	14	nC

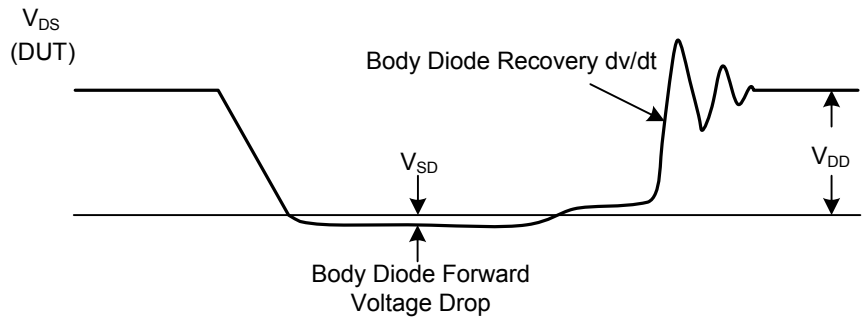
Note: Pulse Test: Pulse width < 300μs, Duty cycle < 2.0%.

■ TEST CIRCUITS AND WAVEFORMS



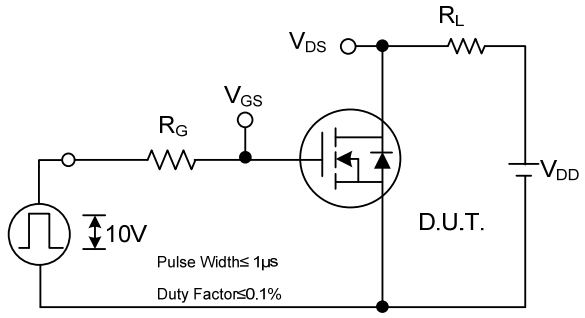




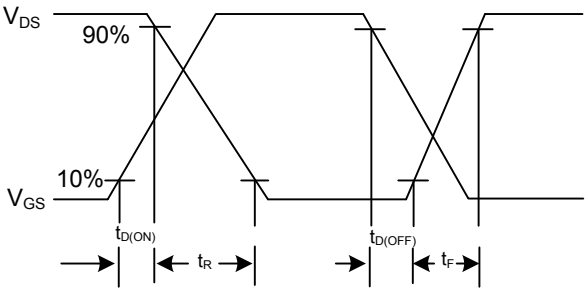


Peak Diode Recovery dv/dt Test Circuit and Waveforms

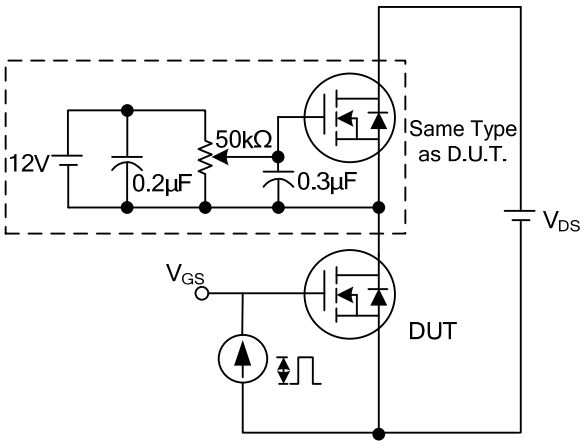
■ TEST CIRCUITS AND WAVEFORMS (Cont.)



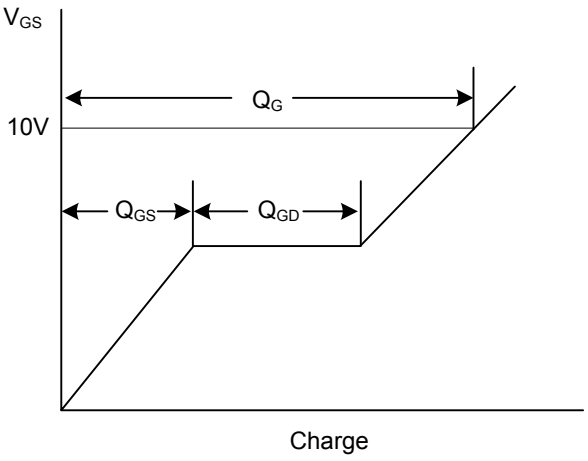
Switching Test Circuit



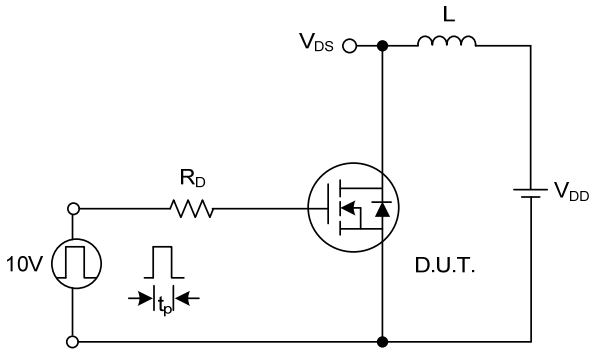
Switching Waveforms



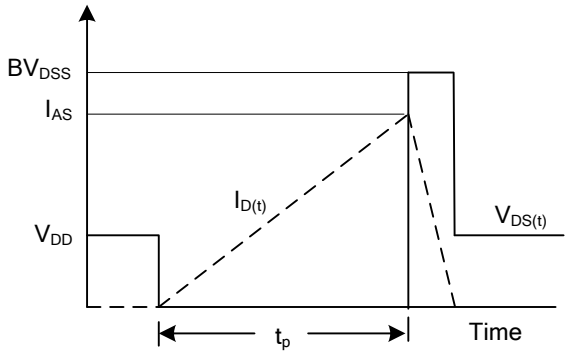
Gate Charge Test Circuit



Gate Charge Waveform



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms