PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

M5M52B88AJ-(6),-8,-10

262144-BIT (32768-WORD BY 8-BIT) BiCMOS STATIC RAM

DESCRIPTION

The M5M52B88A is a family of 32768-word by 8-bit static RAMs, fabricated with the high-performance BiCMOS process and designed for high-speed application. These devices operate on a single 5V supply, and are directly TTL compatible. They include a power-down feature as well.

FEATURES

- Fast access time (M5M52B88AJ-6) ..... 6ns(max)
  M5M52B88AJ-8 ..... 8ns(max)
  M5M52B88AJ-10 ..... 10ns(max)
- Low power dissipation Active ..... 450mW(typ)
  Stand by ..... 50mW(typ)
- Power down by $\overline{S}$
- Center power (Vcc, GND) pin out
- Single 5V power supply
- Fully static operation
- Requires neither external clock nor refreshing
- All inputs and outputs are directly TTL compatible
- Easy memory expansion by chip-select ($\overline{S}$) input
- Output enable ($\overline{OE}$) prevents data contention in the I/O bus
- All address inputs are changeable with each other

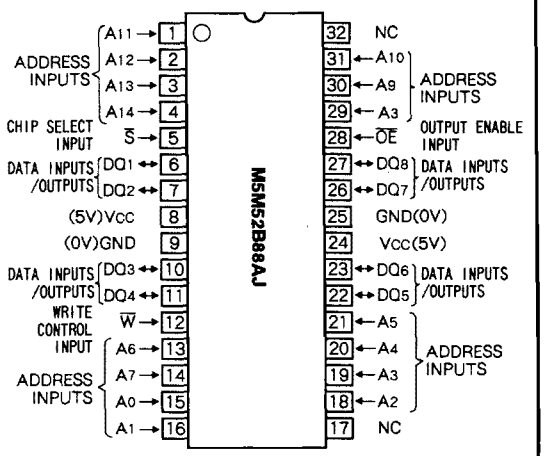
APPLICATION

High-speed memory systems

FUNCTION

A write operation is executed during the $\overline{S}$ low, and $\overline{W}$ low overlap time. In this period, address signals must be stable. When $\overline{W}$ is low, the DQ terminal is maintained in the high impedance state.

PIN CONFIGURATION (TOP VIEW)



Outline 32P0J(SOJ)

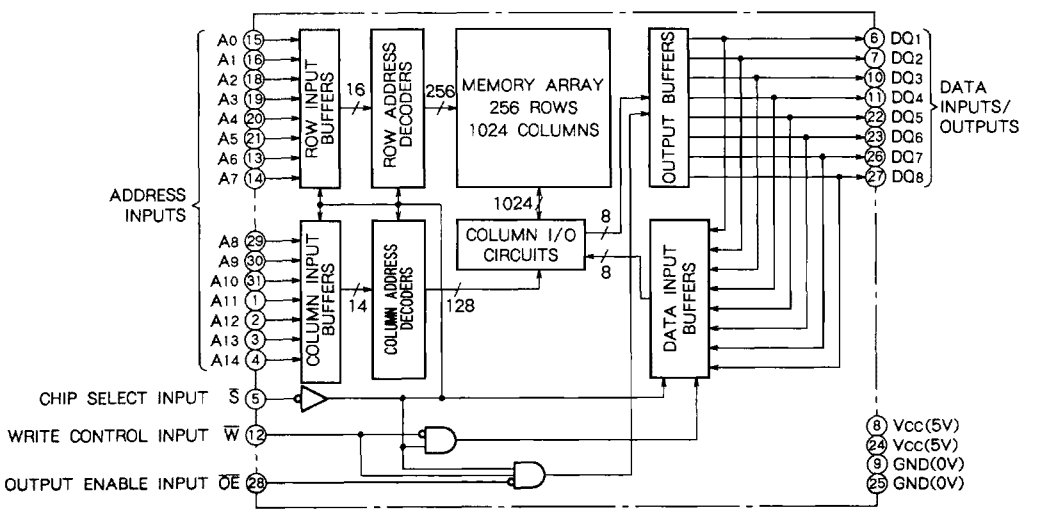
NC : NO CONNECTION

In a read operation, after setting $\overline{W}$ to high, $\overline{S}$ to low, and $\overline{OE}$ to low if the address signals are stable, the data is available at the DQ terminal.

When $\overline{S}$ is high, the chip is in the non-selectable state, disabling both reading and writing. In this case the output is in the floating (high-impedance) state, useful for OR-ties with other devices.

Single $\overline{S}$ controls the power-down feature. When $\overline{S}$ goes high, power dissipation is reduced extremely. The access time from $\overline{S}$ is equivalent to the address access time.

BLOCK DIAGRAM



MODE SELECTION

$\overline{S}$	$\overline{W}$	$\overline{OE}$	Mode	Data input/output	Icc
H	X	X	Non selection	High-impedance	Stand by
L	L	X	Write	D_{in}	Active
L	H	L	Read	D_{out}	Active
L	H	H		High-impedance	Active

H : V_{IH} L : V_{IL} X : V_{IH} or V_{IL}

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to GND	−3.5* ~7	V
V_I	Input voltage		−3.5* ~7	V
V_O	Output voltage		−3.5* ~7	V
P_d	Maximum power dissipation		1	W
T_{opr}	Operating temperature		0~70	℃
$T_{stg(bias)}$	Storage temperature(bias)		−10~85	℃
T_{stg}	Storage temperature		−65~150	℃

* Pulse width ≦ 10ns, In case of DC : −0.5V

DC ELECTRICAL CHARACTERISTICS (Ta = 0~70℃, V_{CC} = 5V ± 10%, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ	Max	
V_{IH}	High-level input voltage			2.2		V_{CC}+0.3	V
V_{IL}	Low-level input voltage			−0.5*		0.8	V
V_{OH}	High-level output voltage	I_{OH} = −4mA		2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8mA				0.4	V
I_I	Input current	V_I = 0~V_{CC}				2	μA
$\lvert I_{OZ} \rvert$	Off-state output current	$V_{I(\overline{S})} = V_{IH}$, V_O = 0~V_{CC}				10	μA
I_{CC1}	Supply current from V_{CC}	$V_{I(\overline{S})} = V_{IL}$ Output open	AC(6ns cycle)			210	mA
			AC(8ns cycle)			195	
			AC(10ns cycle)			185	
			DC		90	115	
I_{CC2}	Stand by current	$V_{I(\overline{S})} = V_{IH}$	AC(6ns cycle)			80	mA
			AC(8, 10ns cycle)			70	
			Other $V_I \geqq V_{IH}$ or $\leqq V_{IL}$			50	
I_{CC3}	Stand by current	$V_{I(\overline{S})} = V_{CC} - 0.2V$ Other $V_I \leqq 0.2V$ or $V_I \geqq V_{CC} - 0.2V$				10	mA

Note 1. Current flow into an IC is positive, out is negative.
* −3.0V in case of AC (Pulse width ≦ 6ns)

CAPACITANCE

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
C_I	Input capacitance	V_I = GND, V_I = 25mVrms, f = 1MHz			5	pF
C_O	Output capacitance	V_O = GND, V_O = 25mVrms, f = 1MHz			7	pF

AC ELECTRICAL CHARACTERISTICS (Ta = 0~70℃, V_{CC} = 5V ± 10%, unless otherwise noted)

(1) MEASUREMENT CONDITIONS

Input pulse levels ····· V_{IH} = 3V, V_{IL} = 0V
Input rise and fall time ····· 3ns
Input timing reference levels ····· V_{IH} = 1.5V, V_{IL} = 1.5V
Output timing reference levels ··· V_{OH} = 1.5V, V_{OL} = 1.5V
Output loads ····· Fig.1, Fig.2

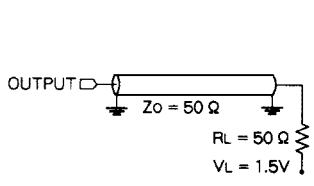


Fig.1 Output load

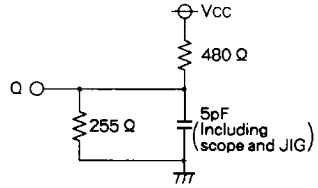


Fig. 2 Output load for t_{en}, t_{dis}

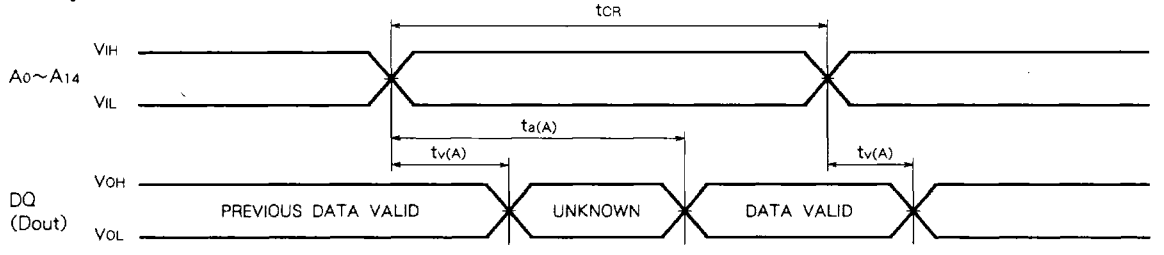
MITSUBISHI ELECTRIC

(2) READ CYCLE

Symbol	Parameter	Limits						Unit
		(M5M52B88A-6)		M5M52B88A-8		M5M52B88A-10		
		Min	Max	Min	Max	Min	Max	
t_{CR}	Read cycle time	6		8		10		ns
$t_{a(A)}$	Address access time		6		8		10	ns
$t_{a(S)}$	Chip select access time		6		8		10	ns
$t_{a(OE)}$	Output enable access time		3		4		5	ns
$t_{v(A)}$	Data valid time after address change	2.5		3		4		ns
$t_{en(S)}$	Output enable time from($\overline{S}$)	2.5		3		4		ns
$t_{en(OE)}$	Output enable time from($\overline{OE}$)	2		3		3		ns
$t_{dis(S)}$	Output disable time from($\overline{S}$)	0	3	0	4	0	5	ns
$t_{dis(OE)}$	Output disable time from($\overline{OE}$)	0	3	0	4	0	5	ns
t_{PU}	Power-up time after chip selection	0		0		0		ns
t_{PD}	Power-down time after chip selection		6		8		10	ns

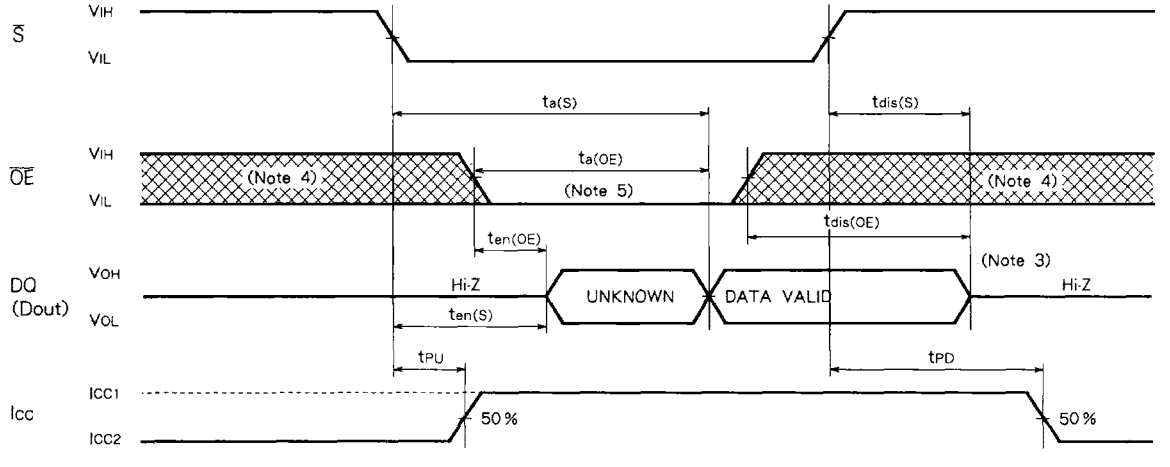
(3) TIMING DIAGRAMS FOR READ CYCLE

Read cycle 1



$\overline{W}$ = H $\overline{S}$ = L $\overline{OE}$ = L

Read cycle 2 (Note 2)



$\overline{W}$ = H

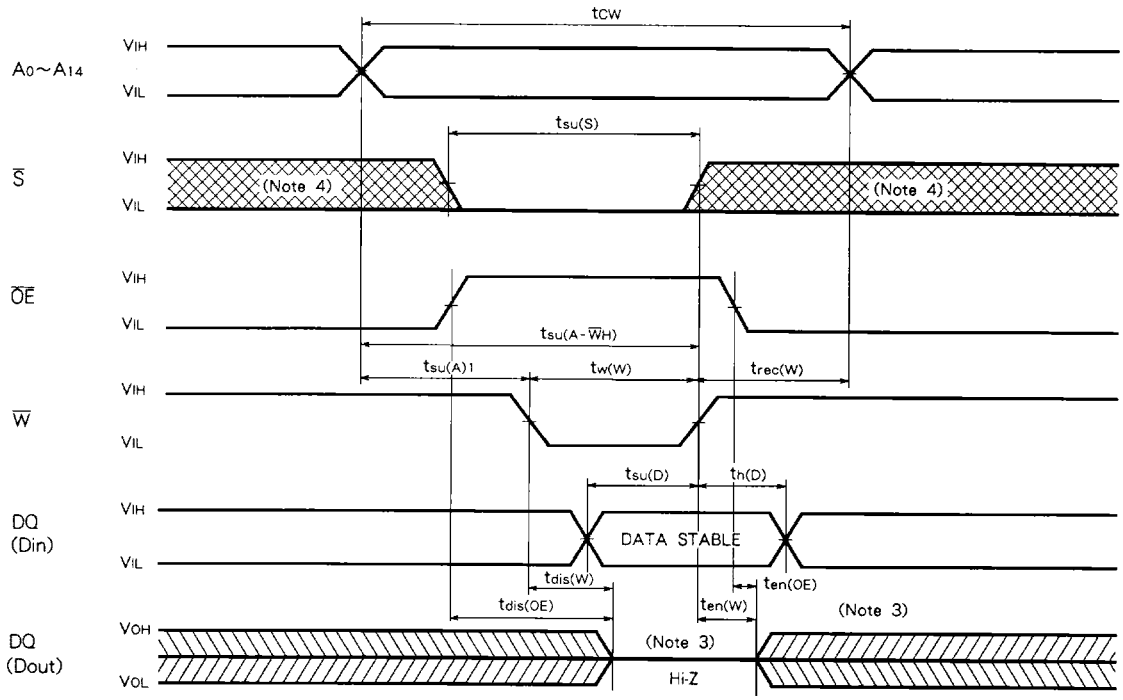
Note 2. Addresses valid prior to or coincident with $\overline{S}$ transition low.
3. Transition is measured ± 500mV from steady state voltage with specified loading in Figure2.
4. Hatching indicates the state is don't care.
5. Addresses and $\overline{S}$ valid prior $\overline{OE}$ transition low by ($t_{a(A)} - t_{a(OE)}$, $t_{a(S)} - t_{a(OE)}$).

(4) WRITE CYCLE

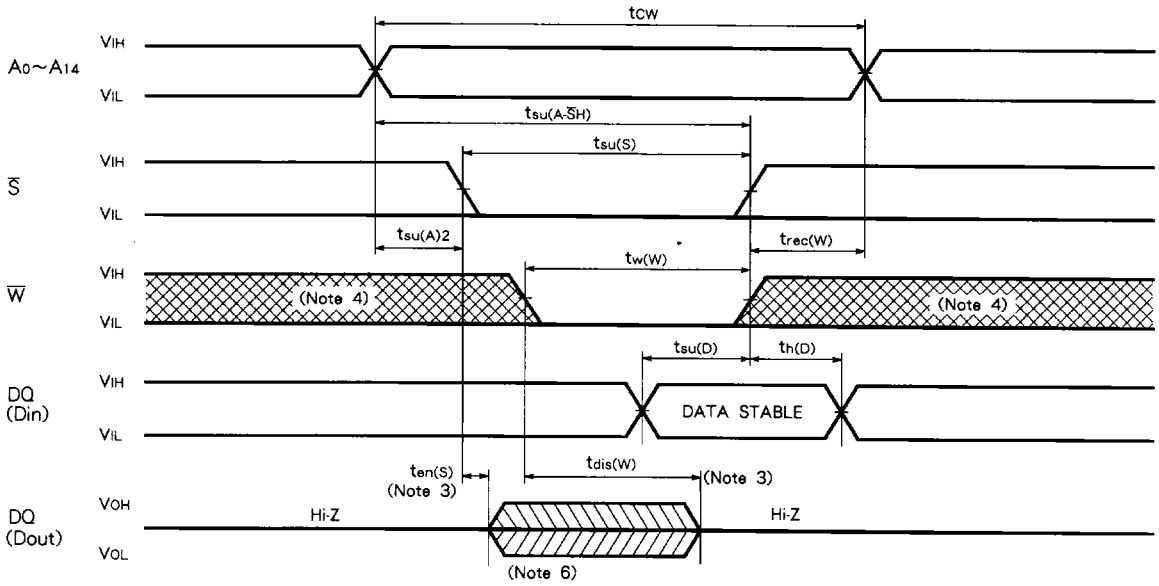
Symbol	Parameter	Limits						Unit
		(M5M52B88A-6)		M5M52B88A-8		M5M52B88A-10		
		Min	Max	Min	Max	Min	Max	
t_{CW}	Write cycle time	6		8		10		ns
$t_{su(S)}$	Chip select setup time	6		7		9		ns
$t_{su(A)1}$	Address setup time($\overline{W}$)	0		0		0		ns
$t_{su(A)2}$	Address setup time($\overline{S}$)	0		0		0		ns
$t_{w(W)}$	Write pulse width	5		7		9		ns
$t_{rec(W)}$	Write recovery time	0		0		0		ns
$t_{su(D)}$	Data setup time	3		4		5		ns
$t_{h(D)}$	Data hold time	0		0		0		ns
$t_{dis(W)}$	Output disable time from $\overline{W}$	0	3	0	4	0	5	ns
$t_{dis(OE)}$	Output disable time from $\overline{OE}$	0	3	0	4	0	5	ns
$t_{en(W)}$	Output enable time from $\overline{W}$	0		0		0		ns
$t_{en(OE)}$	Output enable time from $\overline{OE}$	0		0		0		ns
$t_{su(A-\overline{W}H)}$	Address to $\overline{W}$ high	5		7		9		ns
$t_{su(A-\overline{S}H)}$	Address to $\overline{S}$ high	5		7		9		ns

(5) TIMING DIAGRAMS FOR WRITE CYCLE

Write cycle 1 ($\overline{W}$ control mode)



Write cycle 2 ($\overline{S}$ control mode)



Note 6. When the falling edge of $\overline{W}$ is simultaneous or prior to the falling edge of $\overline{S}$, the output is maintained in the high impedance.