PERICOM

Clock Generation for Pentium II Processor with Direct RAMBUS Memory

Features

- Three copies of CPU Clock @ 133/100 MHz
- Ten copies of PCI Clock (Synchronous w/CPU Clock) including one free running PCI clock.
- One CPU/2 output @ CPU/2 frequency for synchronous memory reference
- Three copies of fixed frequencies 3.3V Clock @ 66 MHz
- One copy of the APIC Clock @ 16.667 MHz, synchronous to CPU Clock
- One copy of 48 MHz Clock
- Two copies of REF. Clock@14.13818 MHz
- Ref.14.31818 MHz Xtal Oscillator Input
- CPU Clock Frequency selection pin for selecting 133 MHz or 100 MHz operation
- Power Management Control Input Pins
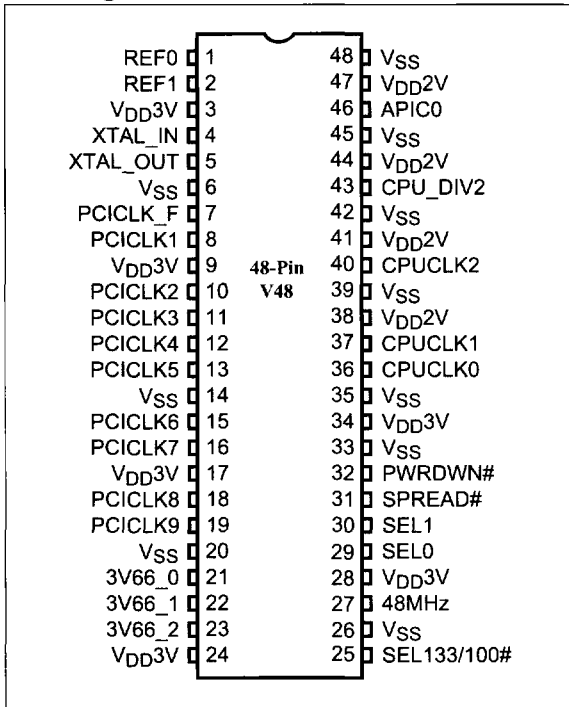- Spread Spectrum enable/disable pin
- 48-pin SSOP (V48) package

Description

The PI6C133 is a low-skew, low-jitter 133 MHz clock generator for Intel Architecture for PC99-compliant platforms. The PI6C133 is specifically designed to meet all the clocking requirements for 133 MHz and 100 MHz desktop with high performance and lower power features.
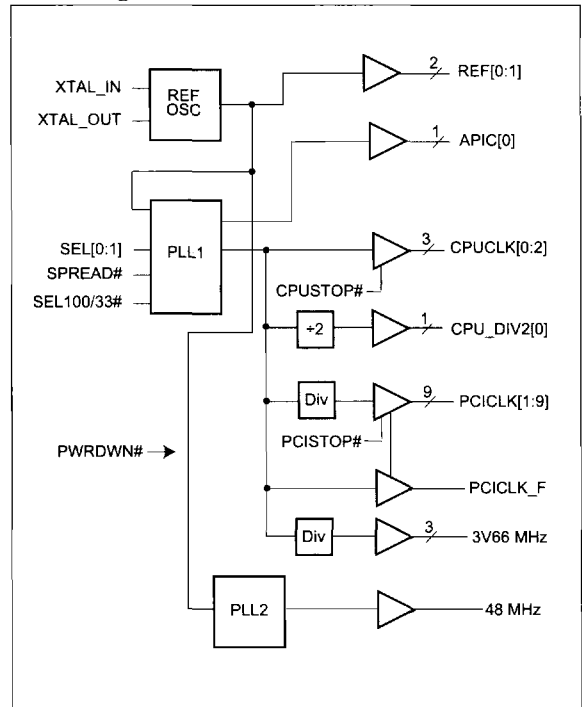
Split power supplies of 2.5V and 3.3V are used to reduce power consumption, minimize noise and to ensure CPU independence. The 2.5V supply is used to power CPUCLK clocks to the processor module and for CPUDIV2 for Rambus DRCG clock. 2.5V signalling is compliant to the JEDEC standard 8-X. The rest of circuitry is powered by 3.3V supply.

Key features such as power management and spread spectrum function are fully supported. PWRDWN# signal will turn off all internal circuits and keep all outputs to low state to bring the power consumption less than 100mA. For less stringent power requirement, CPUSTOP# will turn off CPUCLK and 3V66 outputs instantaneously to support PC99 "ON NOW" initiative. Spread spectrum function can be optionally disabled by pulling SPREAD# pin to a HIGH state.

Pin Configuration

	48-Pin V48	
REF0	1	48 V$_{SS}$
REF1	2	47 V$_{DD}$2V
V$_{DD}$3V	3	46 APIC0
XTAL_IN	4	45 V$_{SS}$
XTAL_OUT	5	44 V$_{DD}$2V
V$_{SS}$	6	43 CPU_DIV2
PCICLK_F	7	42 V$_{SS}$
PCICLK1	8	41 V$_{DD}$2V
V$_{DD}$3V	9	40 CPUCLK2
PCICLK2	10	39 V$_{SS}$
PCICLK3	11	38 V$_{DD}$2V
PCICLK4	12	37 CPUCLK1
PCICLK5	13	36 CPUCLK0
V$_{SS}$	14	35 V$_{SS}$
PCICLK6	15	34 V$_{DD}$3V
PCICLK7	16	33 V$_{SS}$
V$_{DD}$3V	17	32 PWRDWN#
PCICLK8	18	31 SPREAD#
PCICLK9	19	30 SEL1
V$_{SS}$	20	29 SEL0
3V66_0	21	28 V$_{DD}$3V
3V66_1	22	27 48MHz
3V66_2	23	26 V$_{SS}$
V$_{DD}$3V	24	25 SEL133/100#

Block Diagram

Pin Description

Pin	Symbol	I/O	Functional Description
1,2	REF [0:1]	O	3.3V 14.318 MHz clock output
4	XTAL_IN	I	14.318 MHz Crystal input
5	XTAL_OUT	O	14.318 MHz Crystal output
7	PCICLK_F	O	3.3V Free Running PCI clock
8,10,11,12,13,15, 16,18,19	PCICLK[1-9]	O	3.3V PCI Clock Outputs
21,22,23	3V66 [0-2]	O	3.3V Fixed 66 MHz Clock Outputs
25	SEL133/100#	I	3.3 LVTTL compatible input for 133 MHz or 100 MHz CPU Outputs. H = 133 MHz L = 100 MHz
27	48MHz	O	3.3V Fixed 48 MHz Clock output
29,30	SEL[0-1]	I	3.3 LVTTL compatible input for logic selection function
31	SPREAD#	I	3.3 LVTTL compatible input. Enables spread spectrum mode when held LOW
32	PWRDWN#	I	3.3 LVTTL compatible input. Device Enters Powerdown mode when held LOW
36,37,40	CPUCLK[0-2]	O	2.5V Host Bus Clock output. 133 MHz or 100 MHz depending on state of SEL133/100#
43	CPU_DIV2	O	2.5V output running at 1/2 CPU (Host bus) clock frequency. 66 MHz or 50 MHz depending on state SEL133/100#
46	APIC0	O	2.5V Clock output running divide synchonous with the CPU (Host bus) clock frequency. Fixed 16.67 MHz limit. If CPU = 133 MHz, APIC = CPU/8 If CPU = 100 MHz, APIC = CPU/6
3,9,17,24,28,34	V$_{DD}$3V	3.3V Power	3.3V power supply
6,14,20,26,33,35, 39,42,45,48	V$_{SS}$	V$_{SS}$	Ground
41,44,47	V$_{DD}$2V	2.5V Power	2.5V power

IOAPIC Clock Outputs Must Be Synchronous with CPUCLK

The IOAPIC clocks, which were previously obtained by buffering the input reference crystal frequency, are now required to be synchronous with the CPUCLK outputs. The IOAPIC voltage will track that of the Host bus and will have maximum frequency of 16.667 MHz. The IOAPIC clocks will be derived by dividing the CPUCLK outputs by eight when the Host bus is 133.33 MHz, and by six when the Host bus is 100 MHz. IOAPIC clocks will lag the Host bus clocks by 1.5 - 4.0ns at the maximum device load of 20pF.

PI6C133 Select Functions

SEL133/100#	SEL1	SEL0	Function
0	0	0	All outputs Tri-State
0	0	1	(Reserved)
0	1	0	Active 100 MHZ, 48 MHz PLL inactive
0	1	1	Active 100 MHZ, 48 MHz PLL active
1	0	0	Test Mode
1	0	1	(Reserved)
1	1	0	Active 133 MHZ, 48 MHz PLL inactive
1	1	1	Active 133 MHZ, 48 MHz PLL active

PI6C133 Truth Table

SEL 133/100#	SEL1	SEL0	CPU	CPU_div2	3V66	PCI	48 MHz	REF	IOAPIC	Notes
0	0	0	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	1
0	0	1	n/a	n/a	n/a	n/a	n/a	n/a	n/a	
0	1	0	100 MHz	50 MHz	66 MHz	33 MHz	Hi-Z	14.318 MHz	16.67 MHz	2
0	1	1	100 MHz	50 MHz	66 MHz	33 MHz	48 MHz	14.318 MHz	16.67 MHz	3,6,7
1	0	0	TCLK/2	TCLK/4	TCLK/4	TCLK/8	TCLK/2	TCLK	TCLK/16	4,5
1	0	1	n/a	n/a	n/a	n/a	n/a	n/a	n/a	
1	1	0	133 MHz	66 MHz	66 MHz	33 MHz	Hi-Z	14.318 MHz	16.67 MHz	2
1	1	1	133 MHz	66 MHz	66 MHz	33 MHz	48 MHz	14.318 MHz	16.67 MHz	3,6,7

Notes:
1. Required for board-level "bed of nails" testing.
2. 48 MHz PLL disabled to reduce component jitter.
   48 MHz outputs are held H-Z instead of driven to a LOW state.
3. "Normal" mode of operation.
4. TCLK is a test clock over driven on the XTAL_IN input during test mode. TCLK mode is based on 133 MHz CPU select logic.
5. For DC output impedance verification.
6. Range of reference frequency allowed is min = 14.316 nominal = 14.31818 MHz, max = 14.32 MHz.
7. Frequency accuracy of 48 MHz must be +167PPM to match USB default.

The power-down controller provides a signal that is latched with its own copy of the PCI clock.

Clock sequencing always guarantees full clock timing parameters after the system has initially powered up, except where noted. During power-up and power-down operations using the PWR_DWN# select pin, partial clocks are not allowed and all clock timing parameters are met except for the following: the first clock pulse coming out of a stopped clock condition could be slightly distorted because of the other clock network charging requirements: it is also understood that board routing and signal loading have a large impact on the initial clock distortion.

V$_{DD}$3V Power-Down Removal

The PI6C133 device meets the following requirement to allow for a common design across multiple platforms.

To allow for multiple devices in platforms to share voltage regulators, the PI6C133 allows the removal of power from the V$_{DD}$3V voltage pins during the following specific condition. (Leakage currents from the V$_{DD}$3V and V$_{DD}$2V pins are not allowed to violate existing powerdown# specifications.)

Going to Powerdown Mode:

1. Assert the PWRDWN# signal to the PI6C133

2. Remove power from the 3.3V pins of the PI6C133.

3. All input pins of PI6C133 will be either powered down or driven to ground.

4. V$_{DD}$3 power plane will be pulled to or discharge to < 250mV.

5. The 2.5V pins will remain powered at 2.5V

To Restore Power:

1. Apply 3.3V to the PI6C133

2. Wait 200-2000ms

3. De-assert the PWRDWN# signal

4. Wait Xms (TBD) - longer than lock time specified for the device

5. Continue operation as normal

PI6C133 Clock Enable Configuration

CPU_STOP#	PWR_DWN#	PCI_STOP#	CPUCLK	CPU_div2	APIC	3V66	PCI	PCI_F	REF, 48 MHz	Osc	VCOs
X	0	X	LOW	LOW	LOW	LOW	LOW	LOW	LOW	OFF	OFF
0	1	0	LOW	ON	ON	LOW	LOW	ON	ON	ON	ON
0	1	1	LOW	ON	ON	LOW	ON	ON	ON	ON	ON
1	1	0	ON	ON	ON	ON	LOW	ON	ON	ON	ON
1	1	1	ON	ON	ON	ON	ON	ON	ON	ON	ON

Notes:
1. LOW means outputs held static LOW as per latency requirement below.
2. ON means active.
3. PWR_DWN# pulled LOW, impacts all outputs including REF and 48 MHz outputs.
4. All 3V66 as well as all CPU clocks should stop cleanly when CPU_STOP# is pulled LOW.
5. CPU_DIV2, IOAPIC, REF, 48 MHz signals are not controlled by the CPU_STOP# functionality and are enabled all in all conditions except PWR_DWN# = LOW.

PI6C133 Power Management Requirements

Signal	Signal State	Latency
		No. of rising edges of PCICLK
CPU_STOP#	0 (Disabled)	1
	1 (Enabled)	1
PCI_STOP#	0 (Disabled)	1
	1 (Enabled)	1
PWR_DWN#	1 (Normal Operation)	3ms
	0 (Power Down)	2 max.

Notes:
1. Clock on/off latency is defined in the number of rising edges of free running PCICLKs between the clock disable goes low/high to the first valid clock comes out of the device.
2. Power up latency is when PWR_DWN# goes inactve (high) to when the first valid clocks are driven from the device.

CPU_STOP# is an input to the clock synthesizer. It is used to turn off the CPU and 3V66 clocks for low power operation. CPU_STOP# is asserted asynchronously by the external clock control logic with the rising edge of the free running PCI clock (and hence CPU clock) and must be internally synchronized to the external PCI_F output. All other clocks will continue to run while the CPU clocks are disabled. The CPU clocks must always be stopped in a low state and started in such a manner as to guarantee that the high pulse width is a full pulse. **ONLY one rising edge of the PCI_F is allowed** after the clock control logic switched for both the CPU and 3V66 outputs to become enabled/disabled.
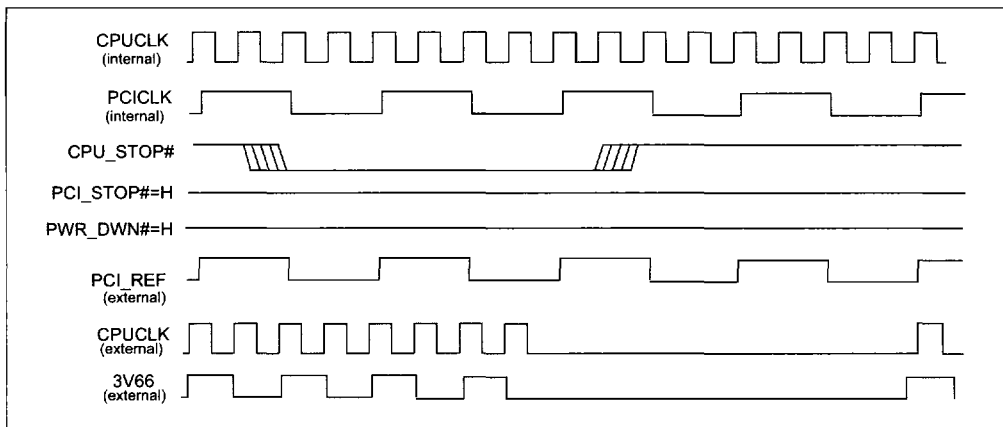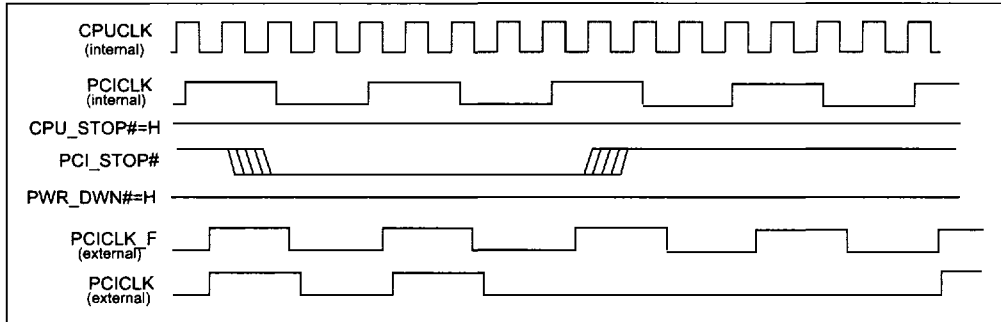

PI6C133 CPU_STOP# Timing Diagram

Notes:
1. All internal timing is referenced to the CPUCLK
2. The internal label means inside the chip and is a reference only. This in fact may not be the way that the control is designed.
3. CPU_STOP# signal is an input signal that must be made synchronous to free running PCI_F
4. 3V66 clocks also stop/start before
5. PWR_DWN# and PCI_STOP# are shown in a high state.
6. Diagrams shown with respect to 133 MHz. Similar operation when CPU is 100 MHz.

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PCI_STOP# is an input to the clock synthesizer and is made synchronous to the clock driver PCI_F output. It is used to turn off the PCI clocks for low-power operation. PCI clocks are required to be stopped in a low state and started such that a full high pulse width is guaranteed. **ONLY one rising edge of PCI_F is needed** after the clock control logic switched for the PCI outputs to become enabled/disabled.
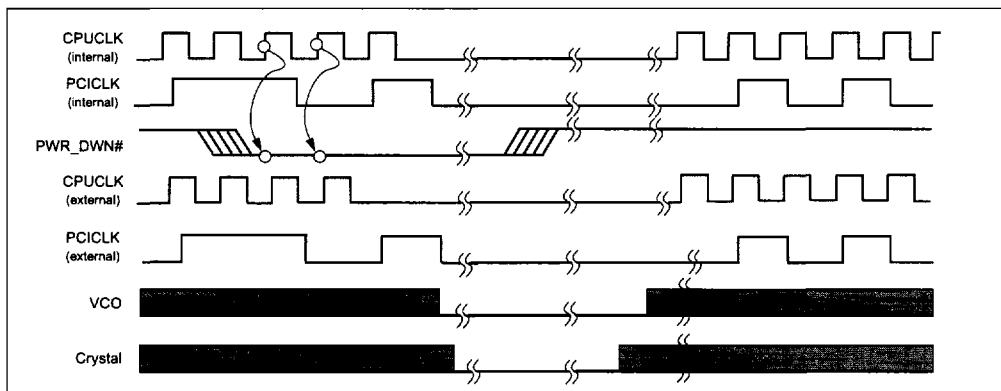

PI6C133 PCI_STOP# Timing Diagram

Notes:
1. All internal timing is referenced to the CPUCLK
2. PCI_STOP# signal is an input signal which is made synchronous to PCI_F output.
3. Internal means inside the chip.
4. All other clocks continue to run undisturbed.
5. PWR_DWN# and CPU_STOP# are shown in a high state.
6. Diagrams shown with respect to 133 MHz. Similar operation when CPU is 100 MHz.

The power-down selection is used to put the part into a very low power state without turning off the power to the part. PWR_DWN# is an asynchronous active low input. The signal needs to be synchronized internal to the device prior to powering down the clock synthesizer. PWR_DWN# is an asynchronous function for powering up the system. Internal clocks are not running after the device is put in power down. When PWR_DWN# is active low all clocks need to be driven to a low value and held prior to turning off the VCO's and the crystal. The power-up latency is less than 3ms. The power-down latency is short and conforms to the sequence requirements shown below. PCI_STOP# and CPU_STOP# are considered to be don't cares during power-down operations. REF and 48 MHz clocks are expected to be stopped in the LOW state as soon as possible. Owing to the state of internal logic stopping and holding REF clock outputs in the LOW state, more than one clock cycle may be required to complete.

PI6C133 PWR_DWN# Timing Diagram

Notes:
1. All internal timing is referenced to the CPUCLK
2. Internal means inside the chip.
3. PWR_DWN# is an asynchronous input and metstable conditions could exist.
   This signal is required to be synchronized inside the part.
4. The shaded sections on the VCO and the crystal signals indicate an active clock.
5. Diagrams shown with respect to 133 MHz. Similar operation when CPU is 100 MHz.

DC Specifications

DC parameters must be sustainable under steady state (DC) conditions

Absolute Maximum DC Power Supply

Symbol	Parameter	Min.	Max.	Units
$V_{DD}3V$ $V_{DD}2V$	Supply Voltage	-0.5	4.6	V
T_S	Storage Temperature	-65	150	°C

Absolute Maximum DC I/O

Symbol	Parameter	Min.	Max.	Units
$V_{IH}3$[1]	3.3V Input High Voltage	-0.5	4.6	
$V_{IL}3$	3.3V Input Low Voltage	-0.5		V
ESD prot.[2]	Input ESD protection	2000		

Notes:
1. Maximum V_{IH} is not to exceed maximum V_{DD}.
2. Human body model.

DC Operating Requirements

Symbol	Parameter	Condition	Min.	Max.	Units
$V_{DD}3V$	3.3 Supply Voltage[4]	3.3V ± 5%	3.135	3.465	V
$V_{DD}2V$	2.5V Supply Voltage[4]	2.5V ± 5%	2.375	2.625	
$V_{DD}3V = 3.3V ± 5\%$					
$V_{IH}3$	3.3V Input High Voltage[7]	$V_{DD}3$	2.0	V_{DD} +0.3	V
$V_{IL}3$	3.3V Input Low Voltage[7]		V_{SS} −0.3	0.8	
I_{IL}	Input Leakage Current[3,7]	$0 < V_{IN} < V_{DDQ}3$	−5	+5	µA
$V_{DD}2V = 2.5V ± 5\%$					
$V_{OH}2$	2.5V Output High Voltage[1]	$I_{OH} = -1mA$	2.0		V
$V_{OL}2$	2.5V Output Low Voltage[1]	$I_{OL} = 1mA$		0.4	
$V_{DD}3V = 3.3V ± 5\%$					
$V_{OH}3$	3.3V Output High Voltage[1]	$I_{OH} = -1mA$	2.4		V
$V_{OL}3$	3.3V Output Low Voltage[1]	$I_{OL} = 1mA$		0.4	

DC Operating Requirements (continued)

Symbol	Parameter	Condition	Min.	Max.	Units
$V_{DD3V} = 3.3V \pm 5\%$					
V_{POH}	PCI Bus Output High Voltage[1]	$I_{OH} = -1mA$	2.4		V
V_{POL}	PCI Bus Output Low Voltage[1,4]	$I_{OL} = 1mA$		0.55	
C_{IN}	Input Pin Capacitance			5	pF
C_{XTAL}	Xtal Pin Capacitance[5]		13.5	22.5	
C_{OUT}	Output Pin Capacitance			6	
L_{PIN}	Pin Inductance			7	nH
T_A	Ambient Temperature	No Airflow	0	70	°C

Notes:
1. Signal edge is required to be monotonic when transitioning through this region.
2. Input leakage Current does not include inputs with Pull-up or Pull-down resistors.
3. No power sequencing is implied or allowed to be required in the system.
4. Conforms to 5V PCI Signaling specification.
5. As seen by the crystal. Device is intended to be used with a 17-20pF AT crystal.
6. All inputs referenced to 3.3V power supply.

Buffer Specifications

Buffer Name	V_{CC} Range (V)	Impedance (Ohms)	Buffer Type
CPU, CPU_DIV2, APIC	2.375 -2.625	13.5 - 45	Type 1
48MHz, REF	3.135 - 3.465	20 -60	Type 3
PCI, 3V66	3.135 - 3.465	12 - 55	Type 5

Type 1 Buffer Characteristics
Operating Requirements

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{OHMIN}	Pull-Up Current[1]	$V_{OUT} = 1.0V$	-27			mA
I_{OHMAX}	Pull-Up Current[1]	$V_{OUT} = 2.375V$			-27	
I_{OLMIN}	Pull-Down Current[1]	$V_{OUT} = 1.2V$	27			
I_{OLMAX}	Pull-Down Current[1]	$V_{OUT} = 0.3V$			30	
T_{RH}	2.5V Type1 Output Rise Edge Rate[2]	2.5V ± 5% @ 0.4V- 2.0V	1/1		4/1	V/ns
T_{FH}	2.5V Type1 Output Fall Edge Rate[2]	2.5V ± 5% @ 2.0V- 0.4V	1/1		4/1	

Notes:
1. Production testing is expected to be a subset of characterization testing.
2. Output Rise and Fall time.
3. Reciever logic thresholds are $V_{IL} = 0.7$ and $V_{IH} = 1.7V$
4. R_{ON} 13.5-45 Ohm with a 29 Ohm nominal driver impedance.
5. $R_{ON} = V_{OUT}/I_{OH}$, V_{OUT}/I_{OL} measured at $V_{CC}/2$.

Type 3 Buffer Characteristics
Operating Requirements

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{OHMIN}	Pull-Up Current[1]	$V_{OUT} = 1.0V$	-29			mA
I_{OHMAX}	Pull-Up Current[1]	$V_{OUT} = 3.135V$			-23	
I_{OLMIN}	Pull-Down Current[1]	$V_{OUT} = 1.95V$	29			
I_{OLMAX}	Pull-Down Current[1]	$V_{OUT} = 0.4V$			27	
T_{RH}	3.3V Type 3 Output Rise Edge Rate[2]	3.3V ± 5% @ 0.4V- 2.4V	0.5		2.0	V/ns
T_{FH}	3.3V Type 3 Output Fall Edge Rate[2]	3.3V ± 5% @ 2.4V- 0.4V	0.5		2.0	

Notes:
1. Production testing is expected to be a subset of characterization testing.
2. Output rise and fall time.
3. Receiver logic thresholds are $V_{IL} = 0.8$ and $V_{IH} = 2.0V$.
4. R_{ON} 20 -60 Ohm with a 40 Ohm nominal driver impedance.
5. $R_{ON} = V_{OUT}/I_{OH}$, V_{OUT}/I_{OL} measured at $V_{CC}/2$.

Type 5 Buffer Characteristics
Operating Requirements

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{OHMIN}	Pull-Up Current[1]	$V_{OUT} = 1.0V$	-33			mA
I_{OHMAX}	Pull-Up Current[1]	$V_{OUT} = 3.135V$			-33	
I_{OLMIN}	Pull-Down Current[1]	$V_{OUT} = 1.95V$	30			
I_{OLMAX}	Pull-Down Current[1]	$V_{OUT} = 0.4V$			38	
T_{RH}	3.3V Type 4 Output Rise Edge Rate[2]	3.3V ± 5% @ 0.4V- 2.4V	1/1		4/1	V/ns
T_{FH}	3.3V Type 4 Output Fall Edge Rate[2]	3.3V ± 5% @ 2.4V- 0.4V	1/1			

Notes:
1. Production testing is expected to be a subset of characterization testing.
2. Output Rise and Fall time.
3. Output rise and fall time must be guaranteed across V_{CC}, process and temperature range.
4. Receiver logic thresholds are $V_{IL} = 0.8$ and $V_{IH} = 2.0$ Volts
5. R_{ON} 12 -55 Ohm with a 30 Ohm nominal driver impedance.
6. $R_{ON} = V_{OUT}/I_{OH}$, V_{OUT}/I_{OL} measured at $V_{CC}/2$.
7. See PCI specification for additional PCI details

AC Timing
Host Bus AC Timing Requirements

Symbol	Parameter	133 MHz Host		100 MHz Host		Units
		Min.	Max.	Min.	Max.	
TPeriod	Host /CPU CLK Period[1,8]	7.5	8.0	10.0	10.5	ns
T$_{HIGH}$	Host /CPU CLK High Time[4,9]	1.87	N/A	3.0	N/A	
T$_{LOW}$	Host /CPU CLK Low Time[5,9]	1.67	N/A	2.8	N/A	
T$_{RISE}$	Host /CPU CLK Rise Time[7]	0.4	1.6	0.4	1.6	
T$_{FALL}$	Host /CPU CLK Fall Time[7]	0.4	1.6	0.4	1.6	
TPeriod	CPU_Div2 CLK Period[1,8]	15.0	16.0	20.0	21.0	ns
T$_{HIGH}$	CPU_Div2 CLK High Time[4,9]	5.25	N/A	7.5	N/A	
T$_{LOW}$	CPU_Div2 CLK Low Time[5,9]	5.05	N/A	7.3	N/A	
T$_{RISE}$	CPU_Div2 CLK Rise Time[7]	0.4	1.6	0.4	1.6	
T$_{FALL}$	CPU_Div2 CLK Fall Time[7]	0.4	1.6	0.4	1.6	
TPeriod	IOAPIC CLK Period[1,8]	60.0	64.0	60.0	64.0	ns
T$_{HIGH}$	IOAPIC CLK High Time[4,9]	25.5	N/A	25.5	N/A	
T$_{LOW}$	IOAPIC CLK Low Time[5,9]	25.3	N/A	25.3	N/A	
T$_{RISE}$	IOAPIC CLK Rise Time[7]	0.4	1.6	0.4	1.6	
T$_{FALL}$	IOAPIC CLK Fall Time[7]	0.4	1.6	0.4	1.6	
TPeriod	3V66 CLK Period[1,3,8]	15.0	16.0	15.0	16.0	ns
T$_{HIGH}$	3V66 CLK High Time[4,9]	5.25	N/A	5.25	N/A	
T$_{LOW}$	3V66 CLK Low Time[5,9]	5.05	N/A	5.05	N/A	
T$_{RISE}$	3V66 CLK Rise Time[7]	0.4	1.6	0.4	1.6	
T$_{FALL}$	3V66 CLK Fall Time[7]	0.4	1.6	0.4	1.6	
TPeriod	PCI CLK Period[1,2,8]	30.0	N/A	30.0	N/A	ns
T$_{HIGH}$	PCICLK High Time[4,9]	12.0	N/A	12.0	N/A	
T$_{LOW}$	PCI CLK Low Time[5,9]	12.0	N/A	12.0	N/A	
T$_{RISE}$	PCI CLK Rise Time[7]	0.5	2.0	0.5	2.0	
T$_{FALL}$	PCI CLK Fall Time[7]	0.5	2.0	0.5	2.0	
tpZL, tpZH	Output Enable Delay (All outputs)	1.0	10.0	1.0	10.0	ns
tpLZ, tpZH	Output Disable Delay (All outputs)	1.0	10.0	1.0	10.0	
tstable	All Clock Stabilization from Power -Up[6]		3		3	ms

Notes:

1. Period, jitter, offset and skew measured on rising edge @1.25V for 2.5V clocks and @1.5V for 3.3V clocks.
2. The PCI clock is the Host clock divided by four at Host = 133 MHz. 3V66 clock internal VCO frequency divided by three for Host = 100 MHz
3. 3V66 is internal VCO frequency divided by four for Host = 133 MHz. 3V66 Clock is internal VCO frequency divided by three for Host = 100 MHz
4. tHIGH is measured at 2.0V for 2.5V outputs, 2.4V for 3.3V outputs.
5. tLOW is measusred at 0.4V for all outputs.
6. The time specified is measured from when V_{DDQ} achieves its nominal operating level (typical condition $V_{DDQ} = 3.3V$) until the frequency output is stable and operating with in specification.
7. tRISE and tFALL are measured as a transition through the threshold region $V_{OL} = 0.4V$ and $V_{OH} = 2.0V$ (1mA) JEDEC Specification.
8. The average period over any 1μs period of time is greater than the minimum specified period.
9. Calculated at minimum edge rate(1V/ns) to guarantee 45/55% duty-cycle. Pulsewidth is required to be wider at faster edge-rate to ensure duty cycle specification is met.

Group Skew and Jitter Limits

Output Group	Pin-Pin Skew	Cycle-Cycle Jitter	Duty Cycle	Nom V_{DD}	Skew, Jitter Measure Point
CPU	175ps	250ps	45/55		
CPU_Div2	175ps	250ps	45/55	2.5V	1.25V
IOAPIC	250ps	500ps	45/55		
48MHz	N/A	500ps	45/55		
3V66	250ps	500ps	45/55		
PCI	500ps	500ps	45/55	3.3V	1.5V
REF	N/A	1000ps	45/55		

Group Offset Limits

Group	Offset	Measurement Loads (Lumped)	Measure Points
CPU to 3V66	0.0-1.5ns CPU Leads	CPU@20pF, 3V66@30pF	CPU@1.25V, 3V66@1.5V
3V66 to PCI	1.5-.40ns 3V66 Leads	3V66@30pF, PCI@30pF	3V66@1.5V, PCI@1.5V
CPU to IOAPIC	1.5-4.0ns CPU Leads	CPU@20pF, IOAPIC@20pF	CPU@1.25V, IOAPIC@1.5V

Notes:

1. All offsets are to be measured at rising edges

Only offset specifications listed above are guaranteed/tested. The specification is treated as ANY ouput within the first specified bank to ANY output of the specified bank. Pin-pin skew is implied within offset specification, jitter is not. Previous offset specifications such as CPU to PCI offset are no longer required.
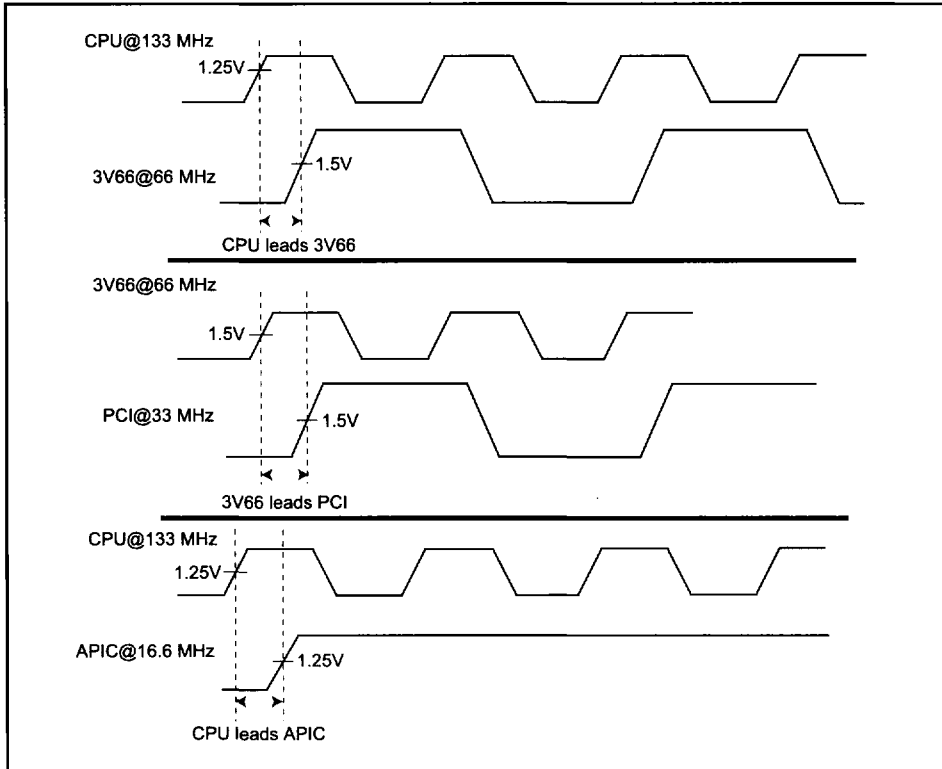
Group Offset Waveforms

Test and Measurement
## Minimum and Maximum Lumped Capacitive Test Loads

Clock	Min. Load	Max. Load	Units	Notes
CPU Clocks (HCLK)		20		1 device load, possible 2 loads
PCI Clocks (PCLK)		30		Must meet PCI 2.1 requirements
CPU_Div2		20		1 device load, possible 2 loads
3V66	10	30	pF	1 device load, possible 2 loads
48MHz Clock		20		1 device load
REF		20		1 device load
APIC		20		1 device load

Notes:
1. Maximum rise/fall times are guaranteed at maximum specified load for each type of output buffer.
2. Minimum rise/fall times are guaranteed at minimum specified load for each type of output buffer.
3. Rise/fall times are specified with pure capacitative load as shown. Testing may be done with an additional 500Ω resistor in parallel, if properly correlated with the capacitive load.

PERICOM
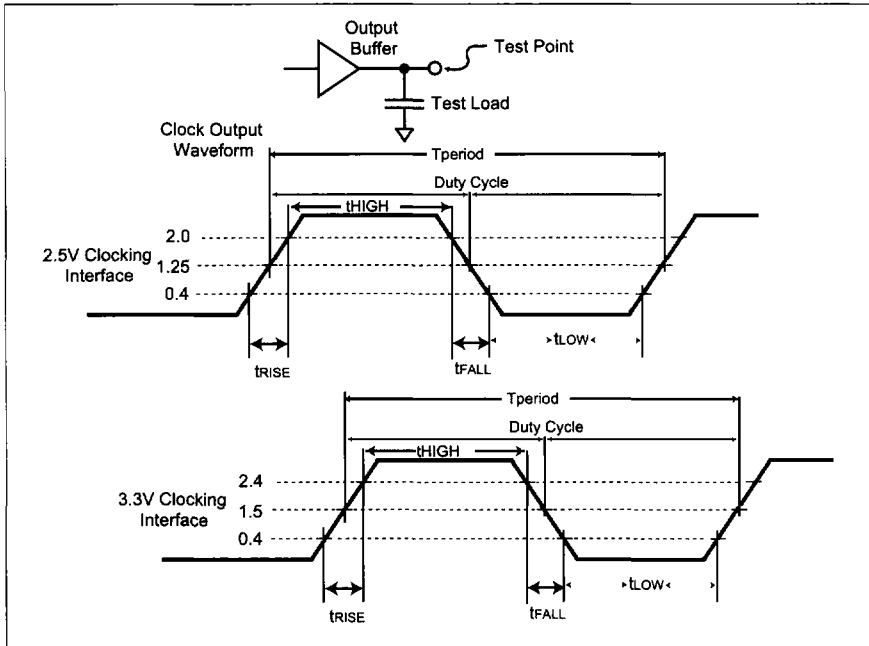
PI6C133 Clock Waveforms
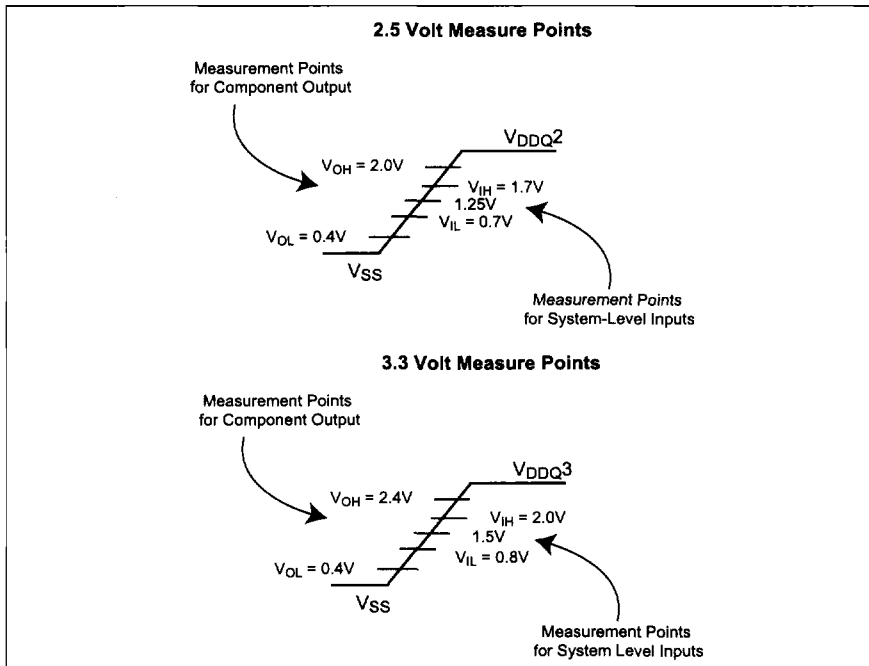
PI6C133 Component versus System Measure Points

48-pin SSOP Package Data
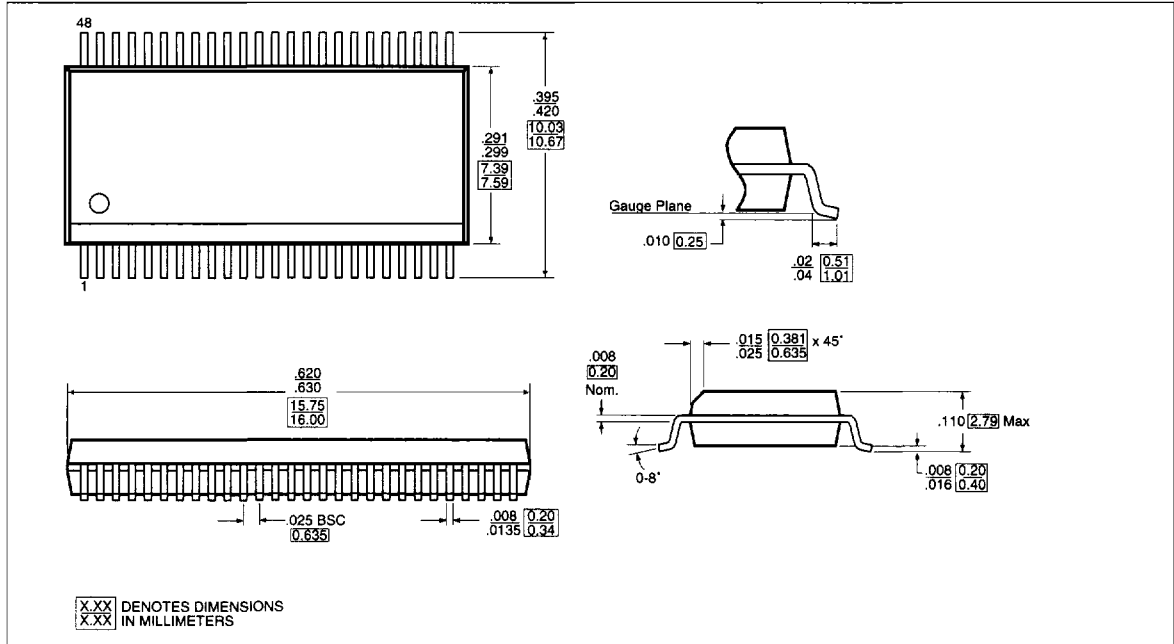
Ordering Information

Pin Number	Description
PI6C133-02V	48-pin SSOP Package