



EDI88512VA-RP

512Kx8 Ruggedized

Plastic Static Ram

Features

512Kx8 bit CMOS Static

Random Access Memory

- Access Times: 15*, 17*, 20 and 25ns
- Extended Temperature Testing

36 lead, JEDEC Approved Revolutionary Pinout

- Plastic SOJ No. 319

Single +3.3V ($\pm 10\%$) Supply Operation

*Industrial Temperature Only

512Kx8 Static RAM

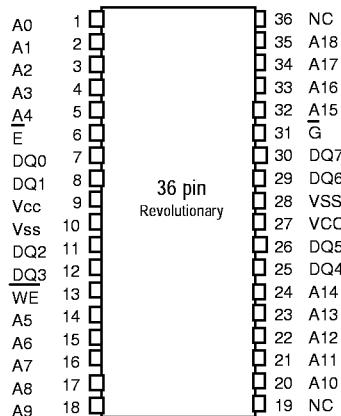
CMOS, Monolithic

EDI's ruggedized plastic 512Kx8 SRAM allows the user to capitalize on the cost advantage of using a plastic component while not sacrificing all of the reliability available in a full military device.

Extended temperature testing is performed with the test patterns developed for use on EDI's fully compliant 512Kx8 SRAMs. EDI fully characterizes devices to determine the proper test patterns for testing at temperature extremes. This is critical because the operating characteristics of a device change when it is operated beyond the commercial temperature range. Using commercial test methods will not guarantee a device that operates reliably in the field at temperature extremes. Users of EDI's ruggedized plastic benefit from EDI's extensive experience in characterizing SRAMs for use in military systems.

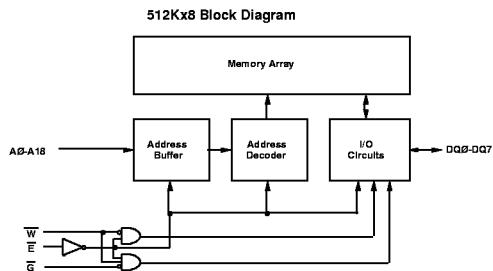
EDI's ruggedized plastic SOJ is footprint compatible with EDI's full military ceramic 36 pin SOJ.

Pin Configurations and Block Diagram



Pin Names

A0-A18	Address Inputs
E	Chip Enable
W	Write Enable
G	Output Enable
DQ0-DQ7	Common Data Input/Output
Vcc	Power (+3.3V)
Vss	Ground



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EDI88512VA-RP Rev. 0 1/98 ECO#9879

Absolute Maximum Ratings*

Voltage on any pin relative to VSS	-0.5V to 7.0V
Operating Temperature TA (Ambient)	
Commercial	0 °C to +70 °C
Industrial	-40 °C to +85 °C
Military	-55 °C to +125 °C
Storage Temperature, Plastic	-65 °C to +125 °C
Power Dissipation	0.55 Watt
Output Current	20 mA
Junction Temperature, TJ	175 °C

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

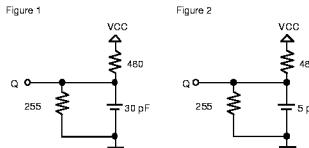
Recommended DC Operating Conditions

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	VCC	3.0	3.3	3.6	V
Supply Voltage	VSS	0	0	0	V
Input High Voltage	VIH	2.2	--	VCC+0.3	V
Input Low Voltage	VIL	-0.3	--	0.8	V

AC Test Conditions

Input Pulse Levels	VSS to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V
Output Load	See Figure 1

(note: For TEHQZ,TGHQZ and TWLQZ see figure 2)



DC Electrical Characteristics

Parameter	Sym	Conditions	Min	Max	Units
Operating Power	ICC1	W, E = VIL, I/O = 0mA, Min Cycle	15ns	--	170 mA
Supply Current		E ≥ VIH, VIN ≤ VIL	20-25ns	--	160 mA
Standby (TTL) Power	ICC2	VIN ≥ VIH	--	50	mA
Supply Current		VIN ≤ VIL			
Full Standby Power	ICC3	E ≥ VCC-0.2V	--	10	mA
Supply Current		VIN ≥ VCC-0.2V or VIN ≤ 0.2V			
Input Leakage Current	I _{LI}	VIN = 0V to VCC	-2	2	µA
Output Leakage Current	I _{LO}	V/I/O = 0V to VCC	-2	2	µA
Output High Voltage	VOH	I _{OH} = 4mA	2.4	--	V
Output Low Voltage	VOL	I _{OL} = 8mA	--	0.4	V

Truth Table

G	E	W	Mode	Output	Power
X	H	X	Standby	High Z	ICC2, ICC3
H	L	H	Output Deselect	High Z	ICC1
L	L	H	Read	DOUT	ICC1
X	L	L	Write	DIN	ICC1

Capacitance

(f=1.0MHz, VIN=VCC or VSS)

Parameter	Sym	Max	Unit
Address Lines	Cl	7	pF
Data Lines	CD/Q	8	pF

These parameters are sampled, not 100% tested.

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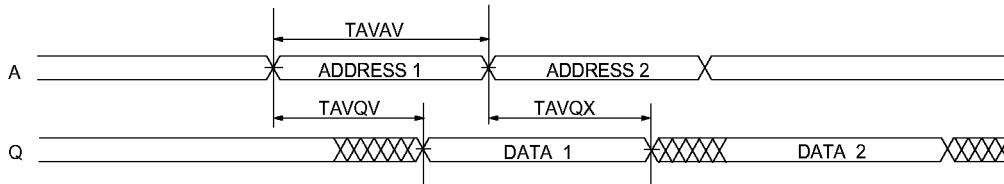
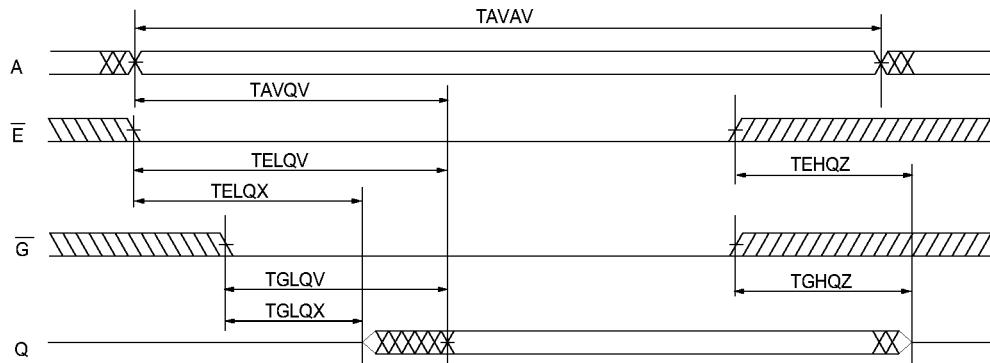
Plastic Static Ram

AC Characteristics Read Cycle

Parameter	Symbol	15ns*		17ns*		20ns		25ns		Units
		JEDEC	Alt.	Min	Max	Min	Max	Min	Max	
Read Cycle Time	TAVAV	TRC		15		17		20		25
Address Access Time	TAVQV	TAA			15		17		20	ns
Chip Enable Access Time	TELQV	TACS			15		17		20	ns
Chip Enable to Output in Low Z (1)	TELQX	TCLZ		3		3		3		ns
Chip Disable to Output in High Z (1)	TEHQZ	TCHZ		0	7	0	7	0	8	0 10
Output Hold from Address Change	TAVQX	TOH				4		5		ns
Output Enable to Output Valid	TGLQV	TOE			7		8		10	ns
Output Enable to Output in Low Z (1)	TGLQX	TLOZ		0		0		0		ns
Output Disable to Output in High Z(1)	TGHQZ	TOHZ		0	7	0	7	0	8	0 10

* Industrial Temperature Range Only

Note 1: Parameter guaranteed, but not tested.

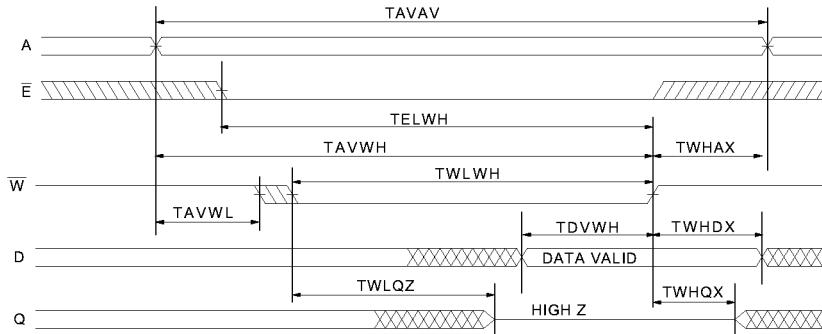
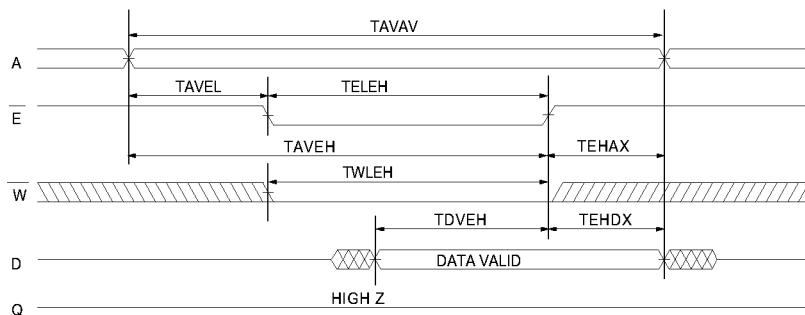
Read Cycle 1 - \bar{W} High, \bar{G}, \bar{E} Low**Read Cycle 2 - \bar{W} High**

AC Characteristics Write Cycle

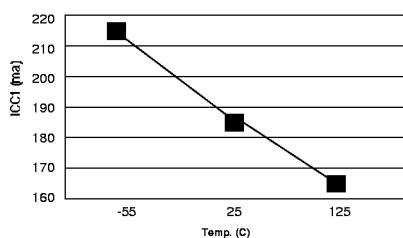
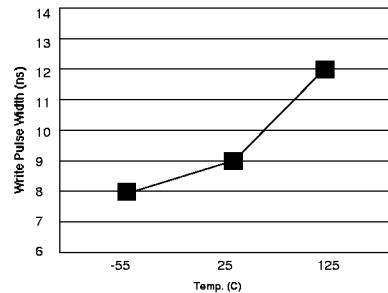
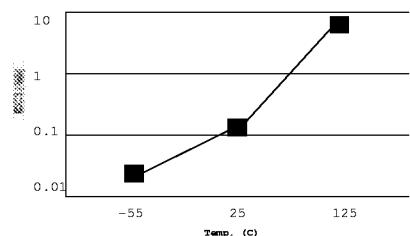
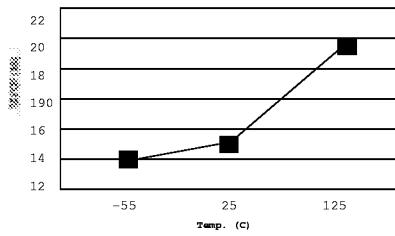
Parameter	JEDEC	Alt.	Symbol		15ns*		17ns*		20ns		25ns		Units
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	TAVAV	TWC	15		17		20		25				ns
Chip Enable to End of Write	TELWH	TCW	12		14		15		17				ns
	TELEH	TCW	12		14		15		17				ns
Address Setup Time	TAVWL	TAS	0		0		0		0				ns
	TAVEL	TAS	0		0		0		0				ns
Address Valid to End of Write	TAVWH	TAW	12		14		15		17				ns
	TAVEH	TAW	12		14		15		17				ns
Write Pulse Width	TLWHL	TWP	12		14		15		17				ns
	TWLEH	TWP	12		14		15		17				ns
Write Recovery Time	TWHAX	TWR	0		0		0		0				ns
	TEHAX	TWR	0		0		0		0				ns
Data Hold Time (1)	TWHDX	TDH	0		0		0		0				ns
	TEHDX	TDH	0		0		0		0				ns
Write to Output in High Z (1)	TWLQZ	TWHZ	0	7	0	8	0	8	0	10			ns
Data to Write Time	TDVWH	TDW	8		8		10		12				ns
	TDVEH	TDW	8		8		10		12				ns
Output Active from End of Write (1)	TWHQX	TWLZ	0		0		0		0				ns

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Note 1: Parameter guaranteed, but not tested.

Write Cycle 1 - \bar{W} Controlled

Write Cycle 2 - \bar{E} Controlled

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Normalized Operating Graphs**ICC1 (20ns) vs Temp****Write Pulse Width vs. Temp.****ICC3 vs. Temp****TAVQV vs. Temp**

Normalized curves are offered as a service to our customers. They are not to be construed as a guarantee of operating characteristics. Characteristics of actual devices will vary.



Ordering Information

Military (-55 °C to +125 °C)

Part No.	Speed (ns)	Package No.
Standard Power		
EDI88512VA20MM	20	319
EDI88512VA25MM	25	319

Industrial (-40 °C to +85 °C)

Part No.	Speed (ns)	Package No.
Standard Power		
EDI88512VA15MI	15	319
EDI88512VA17MI	17	319
EDI88512VA20MI	20	319
EDI88512VA25MI	25	319

Package Description

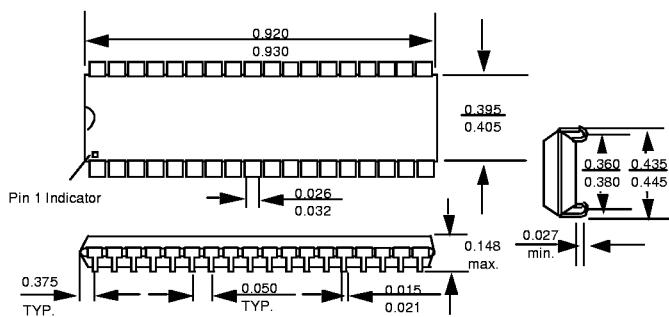
Package No. 319

36 Lead Plastic Small

Outline J-Lead Package

Theta $J_A = 50 \text{ °C/W}$

Theta $J_c = 18 \text{ °C/W}$



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