TC74HCT374AP/AF/AFW
TC74HCT534AP/AF

OCTAL D-TYPE FLIP-FLOP WITH 3-STATE OUTPUT
TC74HCT374AP/AF/AFW NON-INVERTING
TC74HCT534AP/AF INVERTING

The TC74HCT374A and HCT534A are high speed CMOS OCTAL FLIP-FLOPs with 3-STATE OUTPUT fabricated with silicon gate C^2MOS technology.

They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

Their inputs are compatible with TTL, NMOS, and CMOS output voltage levels.

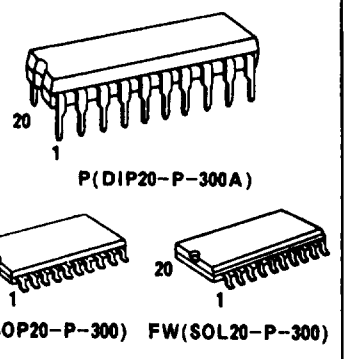
These 8-bit D-type flip-flops are controlled by a clock input (CK) and an output enable input ($\overline{OE}$).

The TC74HCT374A has non-inverting outputs, and the TC74HCT534A has inverting outputs.

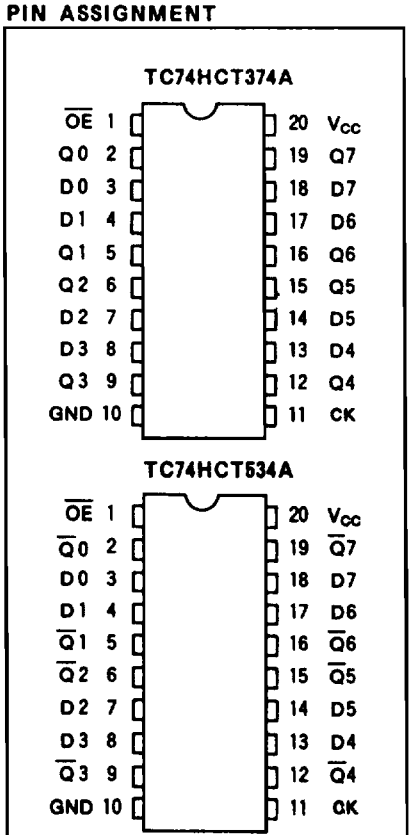
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ····· f_{MAX}=41MHz(Typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4μA(Max.)at Ta=25℃
- Compatible with TTL outputs ··· V_{IH}=2V (Min.)
  V_{IL}=0.8V (Max.)
- Wide interfacing ability ····· LSTTL, NMOS, CMOS
- Output Drive Capability ····· 15 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=6mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Pin and Function Compatible with 74LS374/534



PIN ASSIGNMENT

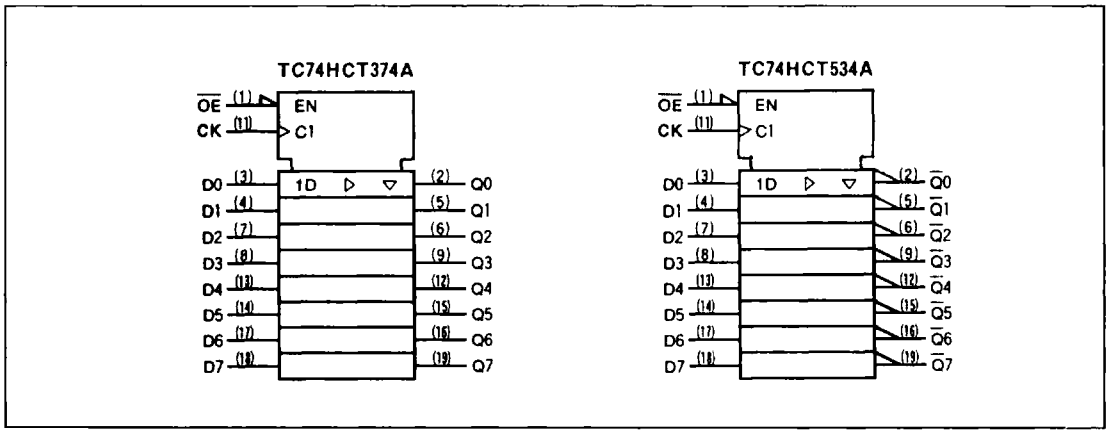


TRUTH TABLE

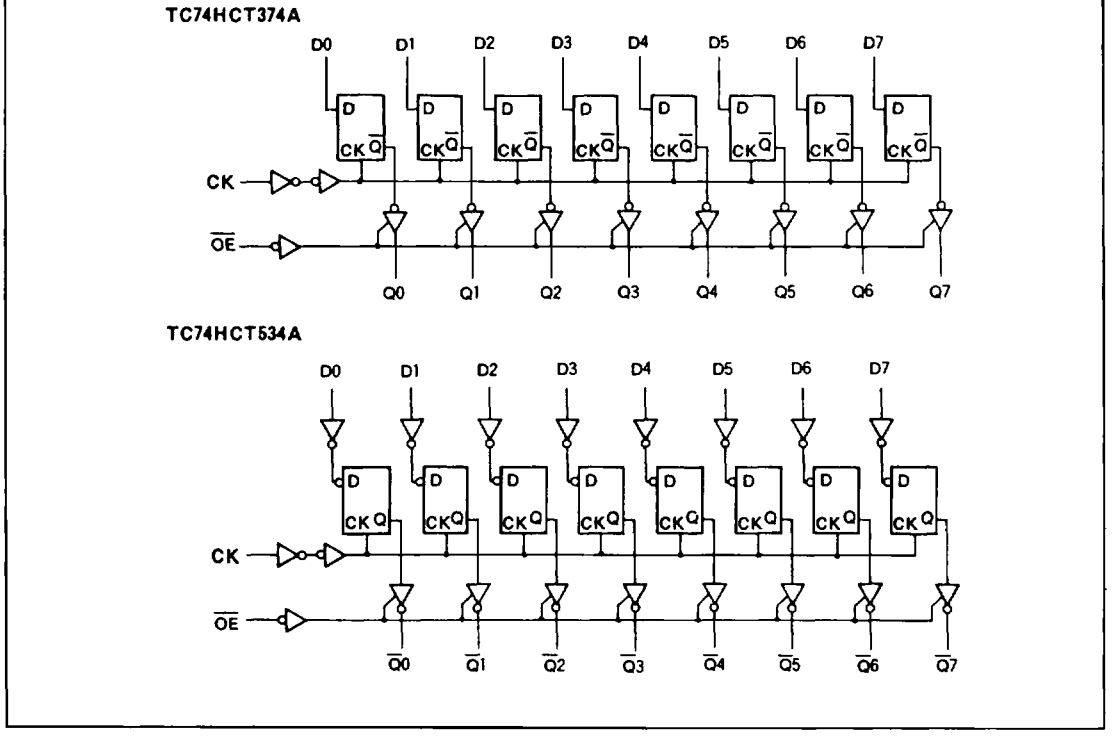
INPUTS			OUTPUTS	
$\overline{OE}$	CK	D	Q(T374A)	$\overline{Q}$(T534A)
H	X	X	Z	Z
L	↓	X	Q_n	$\overline{Q_n}$
L	↑	L	L	H
L	↑	H	H	L

X : Don't Care
Z : High Impedance
Q_n($\overline{Q_n}$) : No Change

IEC LOGIC SYMBOL



SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±75	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	4.5 ~ 5.5	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 500	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			4.5 ~ 5.5	2.0	−	−	2.0	−	V
Low−Level Input Voltage	V_{IL}			4.5 ~ 5.5	−	−	0.8	−	0.8	V
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	4.5	4.4	4.5	−	4.4	−	V
			I_{OH} =−6 mA	4.5	4.18	4.31	−	4.13	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	4.5	−	0.0	0.1	−	0.1	V
			I_{OL} =6 mA	4.5	−	0.17	0.26	−	0.33	
3−State Output Off−State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL}, V_{OUT} = V_{CC} or GND		5.5	−	−	±0.5	−	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		5.5	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		5.5	−	−	4.0	−	40.0	μA
	ΔI_{CC}	PER INPUT: V_{IN} =0.5V or 2.4V, OTHER INPUT: V_{IN} or GND		5.5	−	−	2.0	−	2.9	mA

TIMING REQUIREMENTS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ TYP.	Ta=25℃ LIMIT	Ta=−40 ~85℃ LIMIT	UNIT
Minimum Pulse Width (CK)	$t_{W(H)}$ $t_{W(L)}$		4.5	−	15	19	ns
			5.5	−	14	17	
Minimum Set−up Time (Dn)	t_s		4.5	−	15	19	
			5.5	−	14	17	
Minimum Hold Time (Dn)	t_h		4.5	−	0	0	
			5.5	−	0	0	
Clock Frequency	f		4.5	−	31	25	MHz
			5.5	−	37	30	

AC ELECTRICAL CHARACTERISTICS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	CL	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		50	4.5	−	7	12	−	15	ns
				5.5	−	6	11	−	14	
Propagation Delay Time (CK−Q, $\overline{Q}$)	t_{pLH} t_{pHL}		50	4.5	−	20	30	−	38	
				5.5	−	17	25	−	31	
			150	4.5	−	25	38	−	48	
				5.5	−	22	33	−	41	
Output Enable time	t_{pZL} t_{pZH}	$R_L=1k\Omega$	50	4.5	−	17	30	−	38	
				5.5	−	14	25	−	31	
			150	4.5	−	25	38	−	48	
				5.5	−	19	33	−	41	
Output Disable time	t_{pLZ} t_{pHZ}	$R_L=1k\Omega$	50	4.5	−	16	28	−	35	
				5.5	−	14	24	−	30	
Maximum Clock Frequency	f_{MAX}		50	4.5	31	50	−	25	−	
				5.5	37	59	−	30	−	
Input Capacitance	C_{IN}				−	5	10	−	10	pF
Output Capacitance	C_{OUT}				−	10	−	−	−	
Power Dissipation Capacitance	C_{PD}(1)				−	48	−	−	−	

Note(1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8(\text{per bit})$$

And the total C_{PD} when n pcs. of Flip Flop operate can be gained by the following equation:

$$C_{PD}(\text{total})=30+18 \cdot n$$