IS 61C61/62

16K X 4 HIGH SPEED SEPARATE I/O CMOS STATIC RAM

AUGUST 1990

FEATURES

- Very High Speed - 15, 20, 25, 30ns (Max.)
- **Fast output enable (tDOE) for cache applications**
- Automatic power-down when chip is deselected
- CMOS Low Power Operation
  - 400mW (Typical) Operating
  - 55mW (Typical) TTL standby
  - 25µW (Typical) CMOS standby (L-version)
- TTL compatible interface levels
- Single 5V power supply
- Fully static operation-no clock refresh required
- Three state outputs
- Chip enable $\overline{CE}_1$, $\overline{CE}_2$ for simple memory expansion
- The IS61C61: DOUT follows DIN during write cycle when $\overline{OE}$ is low
- The IS61C62: Output pins stay in high impedance state during write cycle
- Data retention as low as 2V for battery back-up (L-version)

DESCRIPTION

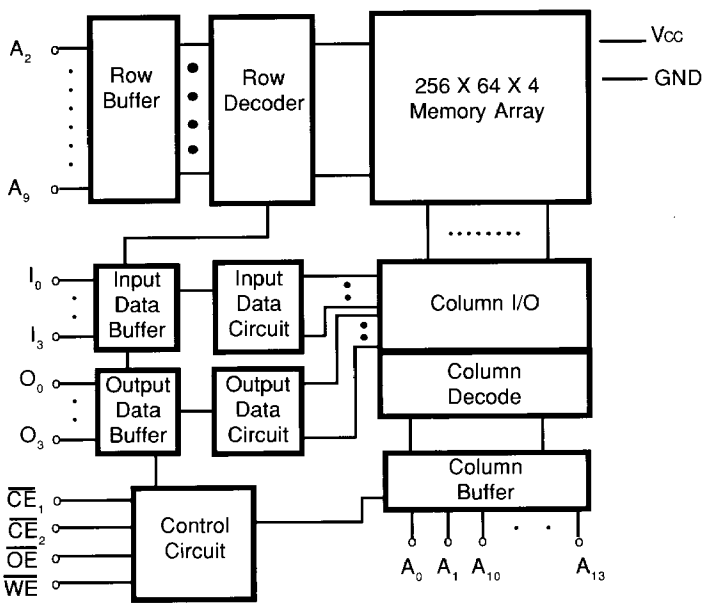
The ISSI IS61C61 and IS61C62 are very high speed, low power, 16384 words by 4 bit static RAMs. The devices are fabricated using ISSI's high performance CMOS double metal technology. This highly reliable process coupled with innovative circuit design techniques, yields access times as fast as 15ns with low power consumption.

When either one of the Chip Enables ($\overline{CE}_1$, $\overline{CE}_2$) are high the device assumes a standby with low power consumption mode at which the power dissipation can be reduced down to 25µW (typical) with CMOS input levels.

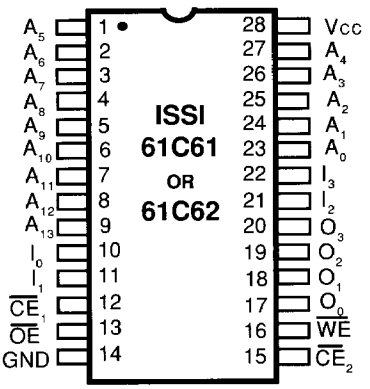
Easy memory expansion is provided by using active low Chip Enables, ($\overline{CE}_1$, $\overline{CE}_2$) and three-state drivers. The IS61C61 and IS61C62 have the active low Output Enable ($\overline{OE}$) feature.

The IS61C61 and IS61C62 are packaged in the JEDEC standard 28 pin, 300 mil DIP and SOJ packages.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



DIP/SOJ

Integrated Silicon Solution, Inc.
680 Almanor Avenue, Sunnyvale, California 94086 (408) 733-4774 FAX (408) 245-4774

ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Parameter	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-65 to +150	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC output Current (low)	20	mA

OPERATING RANGE

Range	Ambient Temperature	Vcc
Commercial	0°C to 70°C	5V ±10%
Industrial	-40°C to 85°C	5V ±10%

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Electrical Characteristics over Operating Range

Symbol	Description	Test Conditions	-15 -L15		-20 -L20		-25 -L25		-30 -L30		Units
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
V_{OH}	Output High Voltage	V_{CC} = MIN., I_{OH} = -4.0mA	2.4		2.4		2.4		2.4		V
V_{OL}	Output Low Voltage	V_{CC} = MIN., I_{OL} = 8.0 mA		0.4		0.4		0.4		0.4	V
V_{IH}	Input High Voltage		2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input Low Voltage (2)		-0.5	0.8	-0.5	0.8	0.5	0.8	-0.5	0.8	V
I_{LI}	Input Leakage	GND ≤ V_{IN} ≤ V_{CC}	-10	10	-10	10	-10	10	-10	10	µA
I_{LO}	Output Leakage	GND ≤ V_{OUT} ≤ V_{CC}, Output Disabled	-10	10	-10	10	-10	10	-10	10	µA
I_{OS}	Output Short Circuit Current (1)	V_{CC} = MAX., V_{OUT} = GND		-150		-150		-150		-150	mA
I_{CC_1}	Vcc Operating Supply Current	V_{CC} = MAX., IOUT = 0mA, f = 0 (3)		160		140		120		120	mA
I_{CC_2}	Vcc Dynamic Operating Supply Current	V_{CC} = MAX., IOUT = 0 mA, f = f_{MAX}. (3)		190		170		145		145	mA
I_{SB_1}	TTL Standby Current (TTL Inputs)	V_{CC} = MAX., V_{IN} = V_{IH} OR V_{IL} $\overline{CE}_1$ or $\overline{CE}_2$ ≥ V_{IH}, f = 0 (3)		40		30		25		20	mA
I_{SB_2}	CMOS Standby	V_{CC} = Max., $\overline{CE}_1$ or $\overline{CE}_2$ ≥ V_{CC} -0.2V V_{IN} ≥ V_{CC} -0.2V, OR V_{IN} ≤ 0.2V, f = 0 (3)		6		5		4		3	mA
			L	100	L	100	L	100	L	100	µA

Notes:
1. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
2. V_{IL} = -3.0V for pulse width less than 10ns.
3. At f = fmax address and data input are cycling at the maximum frequency, f = 0 means no input lines change.

Capacitance (1,2)

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

1. This parameter is guaranteed and not tested.
2. Test condition: TA = 25°C, f = 1MHz, Vcc = 5.0V

TRUTH TABLE

MODE	$\overline{WE}$	$\overline{CE_1}$	$\overline{CE_2}$	$\overline{OE}$	INPUT	OUTPUT	V_{CC} CURRENT
Not Selected (Power Down)	X	H	X	X	X	High Z	I_{SB_1}, I_{SB_2}
	X	X	H	X	X	High Z	I_{SB_1}, I_{SB_2}
Output Disabled	H	L	L	H	X	High Z	I_{CC_1}, I_{CC_2}
Read (61C61/62)	H	L	L	L	X	DOUT	I_{CC_1}, I_{CC_2}
Write (61C62)	L	L	L	X	DIN	High Z	I_{CC_1}, I_{CC_2}
Write (61C61)	L	L	L	L	DIN	Follows DIN	I_{CC_1}, I_{CC_2}
Write (61C61)	L	L	L	H	DIN	High Z	I_{CC_1}, I_{CC_2}

Switching Characteristics Over Operating Range (1)

Symbol	Description	61C61/62-15 61C61/62-L15		61C61/62-20 61C61/62-L20		61C61/62-25 61C61/62-L25		61C61/62-30 61C61/62-L30		Units
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
READ CYCLE										
tRC	Read Cycle Time	15		20		25		30		ns
tAA	Address Access Time		15		20		25		30	ns
tOHA	Output Hold Time	3		3		3		3		ns
tACE	$\overline{CE}$ Access Time		15		20		25		30	ns
tDOE	$\overline{OE}$ Access Time		7		7		9		12	ns
tLZOE	$\overline{OE}$ to Low Z Output	0		0		0		0		ns
tHZOE(2)	$\overline{OE}$ to High Z Output		8		10		12		15	ns
tLZCE	$\overline{CE}$ to Low Z Output	3		3		3		3		ns
tHZCE(2)	$\overline{CE}$ to High Z Output		8		10		12		15	ns
tPU	$\overline{CE}$ to Power Up	0		0		0		0		ns
tPD	$\overline{CE}$ to Power Down		15		20		20		20	ns
WRITE CYCLE (3)										
tWC	Write Cycle Time	15		20		25		30		ns
tSCE	$\overline{CE}$ to Write End	12		17		22		25		ns
tAW	Address Set-up Time to Write End	12		15		20		25		ns
tHA	Address Hold from Write End	0		0		0		0		ns
tSA	Address Set-up Time	0		0		0		0		ns
tPWE (4)	$\overline{WE}$ Pulse Width	10		12		15		18		ns
tSD	Data Set-up to Write End	9		10		12		15		ns
tHD	Data hold from Write End	0		0		0		0		ns
tHZWE (2)	$\overline{WE}$ LOW to High-Z Output		6		7		8		10	ns
tLZWE	$\overline{WE}$ HIGH to LOW-Z Output	0		0		0		0		ns
tADV	Data Valid to Output Valid (61C61)		15		20		25		30	ns
tAWE	$\overline{WE}$ Low to Data Valid (61C61)		15		20		25		30	ns

Notes:

1. Test conditions assume signal transition times of 5ns or less, timing reference levels of 1.5V, Input pulse levels of 0 to 3.0V and output loading specified in figure 1a.
2. Tested with the load in Figure 1b. Transition is measured ± 500mV from steady state voltage.
3. The internal write time is defined by the overlap of $\overline{CE_1}$, $\overline{CE_2}$ and $\overline{WE}$ low. All signals must be in valid states to initiate a Write, but anyone can go inactive to terminate the Write. The Data input Setup and Hold timing are referenced to the rising edge of the signal that terminates the write.
4. Tested with $\overline{OE}$ high.
5. $\overline{WE}$ is high for a Read Cycle.
6. The device is continuously selected. $\overline{OE}$, $\overline{CE_1}$, $\overline{CE_2}$ = VIL.
7. Address is valid prior to or coincident with $\overline{CE_1}$, $\overline{CE_2}$ Low transitions.
8. Output pin will assume the High-Z state if $\overline{OE}$ = VIH.

AC TEST CONDITIONS

Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing and Reference Level	1.5V

AC TEST LOADS

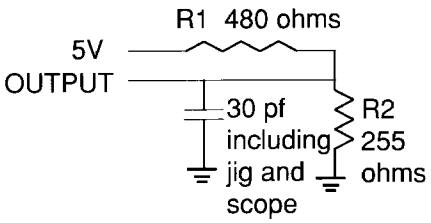


Figure 1a

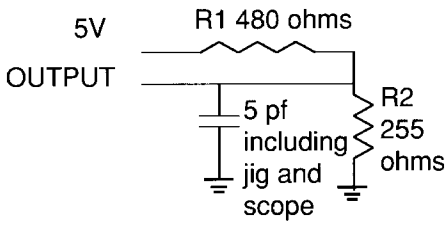
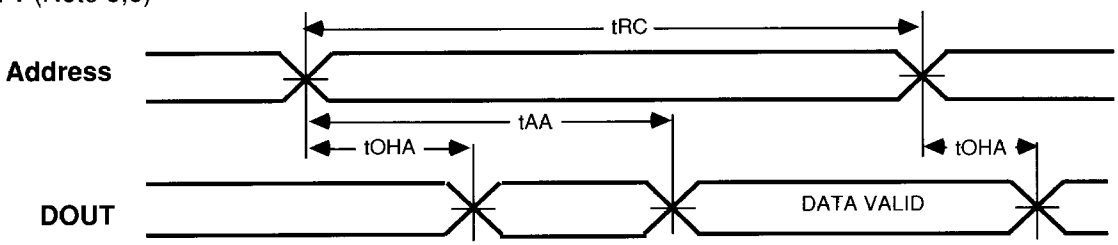


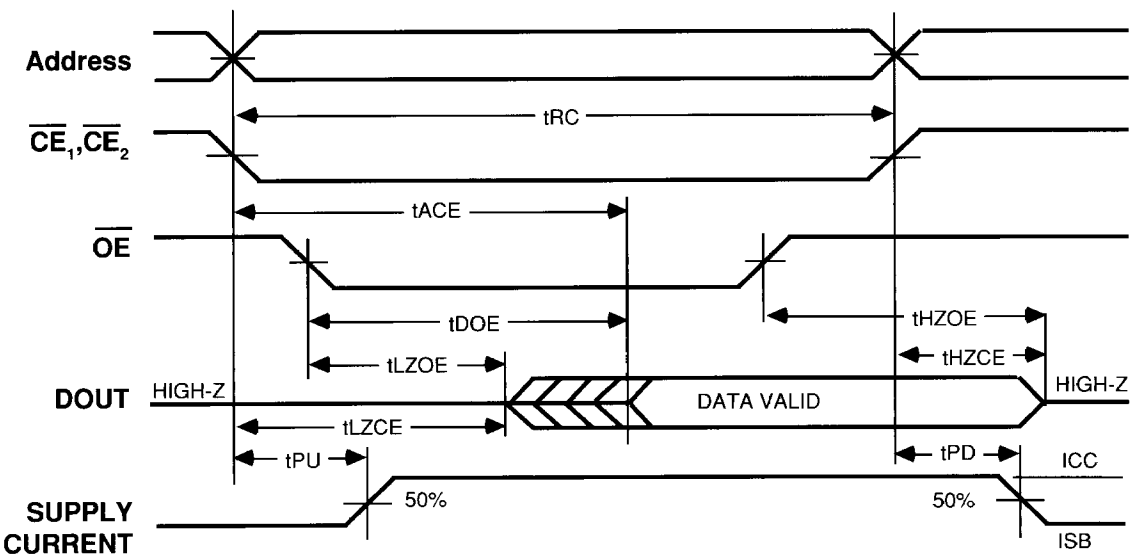
Figure 1b

AC WAVEFORMS

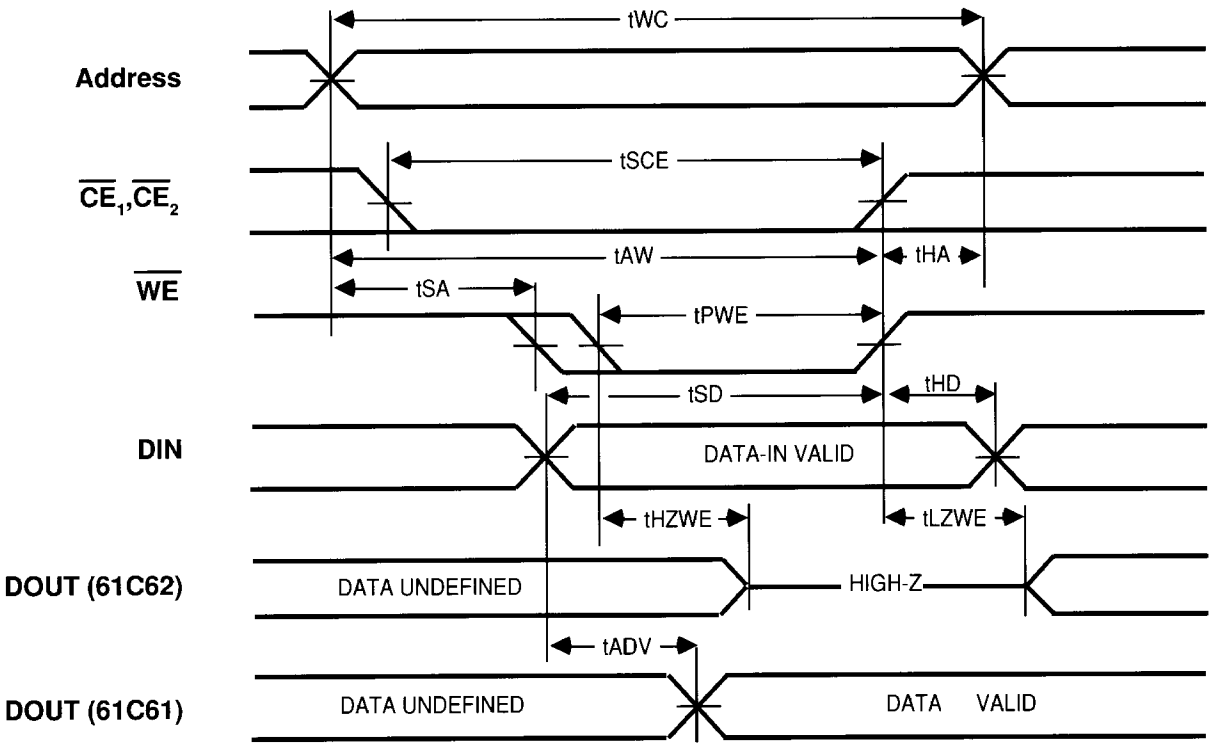
READ CYCLE NO. 1 (Note 5,6)



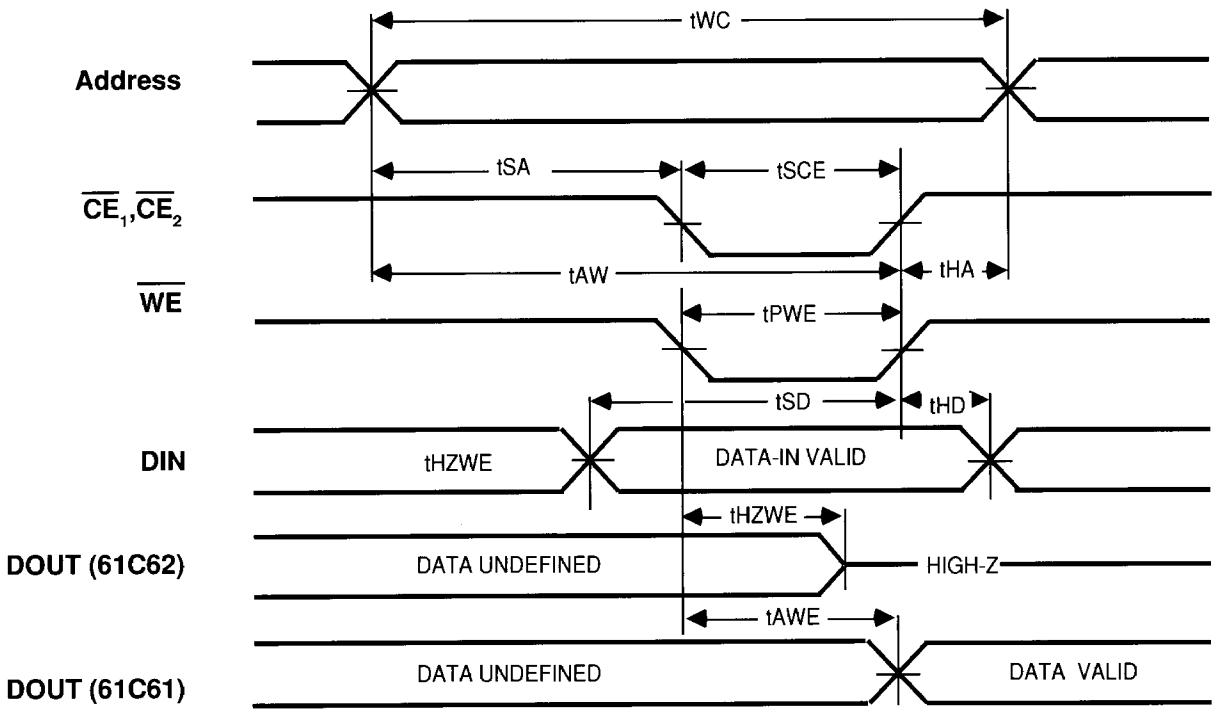
READ CYCLE NO. 2 (Note 5,7)



WRITE CYCLE NO. 1 ($\overline{WE}$ controlled) (Note 3,8)



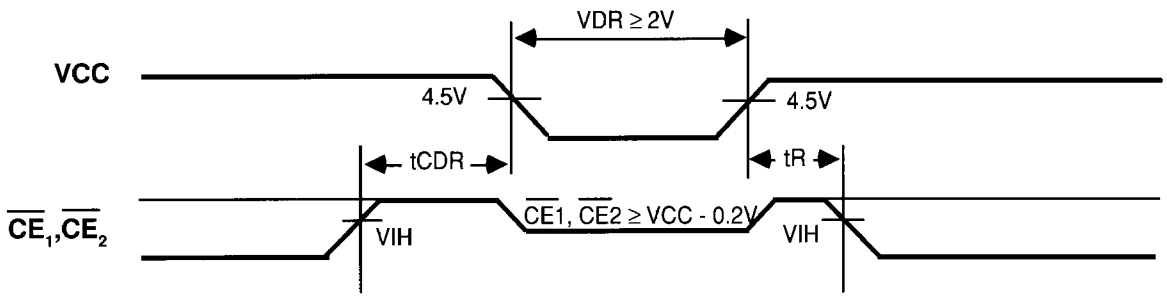
WRITE CYCLE NO. 2 ($\overline{CE}$ controlled) (Note 3,8)



DATA RETENTION CHARACTERISTICS (L Version only)

Parameter	Description	Test Conditions	Min.	Max.	Units
VDR	VCC for retention of data	VCC = 2.0V	2.0	-----	V
ICCDR	Data retention current	$\overline{CE}_1, \overline{CE}_2 \geq$ VCC - 0.2V,	-----	100	µA
tCDR	Chip deselect to data retention time	CMOS Inputs	0	-----	ns
tR	Operation recovery time		tRC	-----	ns
IL I	Input leakage current		-----	2	µA

DATA RETENTION WAVEFORM



PIN DESCRIPTIONS

A_0 - A_{13} Address Inputs
These 14 address inputs select one of the 16384 4-bit words in the RAM.

$\overline{CE}$1 and $\overline{CE}$2 Chip Enable Input
$\overline{CE}$1, $\overline{CE}$2 chip enable inputs are active Low. The chip enables must be active to read from or write to the device. If the chip enable is not active, the device is deselected and is in a standby power mode. The output pins will be in the high-impedance state when the device is deselected.

$\overline{OE}$ Output Enable Input
The ouput enable input is active Low. If the output enable is active while the chip is selected and the write enable is inactive, data will be present on the Output pins. The Output pins will be in the high-impedance state when $\overline{OE}$ is inactive. If the output enable is active while the chip is selected and the write enable is active, data will be present on the output pins same as data input for IS61C61.

$\overline{WE}$ Write Enable Input
The write enable input is active Low and controls read and write operations. With the chip selected, when $\overline{WE}$ is Low, Input data present on the Input pins will be written into the selected memory location.

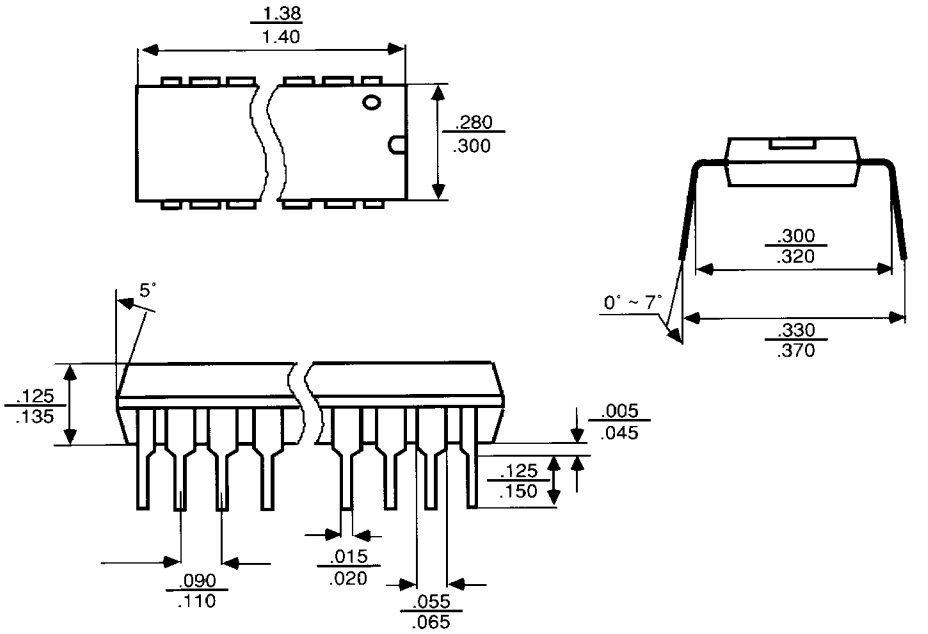
I_0 - I_3
These 4 input pins are used to write data into the RAM.

O_0 - O_3
These 4 output pins are used to read the data from the RAM.

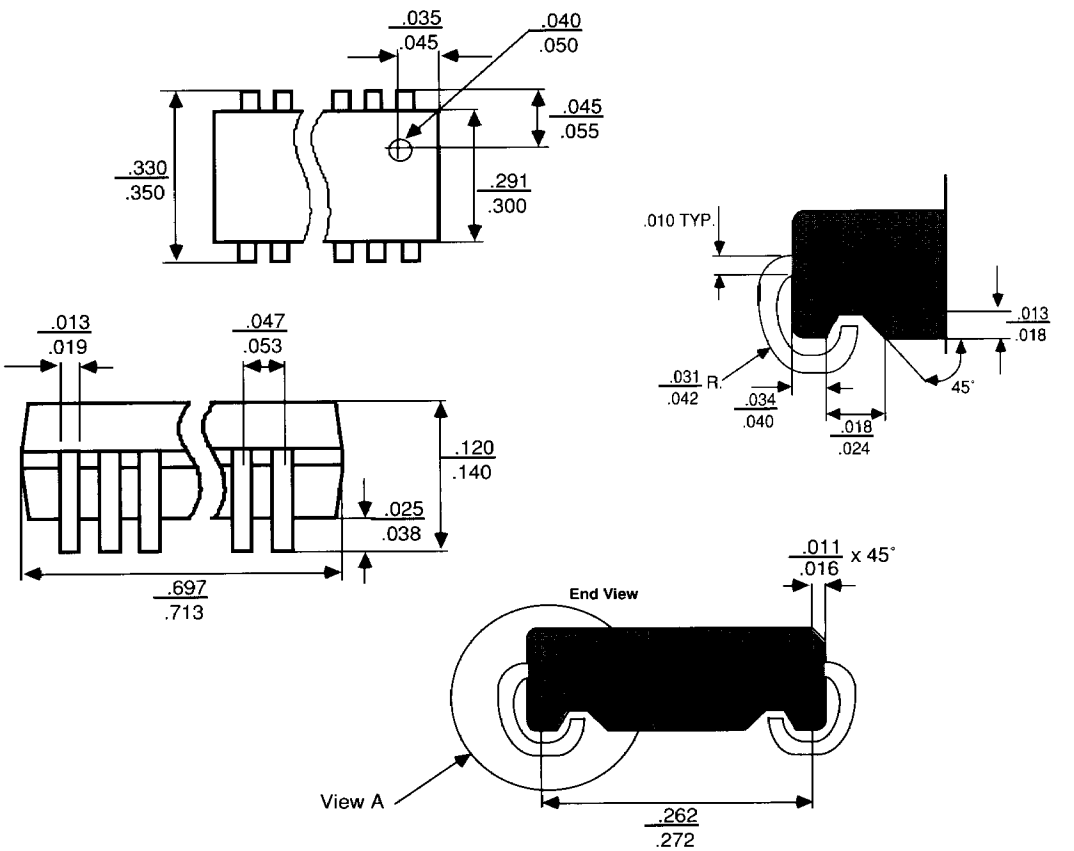
Vcc - Power

GND - Ground

28 Pin 300 MIL PLASTIC DIP Package



28 PIN SOJ PACKAGE



SPEED (ns)	ORDER PART NUMBER	PACKAGE	TEMPERATURE RANGE
15	IS61C61/62-15N	Plastic DIP - 300 mil	0°C to +70°C
15	IS61C61/62-15J	Plastic Small Outline J	0°C to +70°C
15 LOW	IS61C61/62-L15N	Plastic DIP - 300 mil	0°C to +70°C
15 POWER	IS61C61/62-L15J	Plastic Small Outline J	0°C to +70°C
20	IS61C61/62-20N	Plastic DIP - 300 mil	0°C to +70°C
20	IS61C61/62-20J	Plastic Small Outline J	0°C to +70°C
20 LOW	IS61C61/62-L20N	Plastic DIP - 300 mil	0°C to +70°C
20 POWER	IS61C61/62-L20J	Plastic Small Outline J	0°C to +70°C
25	IS61C61/62-25N	Plastic DIP - 300 mil	0°C to +70°C
25	IS61C61/62-25J	Plastic Small Outline J	0°C to +70°C
25 LOW	IS61C61/62-L25N	Plastic DIP - 300 mil	0°C to +70°C
25 POWER	IS61C61/62-L25J	Plastic Small Outline J	0°C to +70°C
30	IS61C61/62-30N	Plastic DIP - 300 mil	0°C to +70°C
30	IS61C61/62-30J	Plastic Small Outline J	0°C to +70°C
30 LOW	IS61C61/62-L30N	Plastic DIP - 300 mil	0°C to +70°C
30 POWER	IS61C61/62-L30J	Plastic Small Outline J	0°C to +70°C

ISSI
Integrated Silicon Solution, Inc.
680 Almanor Avenue, Sunnyvale, California 94086 (408) 733-ISSI FAX (408) 245-ISSI