

74F251A 8-Input Multiplexer with 3-STATE Outputs

General Description

The 74F251A is a high-speed 8-input digital multiplexer. It provides, in one package, the ability to select one bit of data from up to eight sources. It can be used as a universal function generator to generate any logic function of four variables. Both assertion and negation outputs are provided.

Features

- Multifunctional capability
- On-chip select logic decoding
- Inverting and non-inverting 3-STATE outputs

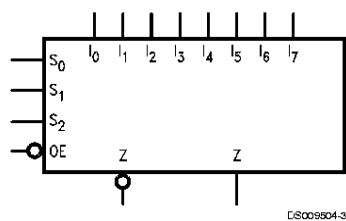
Ordering Code:

| Commercial | Military | Package Number | Package Description |
|--------------------|--------------------|----------------|---|
| 74F251APC | | N16E | 16-Lead (0.300" Wide) Molded Dual-In-Line |
| | 54F251ADM (Note 2) | J16A | 16-Lead Ceramic Dual-In-Line |
| 74F251ASC (Note 1) | | M16A | 16-Lead (0.150" Wide) Molded Small Outline, JEDEC |
| 74F251ASJ (Note 1) | | M16D | 16-Lead (0.300" Wide) Molded Small Outline, EIAJ |
| | 54F251AFM (Note 2) | W16A | 16-Lead Cerpack |
| | 54F251ALL (Note 2) | E20A | 20-Lead Ceramic Leadless Chip Carrier, Type C |

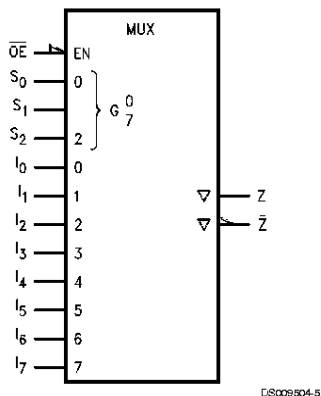
Note 1: Devices also available in 13" reel. Use suffix = SCX and SJX

Note 2: Military grade device with environmental and burn-in processing. Use suffix = DMQB, FMQB and LMQB

Logic Symbols



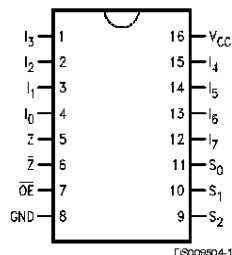
IEEE/IEC



DS009504-5

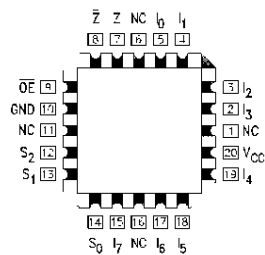
Connection Diagrams

Pin Assignment for DIP, SOIC and Flatpak



DS009504-1

Pin Assignment for LCC



DS009504-2

Unit Loading/Fan Out

| Pin Names | Description | 54F/74F | |
|-----------------|--|------------------|---|
| | | U.L. HIGH/LOW | Input I_{IH}/I_{IL} Output I_{OH}/I_{OL} |
| S_0-S_2 | Select Inputs | 1.0/1.0 | 20 μ A/-0.6 mA |
| \overline{OE} | 3-STATE Output Enable Input (Active LOW) | 1.0/1.0 | 20 μ A/-0.6 mA |
| I_0-I_7 | Multiplexer Inputs | 1.0/1.0 | 20 μ A/-0.6 mA |
| Z | 3-STATE Multiplexer Output | 150/40 (33.3) | -3 mA/24 mA (20 mA) |
| \overline{Z} | Complementary 3-STATE Multiplexer Output | 150/40 (33.3) | -3 mA/24 mA (20 mA) |

Functional Description

This device is a logical implementation of a single-pole, 8-position switch with the switch position controlled by the state of three Select inputs, S_0 , S_1 , S_2 . Both assertion and negation outputs are provided. The Output Enable input (\overline{OE}) is active LOW. When it is activated, the logic function provided at the output is:

$$Z = \overline{OE} \cdot (I_0 \cdot \overline{S_0} \cdot \overline{S_1} \cdot \overline{S_2} + I_1 \cdot S_0 \cdot \overline{S_1} \cdot \overline{S_2} + I_2 \cdot \overline{S_0} \cdot S_1 \cdot \overline{S_2} + I_3 \cdot S_0 \cdot S_1 \cdot \overline{S_2} + I_4 \cdot \overline{S_0} \cdot \overline{S_1} \cdot S_2 + I_5 \cdot S_0 \cdot \overline{S_1} \cdot S_2 + I_6 \cdot \overline{S_0} \cdot S_1 \cdot S_2 + I_7 \cdot S_0 \cdot S_1 \cdot S_2)$$

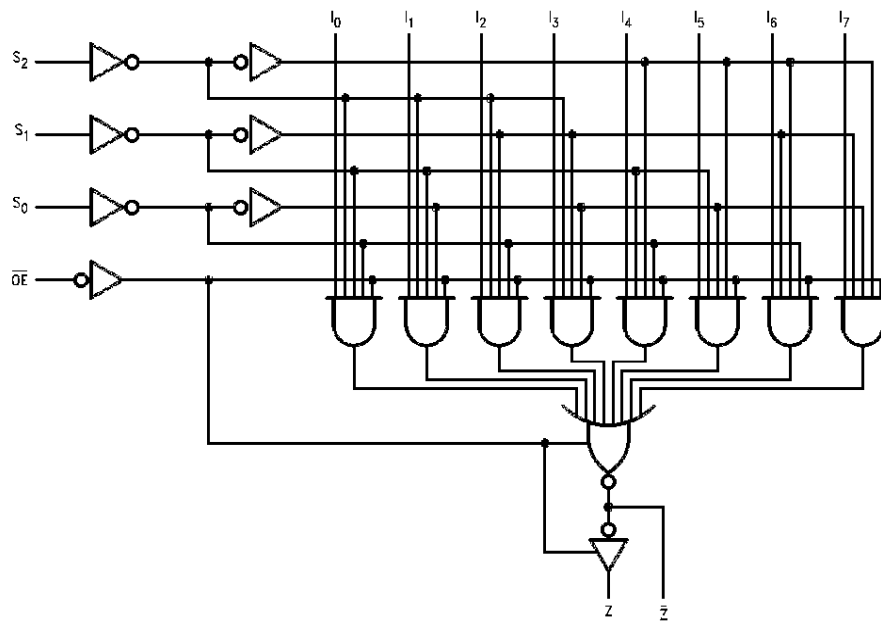
When the Output Enable is HIGH, both outputs are in the high impedance (High Z) state. This feature allows multiplexer expansion by tying the outputs of up to 128 devices together. When the outputs of the 3-STATE devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. The Output Enable signals should be designed to ensure there is no overlap in the active LOW portion of the enable voltages.

Truth Table

| \overline{OE} | Inputs | | | Outputs | |
|-----------------|--------|-------|-------|------------------|-------|
| | S_2 | S_1 | S_0 | \overline{Z} | Z |
| H | X | X | X | Z | Z |
| L | L | L | L | $\overline{I_0}$ | I_0 |
| L | L | L | H | $\overline{I_1}$ | I_1 |
| L | L | H | L | $\overline{I_2}$ | I_2 |
| L | L | H | H | $\overline{I_3}$ | I_3 |
| L | H | L | L | $\overline{I_4}$ | I_4 |
| L | H | L | H | $\overline{I_5}$ | I_5 |
| L | H | H | L | $\overline{I_6}$ | I_6 |
| L | H | H | H | $\overline{I_7}$ | I_7 |

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Logic Diagram



D8009804-4

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays

Absolute Maximum Ratings (Note 3)

| | |
|---|--------------------------|
| Storage Temperature | -65°C to +150°C |
| Ambient Temperature under Bias | -55°C to +125°C |
| Junction Temperature under Bias | -55°C to +175°C |
| Plastic | -55°C to +150°C |
| V _{CC} Pin Potential to Ground Pin | -0.5V to +7.0V |
| Input Voltage (Note 4) | -0.5V to +7.0V |
| Input Current (Note 4) | -30 mA to +5.0 mA |
| Voltage Applied to Output in HIGH State (with V _{CC} = 0V) | |
| Standard Output | -0.5V to V _{CC} |
| 3-STATE Output | -0.5V to +5.5V |
| Current Applied to Output | |

in LOW State (Max)

twice the rated I_{OL} (mA)

Recommended Operating Conditions

| | |
|------------------------------|-----------------|
| Free Air Ambient Temperature | |
| Military | -55°C to +125°C |
| Commercial | 0°C to +70°C |
| Supply Voltage | |
| Military | +4.5V to +5.5V |
| Commercial | +4.5V to +5.5V |

Note 3: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 4: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

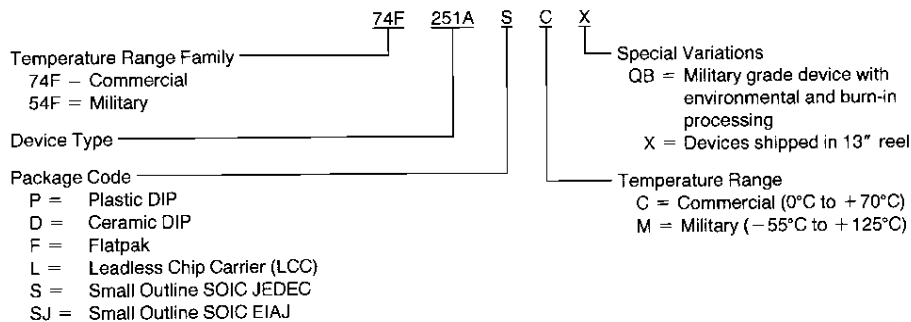
| Symbol | Parameter | 54F/74F | | | Units | V _{CC} | Conditions |
|------------------|-----------------------------------|-------------------------|------|------|-------|-----------------|---|
| | | Min | Typ | Max | | | |
| V _{IH} | Input HIGH Voltage | 2.0 | | | V | | Recognized as a HIGH Signal |
| V _{IL} | Input LOW Voltage | 0.8 | | | V | | Recognized as a LOW Signal |
| V _{CD} | Input Clamp Diode Voltage | -1.2 | | | V | Min | I _{IN} = -18 mA |
| V _{OH} | Output HIGH Voltage | 54F 10% V _{CC} | 2.5 | | V | Min | I _{OH} = -1 mA |
| | | 54F 10% V _{CC} | 2.4 | | | | I _{OH} = -3 mA |
| | | 74F 10% V _{CC} | 2.5 | | | | I _{OH} = -1 mA |
| | | 74F 10% V _{CC} | 2.4 | | | | I _{OH} = -3 mA |
| | | 74F 5% V _{CC} | 2.7 | | | | I _{OH} = -1 mA |
| | | 74F 5% V _{CC} | 2.7 | | | | I _{OH} = -3 mA |
| V _{OL} | Output LOW Voltage | 54F 10% V _{CC} | 0.5 | | V | Min | I _{OL} = 20 mA |
| | | 74F 10% V _{CC} | 0.5 | | | | I _{OL} = 24 mA |
| I _{IH} | Input HIGH Current | 54F | 20.0 | | μA | Max | V _{IN} = 2.7V |
| | | 74F | 5.0 | | | | |
| I _{BVI} | Input HIGH Current Breakdown Test | 54F | 100 | | μA | Max | V _{IN} = 7.0V |
| | | 74F | 7.0 | | | | |
| I _{CEX} | Output HIGH Leakage Current | 54F | 250 | | μA | Max | V _{OUT} = V _{CC} |
| | | 74F | 50 | | | | |
| V _{ID} | Input Leakage Test | 74F | 4.75 | | V | 0.0 | I _{ID} = 1.9 μA All Other Pins Grounded |
| I _{OD} | Output Leakage Circuit Current | 74F | 3.75 | | μA | 0.0 | V _{ID} = 150 mV All Other Pins Grounded |
| I _{IL} | Input LOW Current | | -0.6 | | mA | Max | V _{IN} = 0.5V |
| I _{OZH} | Output Leakage Current | | 50 | | μA | Max | V _{OUT} = 2.7V |
| I _{OZL} | Output Leakage Current | | -50 | | μA | Max | V _{OUT} = 0.5V |
| I _{OS} | Output Short-Circuit Current | | -60 | -150 | mA | Max | V _{OUT} = 0V |
| I _{ZZ} | Bus Drainage Test | | 500 | | μA | 0.0V | V _{OUT} = 5.25V |
| I _{CCL} | Power Supply Current | | 15 | 22 | mA | Max | V _O = LOW |
| I _{CCZ} | Power Supply Current | | 16 | 24 | mA | Max | V _O = HIGH Z |

AC Electrical Characteristics

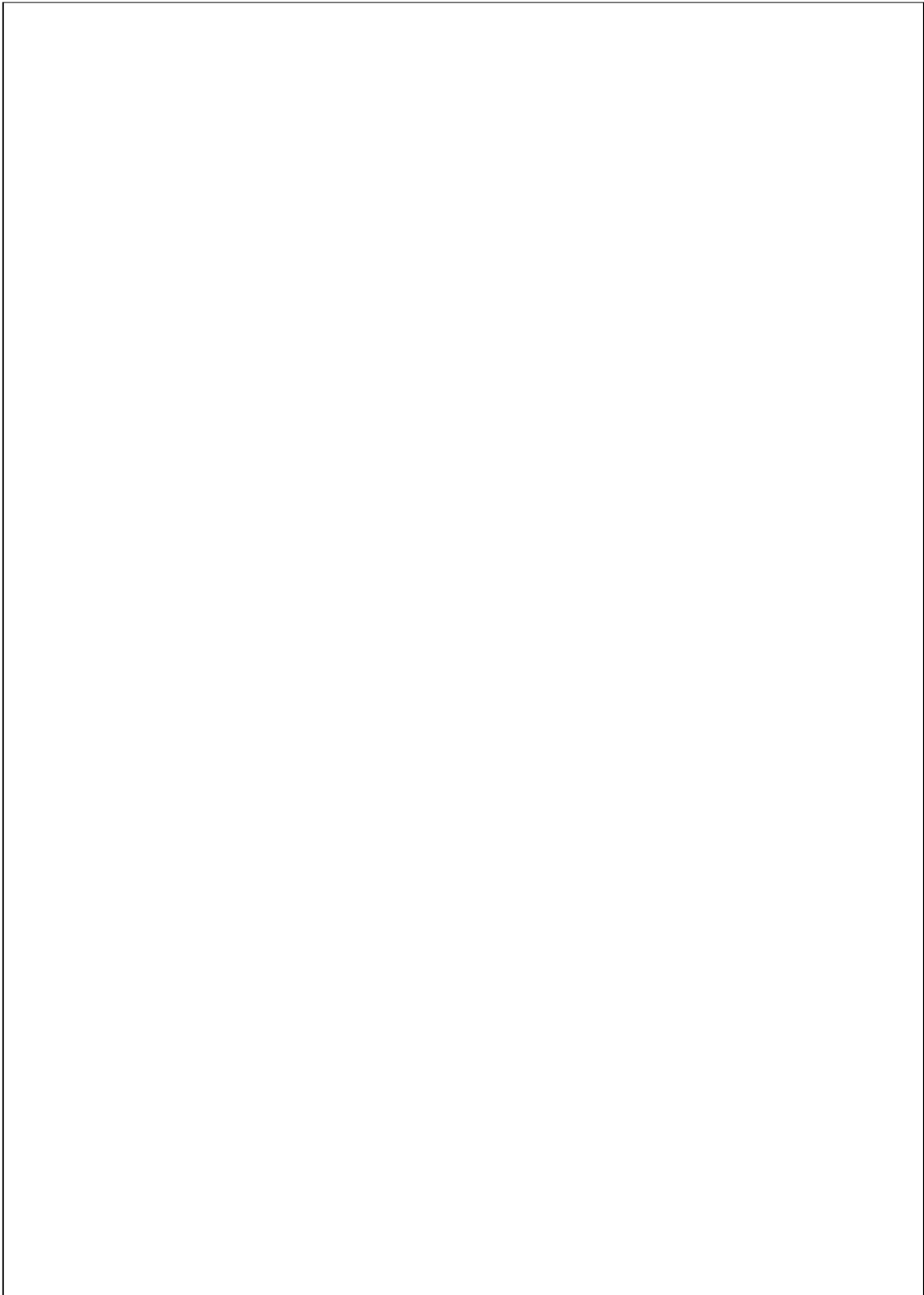
| Symbol | Parameter | 74F | | | 54F | | 74F | | Units |
|------------------|----------------------|---|-----|------|--|------|--|------|-------|
| | | T _A = +25°C V _{CC} = +5.0V C _L = 50 pF | | | T _A , V _{CC} = Mil C _L = 50 pF | | T _A , V _{CC} = Com C _L = 50 pF | | |
| | | Min | Typ | Max | Min | Max | Min | Max | |
| t _{PLH} | Propagation Delay | 3.5 | 6.0 | 9.0 | 3.5 | 11.5 | 3.5 | 9.5 | ns |
| t _{PHL} | S _n to Z̄ | 3.2 | 5.0 | 7.5 | 3.2 | 8.0 | 3.2 | 7.5 | |
| t _{PLH} | Propagation Delay | 4.5 | 7.5 | 10.5 | 3.5 | 14.0 | 4.5 | 12.5 | ns |
| t _{PHL} | S _n to Z | 4.0 | 6.0 | 8.5 | 3.0 | 10.5 | 4.0 | 9.0 | |
| t _{PLH} | Propagation Delay | 3.0 | 5.0 | 6.5 | 2.5 | 8.0 | 3.0 | 7.0 | ns |
| t _{PHL} | I _n to Z̄ | 1.5 | 2.5 | 4.0 | 1.5 | 6.0 | 1.5 | 5.0 | |
| t _{PLH} | Propagation Delay | 3.5 | 5.0 | 7.0 | 2.5 | 9.0 | 2.5 | 8.0 | ns |
| t _{PHL} | I _n to Z | 3.5 | 5.5 | 7.0 | 3.5 | 9.0 | 3.5 | 7.5 | |
| t _{PZH} | Output Enable Time | 2.5 | 4.3 | 6.0 | 2.0 | 7.0 | 2.5 | 7.0 | ns |
| t _{PZL} | OĒ to Z̄ | 2.5 | 4.3 | 6.0 | 2.5 | 7.5 | 2.5 | 6.5 | |
| t _{PHZ} | Output Disable Time | 2.5 | 4.0 | 5.5 | 2.5 | 6.0 | 2.5 | 6.0 | ns |
| t _{PLZ} | OĒ to Z | 1.5 | 3.0 | 4.5 | 1.5 | 5.0 | 1.5 | 4.5 | |
| t _{PZH} | Output Enable Time | 3.5 | 5.0 | 7.0 | 3.0 | 8.5 | 3.0 | 7.5 | ns |
| t _{PZL} | OĒ to Z | 3.5 | 5.5 | 7.5 | 3.5 | 9.0 | 3.5 | 8.0 | |
| t _{PHZ} | Output Disable Time | 2.0 | 3.8 | 5.5 | 2.0 | 5.5 | 2.0 | 5.5 | ns |
| t _{PLZ} | OĒ to Z | 1.5 | 3.0 | 4.5 | 1.5 | 5.5 | 1.5 | 4.5 | |

Ordering Information

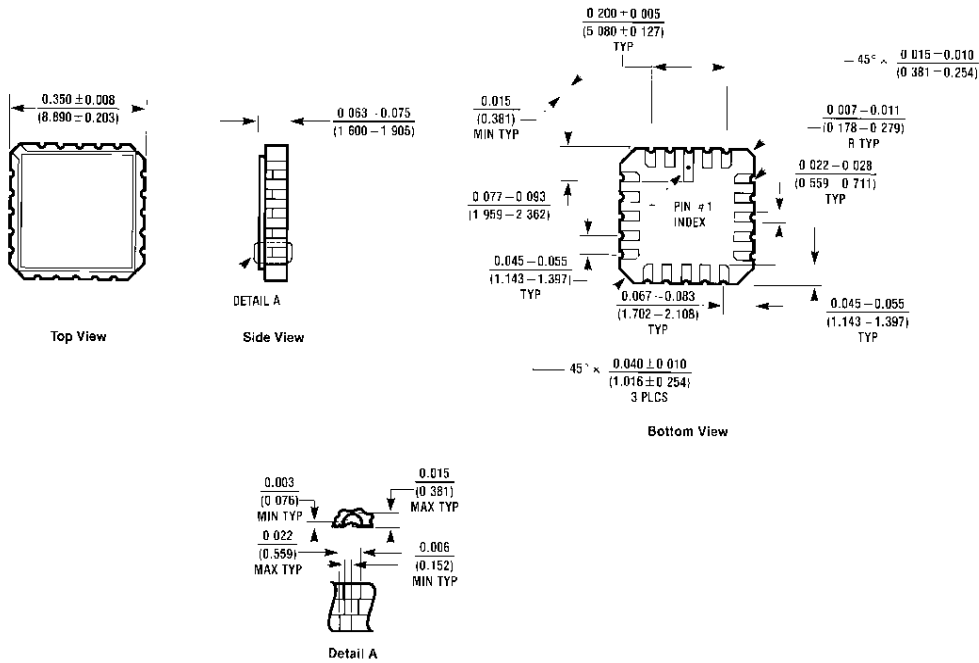
The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



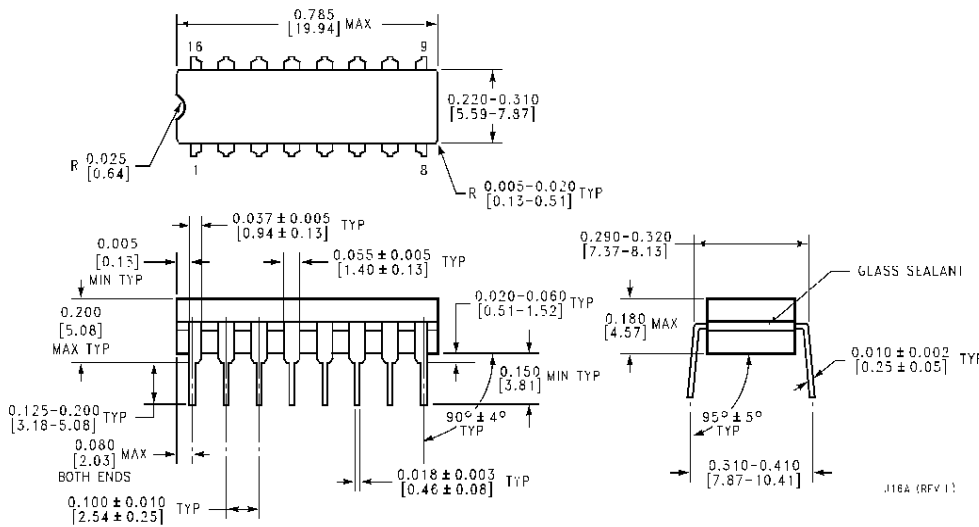
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Physical Dimensions inches (millimeters) unless otherwise noted

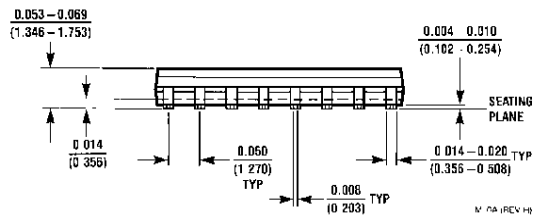
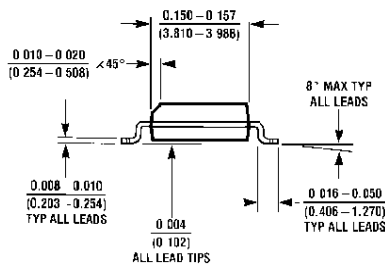
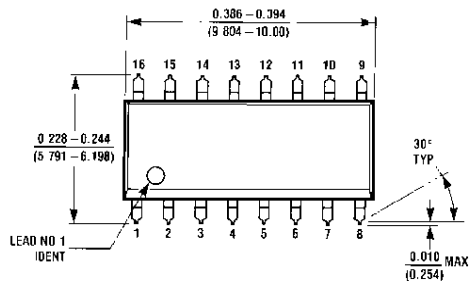


**20-Lead Ceramic Leadless Chip Carrier (L)
 Package Number E20A**

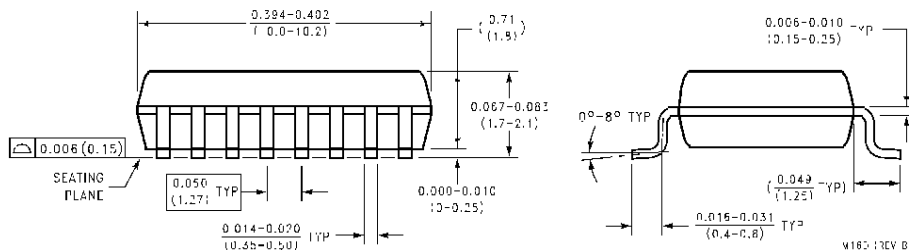
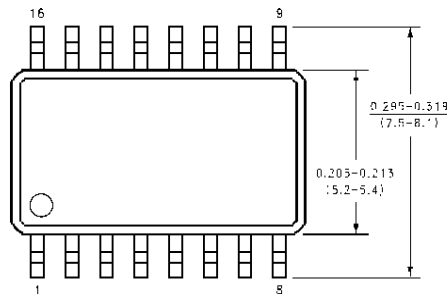


**16-Lead Ceramic Dual-In-Line Package (D)
 Package Number J16A**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

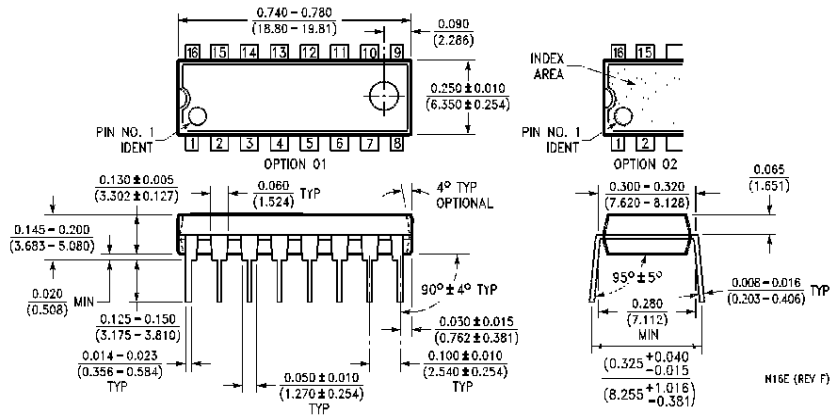


16-Lead (0.150" Wide) Molded Small Outline Package, JEDEC (S)
Package Number M16A

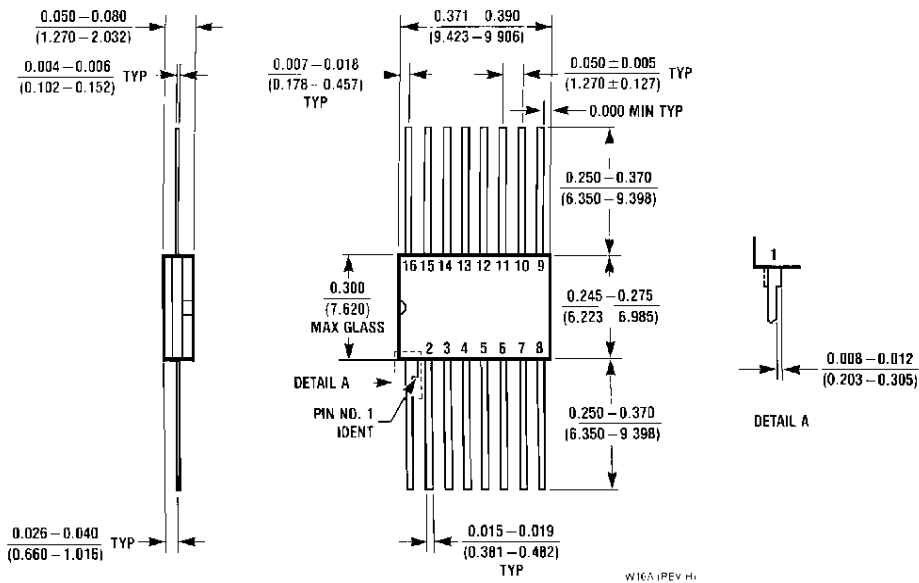


16-Lead (0.300" Wide) Molded Small Outline Package, EIAJ (SJ)
Package Number M16D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead (0.300" Wide) Molded Dual-In-Line Package (P)
Package Number N16E



16-Lead Ceramic Flatpak (F)
Package Number W16A

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