ADVANCE INFORMATION

MX27C8000A

8M-BIT [1M x8] CMOS EPROM

FEATURES

- 1M x 8 organization
- Single +5V power supply
- +12.5V programming voltage
- Fast access time: 120/150 ns
- Totally static operation
- Completely TTL compatible
- Operating current: 60mA
- Standby current: 100uA
- Package type:
  - 32 pin plastic DIP
  - 32 pin PLCC
  - 32 pin SOP
  - 32 pin TSOP

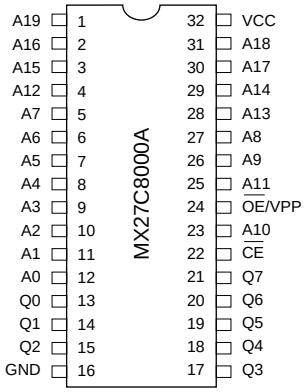
GENERAL DESCRIPTION

The MX27C8000A is a 5V only, 8M-bit, ultraviolet Erasable Programmable Read Only Memory. It is organized as 1M words by 8 bits per word, operates from a single +5 volt supply, has a static standby mode, and features fast single address location programming. All programming signals are TTL levels, requiring a single pulse. For programming outside from the system, existing EPROM programmers may be used. The MX27C8000A supports a intelligent fast programming algorithm which can result in programming time of less than two minutes.

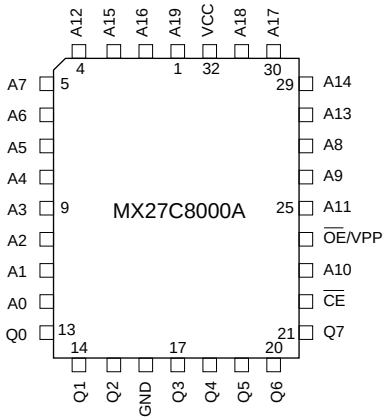
This EPROM is packaged in industry standard 32 pin dual-in-line packages, 32 lead PLCC, 32 lead SOP and 32 lead TSOP packages.

PIN CONFIGURATIONS

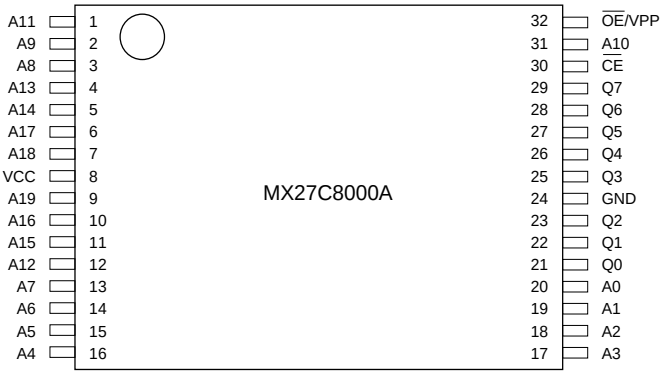
32 PDIP/SOP



32 PLCC



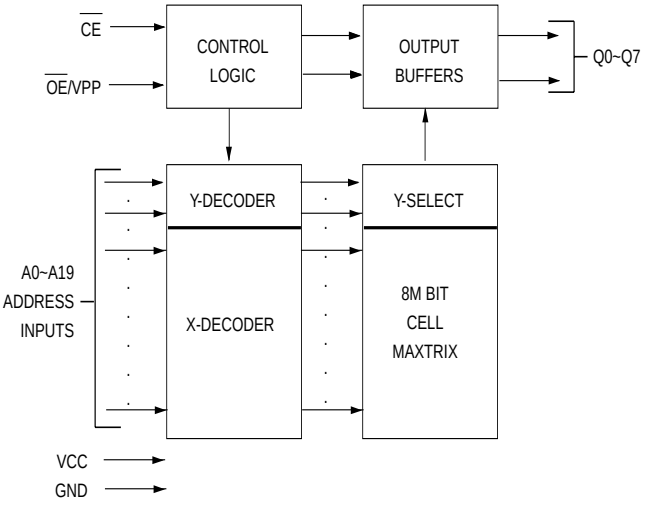
32 TSOP



PIN DESCRIPTION

SYMBOL	PIN NAME
A0~A19	Address Input
Q0~Q7	Data Input/Output
$\overline{CE}$	Chip Enable Input
$\overline{OE}$/VPP	Output Enable Input/Program Supply Voltage
VCC	Power Supply Pin (+5V)
GND	Ground Pin

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

THE PROGRAMMING OF THE MX27C8000A

When the MX27C8000A is delivered, or it is erased, the chip has all 8M bits in the "ONE" or HIGH state. "ZEROs" are loaded into the MX27C8000A through the procedure of programming.

For programming, the data to be programmed is applied with 8 bits in parallel to the data pins.

Vcc must be applied simultaneously or before Vpp, and removed simultaneously or after Vpp. When programming an MXIC EPROM, a 0.1uF capacitor is required across Vpp and ground to suppress spurious voltage transients which may damage the device.

FAST PROGRAMMING

The device is set up in the fast programming mode when the programming voltage $\overline{OE}$/VPP = 12.75V is applied, with VCC = 6.25 V (Algorithm is shown in Figure 1). The programming is achieved by applying twenty-five TTL low level 5us pulses to the $\overline{CE}$ input after addresses and data line are stable. This process is repeated while sequencing through each address of the device. When the programming mode is completed, the data in all address is verified at VCC=5.6V.

PROGRAM INHIBIT MODE

Programming of multiple MX27C8000As in parallel with different data is also easily accomplished by using the Program Inhibit Mode. Except for $\overline{CE}$ and $\overline{OE}$, all like inputs of the parallel MX27C8000A may be common. A TTL low-level program pulse applied to an MX27C8000A $\overline{CE}$ input with $\overline{OE}$/VPP = 12.5 ± 0.5 Vwill program that MX27C8000A. A high-level $\overline{CE}$ input inhibits the other MX27C8000As from being programmed.

PROGRAM VERIFY MODE

Verification should be performed on the programmed bits to determine that they were correctly programmed. The verification should be performed with $\overline{OE}$ /VPPand $\overline{CE}$, at VIL, data should be verified tDV after the falling edge of $\overline{CE}$.

AUTO IDENTIFY MODE

The auto identify mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and device type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25℃ ± 5℃ ambient temperature range that is required when programming the MX27C8000A.

To activate this mode, the programming equipment must force 12.0 ± 0.5 V on address line A9 of the device. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from VIL to VIH. All other address lines must be held at VIL during auto identify mode.

Byte 0 (A0 = VIL) represents the manufacturer code, and byte 1 (A0 = VIH), the device identifier code. For the MX27C8000A, these two identifier bytes are given in the Mode Select Table. All identifiers for manufacturer and device codes will possess odd parity, with the MSB (Q7) defined as the parity bit.

READ MODE

The MX27C8000A has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and

should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (tACC) is equal to the delay from $\overline{CE}$ to output (tCE). Data is available at the outputs tOE after the falling edge of $\overline{OE}$'s, assuming that $\overline{CE}$ has been LOW and addresses have been stable for at least tACC - tOE.

STANDBY MODE

The MX27C8000A has a CMOS standby mode which reduces the maximum VCC current to 100 uA. It is placed in CMOS standby when $\overline{CE}$ is at VCC ± 0.3 V. The MX27C8000A also has a TTL-standby mode which reduces the maximum VCC current to 1.5 mA. It is placed in TTL-standby when $\overline{CE}$ is at VIH. When in standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

TWO-LINE OUTPUT CONTROL FUNCTION

To accommodate multiple memory connections, a two-line control function is provided to allow for:

1. Low memory power dissipation,
2. Assurance that output bus contention will not occur.

It is recommended that $\overline{CE}$ be decoded and used as the primary device-selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

SYSTEM CONSIDERATIONS

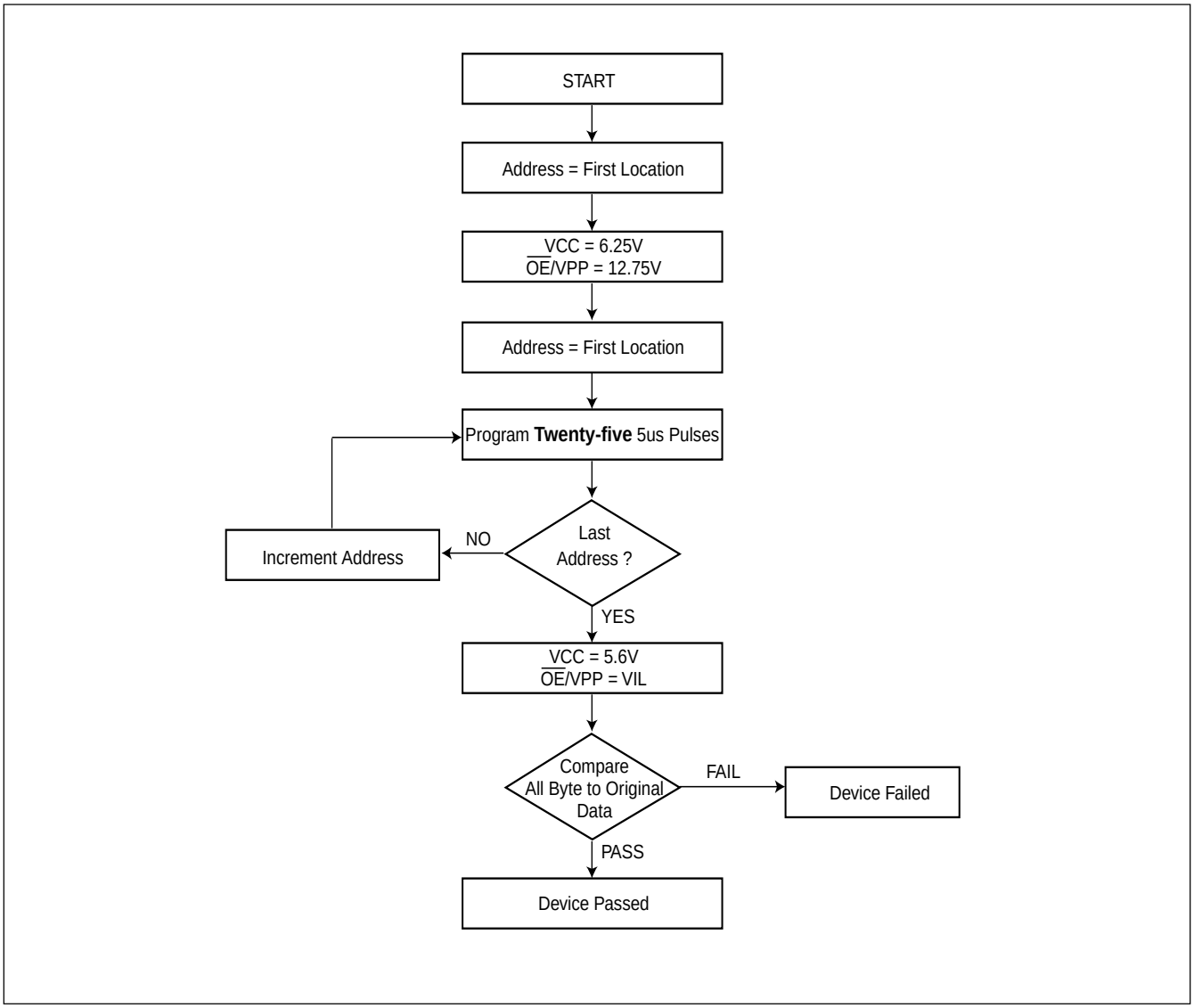
During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1 uF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between VCC and GND to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on EPROM arrays, a 4.7 uF bulk electrolytic capacitor should be used between VCC and GND for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

MODE SELECT TABLE

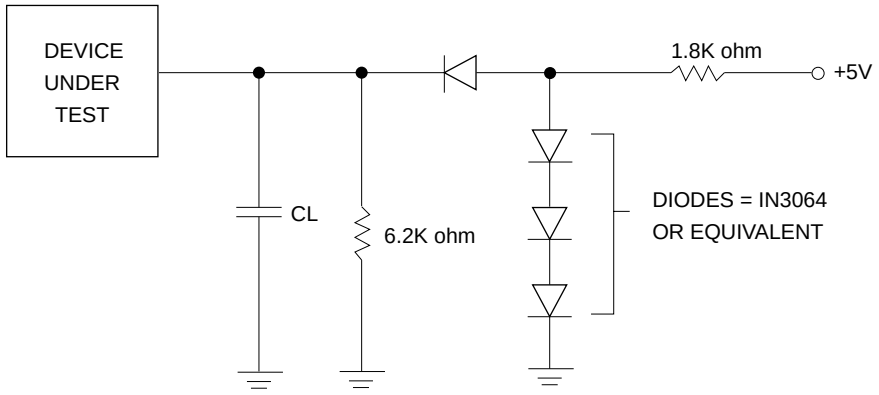
			PINS		
MODE	**$\overline{CE}$**	**$\overline{OE}$/VPP**	**A0**	**A9**	**OUTPUTS**
Read	VIL	VIL	X	X	DOUT
Output Disable	VIL	VIH	X	X	High Z
Standby (TTL)	VIH	X	X	X	High Z
Standby (CMOS)	VCC±0.3V	X	X	X	High Z
Program	VIL	VPP	X	X	DIN
Program Verify	VIL	VIL	X	X	DOUT
Program Inhibit	VIH	VPP	X	X	High Z
Manufacturer Code(3)	VIL	VIL	VIL	VH	C2H
Device Code(3)	VIL	VIL	VIH	VH	02H

NOTES:
1. VH = 12.0 V ± 0.5 V
2. X = Either VIH or VIL
3. A1 - A8 = A10 - A19 = VIL (For auto select)
4. See DC Programming Characteristics for VPP voltage during programming

Figure 1. FAST PROGRAMMING FLOW CHART

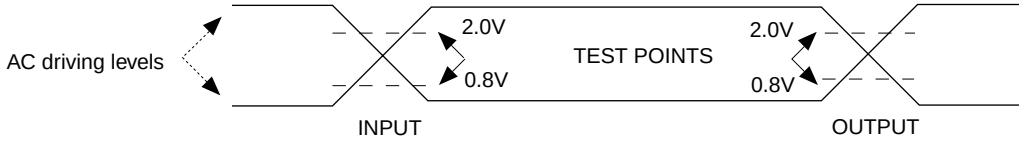


SWITCHING TEST CIRCUITS



CL = 100 pF including jig capacitance

SWITCHING TEST WAVEFORMS



AC TESTING: AC driving levels are 2.4V/0.4V for commercial grade.
Input pulse rise and fall times are ≤ 10ns.

ABSOLUTE MAXIMUM RATINGS

RATING	VALUE
Ambient Operating Temperature	-40°C to 85°C
Storage Temperature	-65°C to 125°C
Applied Input Voltage	-0.5V to 7.0V
Applied Output Voltage	-0.5V to VCC + 0.5V
VCC to Ground Potential	-0.5V to 7.0V
A9 & VPP	-0.5V to 13.5V

NOTICE:
Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.

NOTICE:
Specifications contained within the following tables are subject to change.

DC/AC OPERATING CONDITION FOR READ OPERATION

		MX27C8000A			
		-90	-10	-12	-15
Operating Temperature	Industrial	-40℃ to 85℃	-40℃ to 85℃	-40℃ to 85℃	-40℃ to 85℃
Vcc Power Supply		5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%

DC CHARACTERISTICS

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
VOH	Output High Voltage	2.4		V	IOH = -0.4mA
VOL	Output Low Voltage		0.4	V	IOL = 2.1mA
VIH	Input High Voltage	2.0	VCC + 0.5	V	
VIL	Input Low Voltage	-0.3	0.8	V	
ILI	Input Leakage Current	-10	10	uA	VIN = 0 to 5.5V
ILO	Output Leakage Current	-10	10	uA	VOUT = 0 to 5.5V
ICC3	VCC Power-Down Current		100	uA	$\overline{CE}$ = VCC ± 0.3V
ICC2	VCC Standby Current		1.5	mA	$\overline{CE}$ = VIH
ICC1	VCC Active Current		60	mA	$\overline{CE}$ = VIL, f=5MHz, Iout = 0mA
IPP	VPP Supply Current Read		10	uA	$\overline{CE}$ = $\overline{OE}$ = VIL, VPP = 5.5V

CAPACITANCE TA = 25°C, f = 1.0 MHz (Sampled only)

SYMBOL	PARAMETER	TYP.	MAX.	UNIT	CONDITIONS
CIN	Input Capacitance	8	12	pF	VIN = 0V
COUT	Output Capacitance	8	12	pF	VOUT = 0V
CVPP	VPP Capacitance	18	25	pF	VPP = 0V

AC CHARACTERISTICS

		27C8000A-12		27C8000A-15			
Symbol	**PARAMETER**	**MIN.**	**MAX.**	**MIN.**	**MAX.**	**Unit**	**Conditions**
tACC	Address to Output Delay		120		150	ns	$\overline{CE}$=$\overline{OE}$=VIL
tCE	Chip Enable to Output Delay		120		150	ns	$\overline{OE}$=VIL
tOE	Output Enable to Output Delay		50		65	ns	$\overline{CE}$=VIL
tDF	$\overline{OE}$ High to Output Float, or $\overline{CE}$ High to Output Float	0	35	0	50	ns	
tOH	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$ which ever occurred first		0		0	ns	

DC PROGRAMMING CHARACTERISTICS TA = 25°C ± 5°C

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
VOH	Output High Voltage	2.4		V	IOH = -0.40mA
VOL	Output Low Voltage		0.4	V	IOL = 2.1mA
VIH	Input High Voltage	2.0	VCC + 0.5	V	
VIL	Input Low Voltage	-0.3	0.8	V	
ILI	Input Leakage Current	-10	10	uA	VIN = 0 to 5.5V
VH	A9 Auto Select Voltage	11.5	12.5	V	
ICC3	VCC Supply Current (Program & Verify)		50	mA	
IPP2	VPP Supply Current (Program)		30	mA	$\overline{CE}$ = VIL
VCC1	Fast Programming Supply Voltage	6.00	6.50	V	
VPP1	Fast Programming Voltage	12.5	13.0	V	

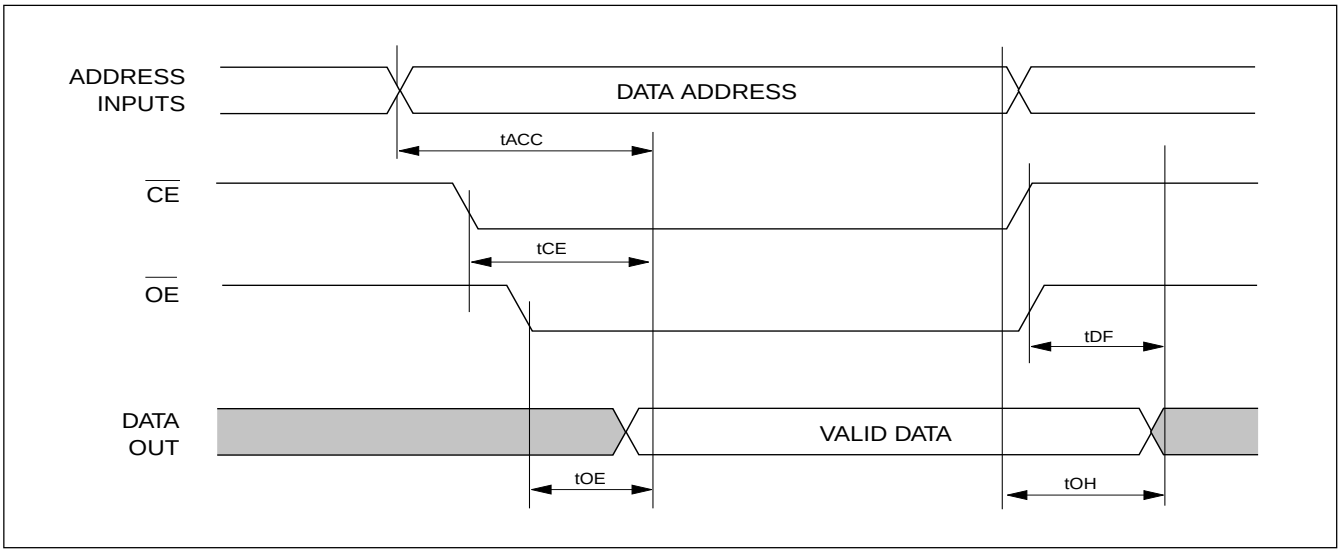
AC PROGRAMMING CHARACTERISTICS TA = 25°C ± 5°C

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
tAS	Address Setup Time	2.0			us
tDS	Data Setup Time	2.0			us
tAH	Address Hold Time	0			us
tDH	Data Hold Time	2.0			us
tDFP	Chip Enable to Output Float Delay	0		130	ns
tVPS	VPP Setup Time	2.0			us
tPW	$\overline{CE}$ Program Pulse Width	5 (Note)			us
tVCS	VCC Setup Time	2.0			us
tDV	Data Valid from $\overline{CE}$			150	ns
tOEH	$\overline{OE}$/VPP Hold Time	2.0			us
tVR	$\overline{OE}$/VPP Recovery Time	2.0			us

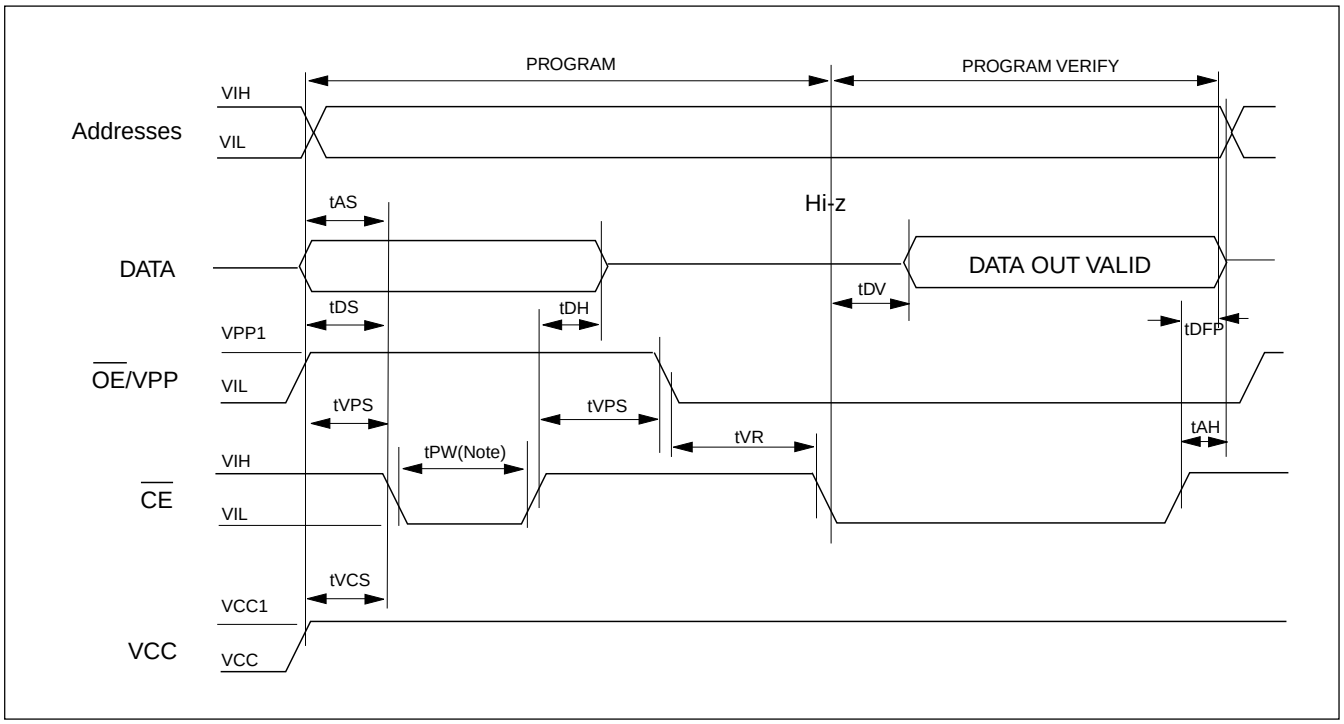
Note : For effective program operation, tPW is recommanded to be 5us.

WAVEFORMS

READ CYCLE



FAST PROGRAMMING ALGORITHM WAVEFORMS



Note : tPW requires 25 pulses.

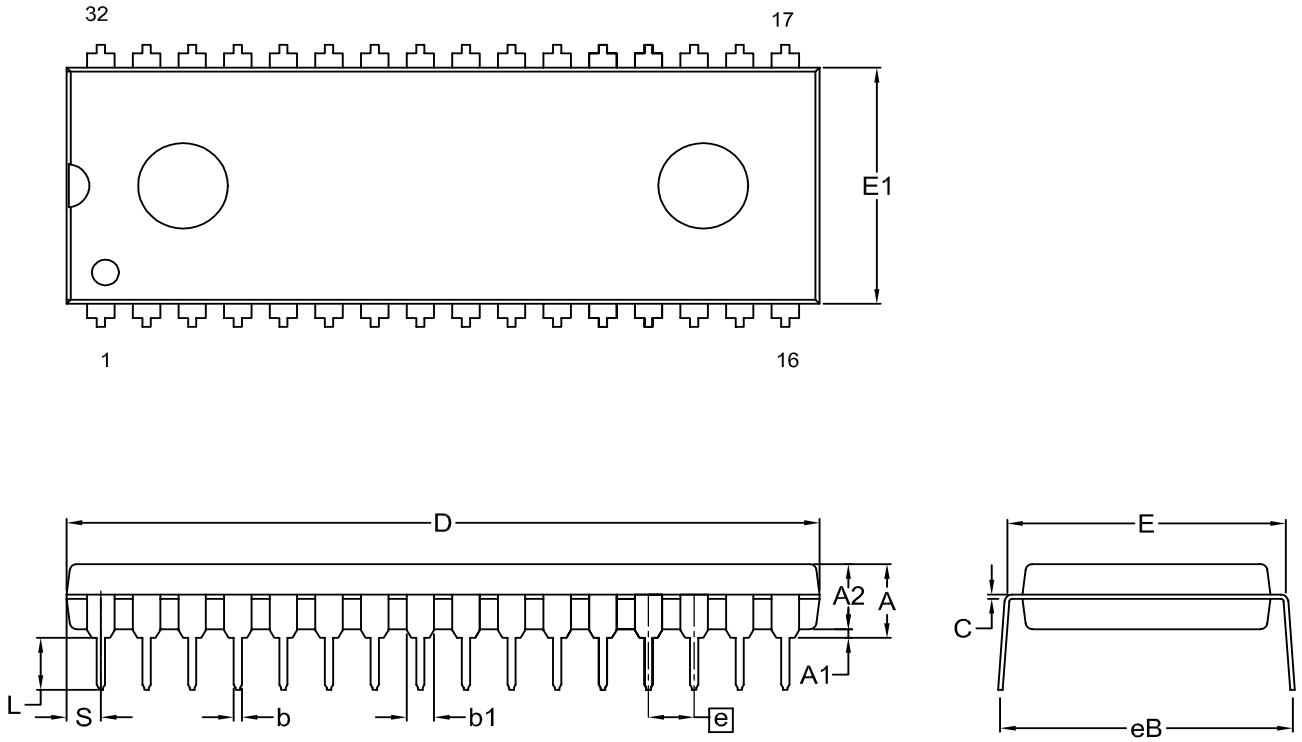
ORDERING INFORMATION

PLASTIC PACKAGE

PART NO.	ACCESS TIME (ns)	OPERATING Current MAX.(mA)	STANDBY Current MAX.(uA)	OPERATING TEMPERATURE	PACKAGE
MX27C8000APC-12	120	30	100	0℃ to 70℃	32 Pin DIP
MX27C8000AQC-12	120	30	100	0℃ to 70℃	32 Pin PLCC
MX27C8000AMC-12	120	30	100	0℃ to 70℃	32 Pin SOP
MX27C8000ATC-12	120	30	100	0℃ to 70℃	32 Pin TSOP
MX27C8000APC-15	150	30	100	0℃ to 70℃	32 Pin DIP
MX27C8000AQC-15	150	30	100	0℃ to 70℃	32 Pin PLCC
MX27C8000AMC-15	150	30	100	0℃ to 70℃	32 Pin SOP
MX27C8000ATC-15	150	30	100	0℃ to 70℃	32 Pin TSOP

PACKAGE INFORMATION

Title: Package Outline for PDIP 32L(600MIL)

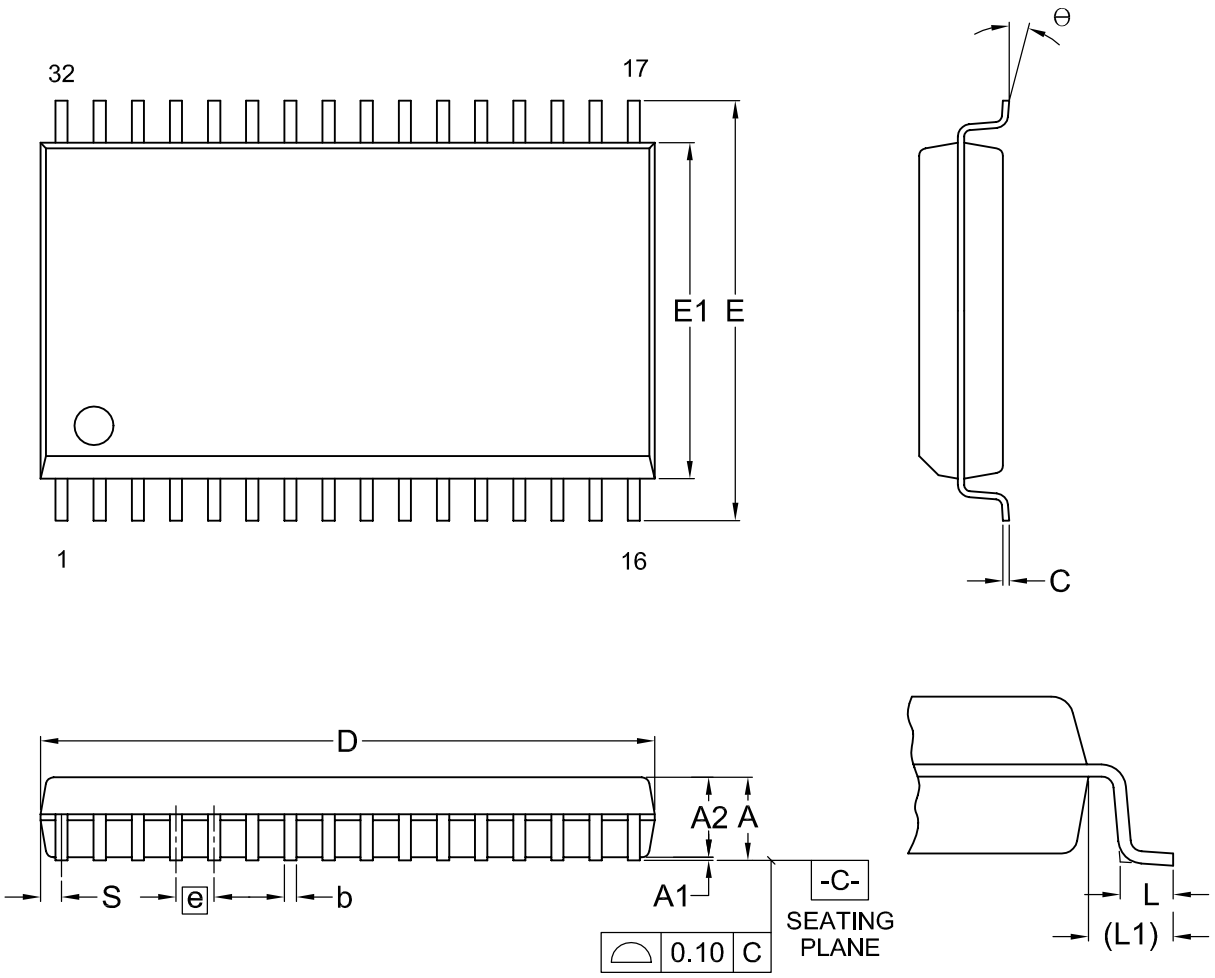


Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	b1	C	D	E	E1	e	eB	L	S
mm	Min.	---	0.51	3.73	0.38	1.14	0.20	41.78	15.11	13.84		15.75	2.92	1.65
	Nom.	---	0.64	3.94	0.46	1.27	0.25	41.91	15.24	13.97	2.54	16.51	3.30	1.90
	Max.	4.90	0.76	4.14	0.53	1.40	0.30	42.04	15.37	14.10		17.27	3.68	2.16
Inch	Min.	---	0.020	0.147	0.015	0.045	0.008	1.645	0.595	0.545		0.620	0.115	0.065
	Nom.	---	0.025	0.155	0.018	0.050	0.010	1.650	0.600	0.550	0.100	0.650	0.130	0.075
	Max.	0.193	0.030	0.163	0.021	0.055	0.012	1.655	0.605	0.555		0.680	0.145	0.085

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-0202.2	5				07-04-'02

Title: **Package Outline for SOP 32L (450MIL)**

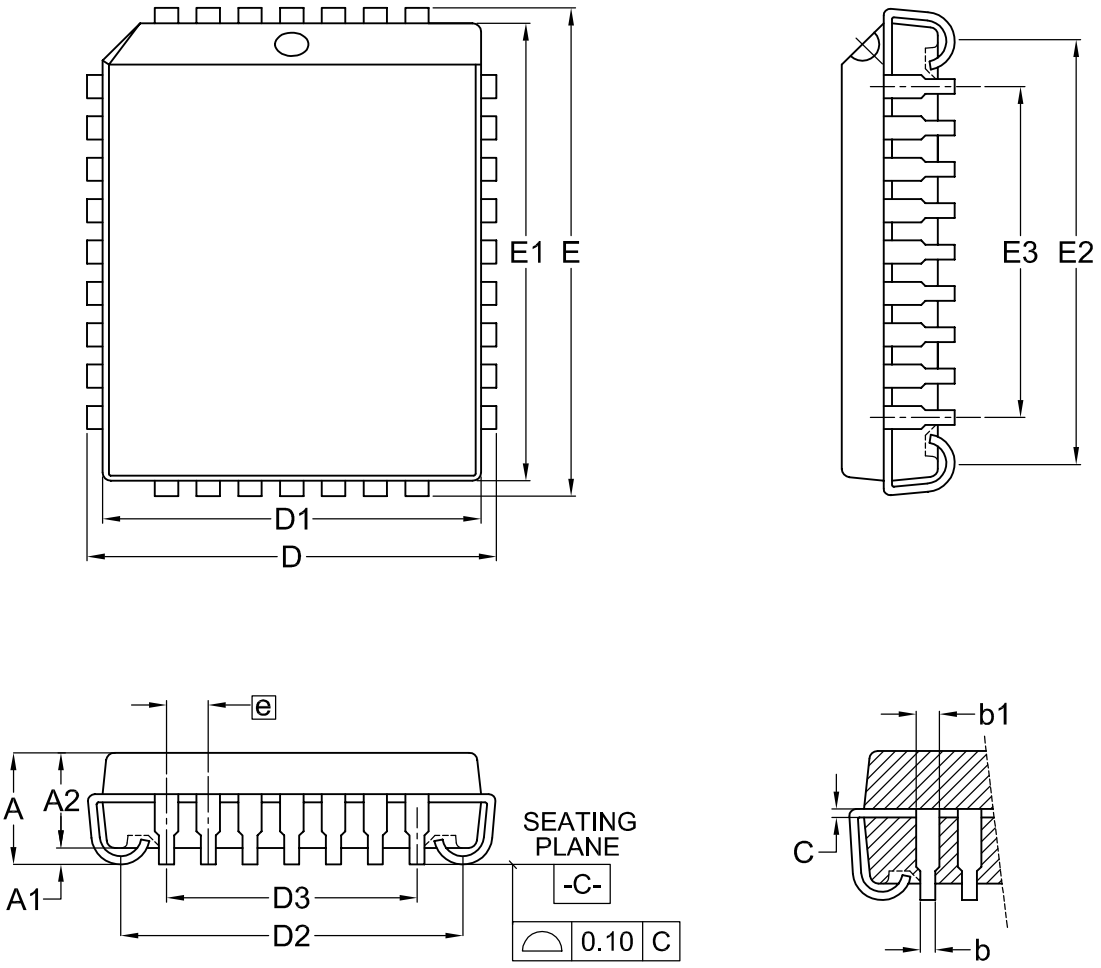


Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	C	D	E	E1	e	L	L1	S	θ
mm	Min.	---	0.10	2.59	0.36	0.15	20.32	13.92	11.18		0.56	1.20	0.58	0
	Nom.	---	0.15	2.69	0.41	0.20	20.45	14.12	11.30	1.27	0.76	1.40	0.70	5
	Max.	3.00	0.20	2.80	0.51	0.25	20.57	14.32	11.43		0.96	1.60	0.83	8
Inch	Min.	---	0.004	0.102	0.014	0.006	0.800	0.548	0.440		0.022	0.047	0.023	0
	Nom.	—	0.006	0.106	0.016	0.008	0.805	0.556	0.445	0.050	0.030	0.055	0.028	5
	Max.	0.118	0.008	0.110	0.020	0.010	0.810	0.564	0.450		0.038	0.063	0.033	8

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-1404	4	MO-099			09-24-'02

Title: **Package Outline for 32L PLCC**

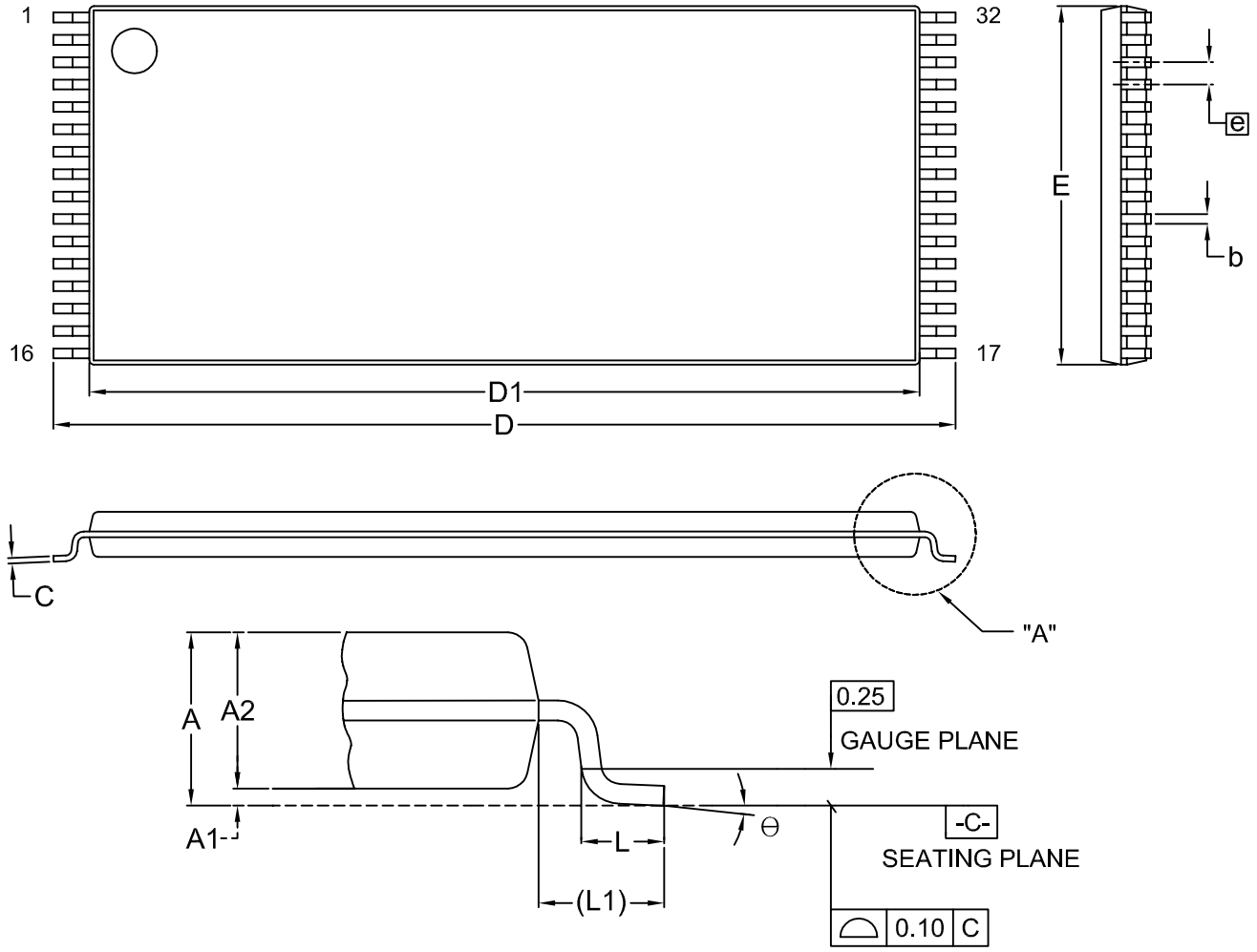


Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	b1	C	D	D1	D2	D3	E	E1	E2	E3	e
mm	Min.	—	0.38	2.69	0.38	0.61	0.20	12.32	11.44	10.11		14.86	13.98	12.65		
	Nom.	—	0.50	2.79	0.46	0.71	0.25	12.45	11.51	10.41	7.62	14.99	14.05	12.95	10.16	1.27
	Max.	3.55	0.66	2.89	0.54	0.81	0.30	12.58	11.58	10.71		15.12	14.12	13.25		
Inch	Min.	---	0.015	0.106	0.015	0.024	0.008	0.485	0.450	0.398		0.585	0.550	0.498		
	Nom.	---	0.020	0.110	0.018	0.028	0.010	0.490	0.453	0.410	0.300	0.590	0.553	0.510	0.400	0.050
	Max.	0.140	0.026	0.114	0.021	0.032	0.012	0.495	0.456	0.422		0.595	0.556	0.522		

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-2002	4	MS-016			09-24-'02

Title: **Package Outline for TSOP(I) 32L (8X20mm)**



DETAIL"A"

Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	C	D	D1	E	e	L	L1	Θ
mm	Min.	---	0.05	0.95	0.17	0.10	19.80	18.30	7.90		0.50	0.70	0
	Nom.	---	0.10	1.00	0.20	0.15	20.00	18.40	8.00	0.50	0.60	0.80	5
	Max.	1.20	0.15	1.05	0.27	0.21	20.20	18.50	8.10		0.70	0.90	8
Inch	Min.	---	0.002	0.037	0.007	0.004	0.780	0.720	0.311		0.020	0.028	0
	Nom.	---	0.004	0.039	0.008	0.006	0.787	0.724	0.315	0.020	0.024	0.031	5
	Max.	0.047	0.006	0.041	0.011	0.008	0.795	0.728	0.319		0.028	0.035	8

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-1604	8	MO-142			09-24-'02

REVISION HISTORY

Revision No.	Description	Page	Date
1.1	To change data sheet title to Advance Information	P1	MAR/15/2001
	To added access time 90ns and 32SOP/TSOP type package	P1,6,7,9,11	
	To changed ID Code from 35H to 02H	P6	
1.2	To modify Package Information	P10~13	JUL/19/2001
1.3	1. To revise the program algorithm	P2,4,5	AUG/30/2002
	2. To remove the 90ns and 100ns speed grade	P1,7,9	
	3. To remove the industrial grade	P9	
1.4	To modify Package Information	P10~13	NOV/20/2002

MACRONIX INTERNATIONAL CO., LTD.

HEADQUARTERS:
TEL:+886-3-578-6688
FAX:+886-3-563-2888

EUROPE OFFICE:
TEL:+32-2-456-8020
FAX:+32-2-456-8021

JAPAN OFFICE:
TEL:+81-44-246-9100
FAX:+81-44-246-9105

SINGAPORE OFFICE:
TEL:+65-348-8385
FAX:+65-348-8096

TAIPEI OFFICE:
TEL:+886-2-2509-3300
FAX:+886-2-2509-2200

MACRONIX AMERICA, INC.
TEL:+1-408-453-8088
FAX:+1-408-453-8488

CHICAGO OFFICE:
TEL:+1-847-963-1900
FAX:+1-847-963-1909

http : //www.macronix.com