



## Improved Current Mode PWM Controller

### FEATURES

- Pin for Pin Compatible with the UC1846
- 65ns Typical Delay from Shutdown to Outputs, and 50ns Typical Delay from Sync to Outputs
- Improved Current Sense Amplifier with Reduced Noise Sensitivity
- Differential Current Sense with 3V Common Mode Range
- Trimmed Oscillator Discharge Current for Accurate Deadband Control
- Accurate 1V Shutdown Threshold
- High Current Dual Totem Pole Outputs (1.5A peak)
- TTL Compatible Oscillator Sync Pin Thresholds
- 4kV ESD Protection

### DESCRIPTION

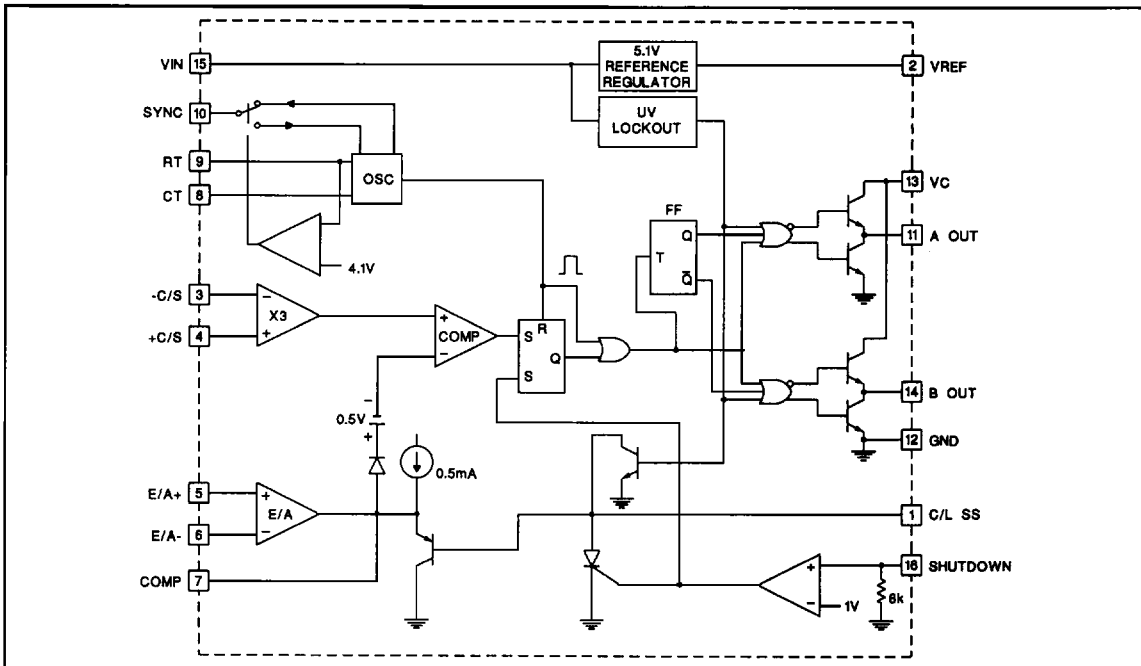
The UC1856 is a high performance version of the popular UC1846 series of current mode controllers, and is intended for both design upgrades and new applications where speed and accuracy are important. All input to output delays have been minimized, and the Current Sense output is slew rate limited to reduce noise sensitivity. Fast 1.5 amp peak output stages have been added to allow rapid switching of power FETs.

A low impedance TTL compatible sync output has been implemented with a tri-state function when used as a sync input.

Internal chip grounding has been improved to minimize internal "noise" caused when driving large capacitive loads. This, in conjunction with the improved differential current sense amplifier results in enhanced noise immunity.

Other features include a trimmed oscillator current (8%) for accurate frequency and dead time control; a 1 volt, 5% shutdown threshold; and 4kV minimum ESD protection on all pins.

### BLOCK DIAGRAM



**ABSOLUTE MAXIMUM RATINGS**

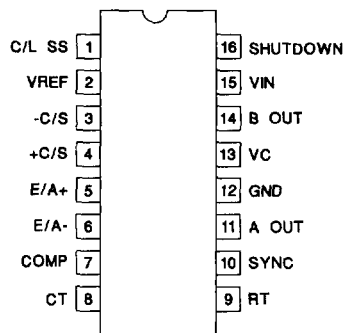
Supply Voltage .....	+40V
Collector Supply Voltage .....	+40V
Output Current, Source or Sink	
DC .....	0.5A
Pulse (0.5 $\mu$ s) .....	2.0A
Error Amp Inputs .....	-0.3V to +VIN
Shutdown Input .....	-0.3V to +10V
Current Sense Inputs .....	-0.3V to +3V
Sync Output Current .....	$\pm$ 10mA
Error Amplifier Output Current .....	-5mA
Soft Start Sink Current .....	50mA
Oscillator Charging Current .....	5mA
Power Dissipation at TA = 25°C (Note 2) .....	1000mW
Power Dissipation at Tc = 25°C (Note 2) .....	2000mW
Storage Temperature Range .....	-65°C to +150°C
Lead Temperature (soldering, 10 seconds) .....	+300°C

All voltages are with respect to Ground. Currents are positive into, negative out of the specified terminal.

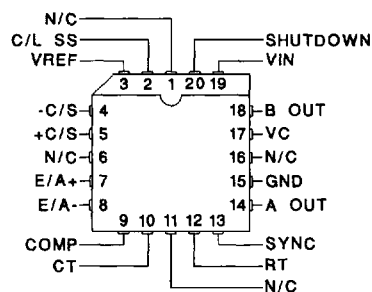
Consult packaging section of databook for thermal limitations and considerations of package.

**CONNECTION DIAGRAMS**

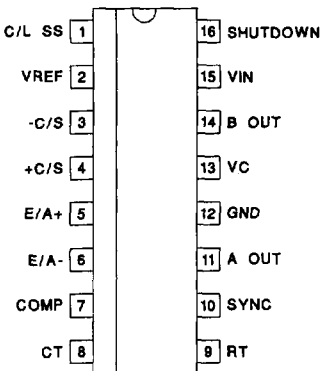
**DIL-16 (TOP VIEW)**  
J or N PACKAGE



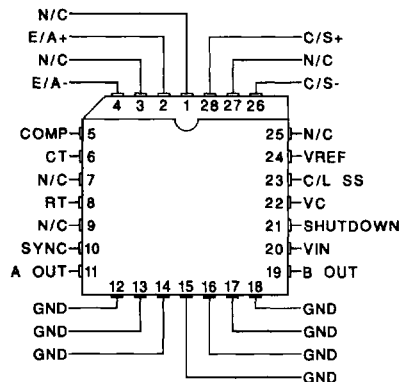
**PLCC-20 (TOP VIEW)**  
Q PACKAGE



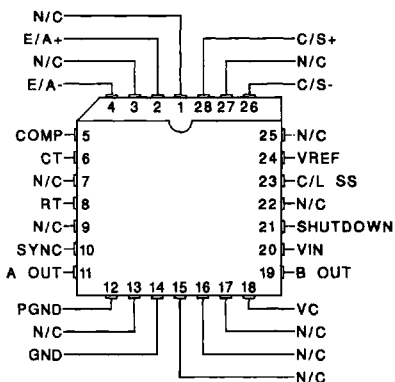
**SOIC-16 (TOP VIEW)**  
DW PACKAGE



**PLCC-28 (TOP VIEW)**  
QP PACKAGE



**LCC-28 (TOP VIEW)**  
L PACKAGE



**ELECTRICAL CHARACTERISTICS** Unless otherwise stated, these specifications apply for  $T_A = -55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  for UC1856;  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  for the UC2856; and  $0^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$  for the UC3856,  $V_{IN} = 15\text{V}$ ,  $R_T = 10\text{k}$ ,  $C_T = 1\text{nF}$ ,  $T_A = T_J$ .

**UC1856**  
**UC2856**  
**UC3856**

PARAMETER	TEST CONDITIONS	UC1856 UC2856			UC3856			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
<b>Reference Section</b>								
Output Voltage	$T_J = 25^{\circ}\text{C}$ , $I_o = 1\text{mA}$	5.05	5.10	5.15	5.00	5.10	5.20	V
Line Regulation	$V_{IN} = 8$ to $40\text{V}$			20			20	mV
Load Regulation	$I_o = -1\text{mA}$ to $-10\text{mA}$			15			15	mV
Total Output Variation	Line, Load, and Temperature	5.00		5.20	4.95		5.25	V
Output Noise Voltage	$10\text{Hz} < f < 10\text{kHz}$ , $T_J = 25^{\circ}\text{C}$		50			50		$\mu\text{V}$
Long Term Stability	$T_J = 125^{\circ}\text{C}$ , 1000Hrs (Note 2)		5	25		5	25	mV
Short Circuit Current	$V_{REF} = 0\text{V}$	-25	-45	-65	-25	-45	-65	mA
<b>Oscillator Section</b>								
Initial Accuracy	$T_J = 25^{\circ}\text{C}$	180	200	220	180	200	220	kHz
	Over Operating Range	170		230	170		230	kHz
Voltage Stability	$V_{IN} = 8$ to $40\text{V}$			2			2	%
Discharge Current	$T_J = 25^{\circ}\text{C}$ , $V_{CT} = 2\text{V}$	7.5	8.0	8.8	7.5	8.0	8.8	mA
	$V_{CT} = 2\text{V}$	6.7	8.0	8.8	6.7	8.0	8.8	mA
Sync Output High Level	$I_o = -1\text{mA}$	2.4	3.6		2.4	3.6		V
Sync Output Low Level	$I_o = +1\text{mA}$		0.2	0.4		0.2	0.4	V
Sync Input High Level	$C_T = 0\text{V}$ , $R_T = V_{REF}$	2.0	1.5		2.0	1.5		V
Sync Input Low Level	$C_T = 0\text{V}$ , $R_T = V_{REF}$		1.5	0.8		1.5	0.8	V
Sync Input Current	$C_T = 0\text{V}$ , $R_T = V_{REF}$ $V_{SYNC} = 5\text{V}$		1	10		1	10	$\mu\text{A}$
Sync Delay to Outputs	$C_T = 0\text{V}$ , $R_T = V_{REF}$ $V_{SYNC} = 0.8\text{V}$ to $2\text{V}$		50	100		50	100	ns
<b>Error Amp Section</b>								
Input Offset Voltage	$V_{CM} = 2\text{V}$			5			10	mV
Input Bias Current				-1			-1	$\mu\text{A}$
Input Offset Current				500			500	nA
Common Mode Range	$V_{IN} = 8$ to $40\text{V}$	0		$V_{IN} - 2$	0		$V_{IN} - 2$	V
Open Loop Gain	$V_o = 1.2$ to $3\text{V}$	80	100		80	100		dB
Unity Gain Bandwidth	$T_J = 25^{\circ}\text{C}$	1	1.5		1	1.5		MHz
CMRR	$V_{CM} = 0$ to $38\text{V}$ , $V_{IN} = 40\text{V}$	75	100		75	100		dB
PSRR	$V_{IN} = 8$ to $40\text{V}$	80	100		80	100		dB
Output Sink Current	$V_{ID} = -15\text{mV}$ , $V_{comp} = 1.2\text{V}$	5	10		5	10		mA
Output Source Current	$V_{ID} = 15\text{mV}$ , $V_{comp} = 2.5\text{V}$	-0.4	-0.5		-0.4	-0.5		mA
Output High Level	$V_{ID} = 50\text{mV}$ , $R_L$ (COMP) = $15\text{k}$	4.3	4.6	4.9	4.3	4.6	4.9	V
Output Low Level	$V_{ID} = -50\text{mV}$ , $R_L$ (COMP) = $15\text{k}$		0.7	1		0.7	1	V
<b>Current Sense Amplifier Section</b>								
Amplifier Gain	$V_{-C/S} = 0\text{V}$ , CL SS Open (Notes 3,4)	2.5	2.75	3.0	2.5	2.75	3.0	V/V
Maximum Differential Input Signal ( $V_{+C/S} - V_{-C/S}$ )	CL SS Open (Note 3) $R_L$ (COMP) = $15\text{k}$	1.1	1.2		1.1	1.2		V
Input Offset Voltage	$V_{CL SS} = 0.5\text{V}$ COMP Open (Note 3)		5	35		5	35	mV
CMRR	$V_{CM} = 0$ to $3\text{V}$	60			60			dB
PSRR	$V_{IN} = 8$ to $40\text{V}$	60			60			dB
Input Bias Current	$V_{CL SS} = 0.5\text{V}$ , COMP Open (Note 3)			-1	-3	-1	-3	$\mu\text{A}$

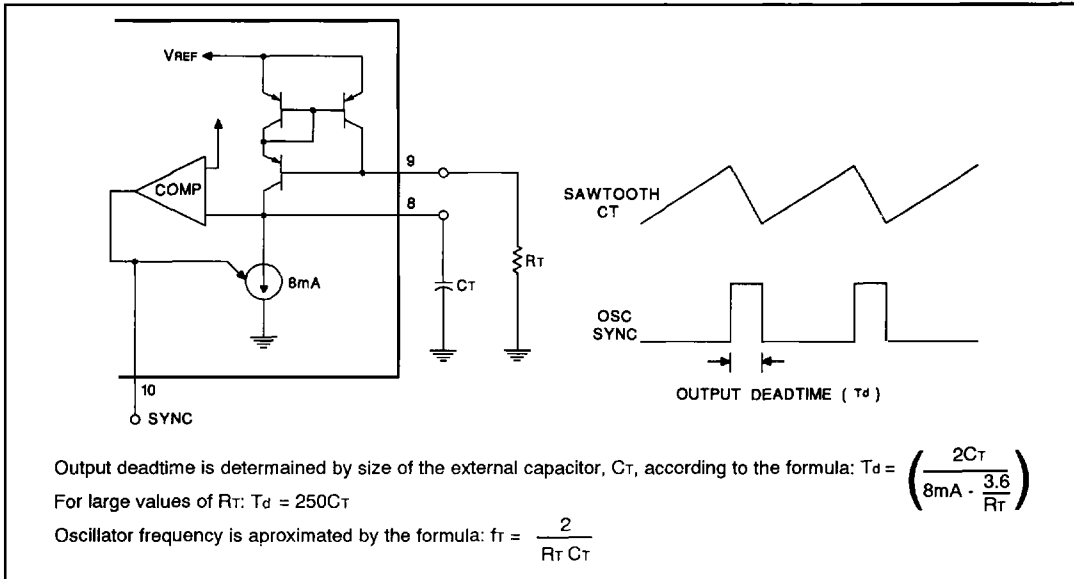
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**UC1856**  
**UC2856**  
**UC3856**

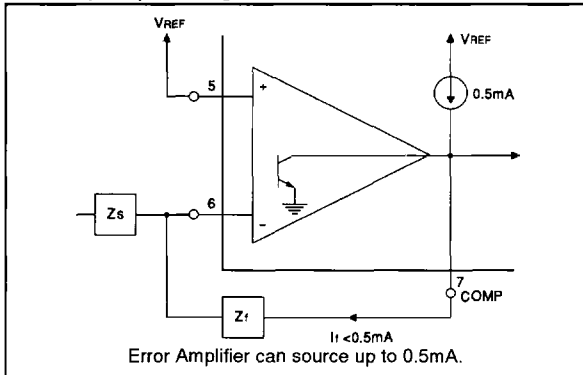
PARAMETER	TEST CONDITIONS	UC1856 UC2856			UC3856			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
<b>Current Sense Amplifier Section (Continued)</b>								
Input Offset Current	$V_{CLSS} = 0.5\text{V}$ , COMP Open (Note 3)			1			1	$\mu\text{A}$
Input Common Mode Range		0		3	0		3	V
Delay to Outputs	$V_{E/A+} = V_{REF}$ , $E/A = 0\text{V}$ $+C/S - -C/S = 0$ to $1.5\text{V}$		120	250		120	250	ns
<b>Current Limit Adjust Section</b>								
Current Limit Offset	$V_{-C/S} = 0\text{V}$ $V_{+C/S} = 0\text{V}$ , COMP = Open (Note 3)	0.43	0.5	0.57	0.43	0.5	0.57	V
Input Bias Current	$V_{E/A+} = V_{REF}$ , $V_{E/A-} = 0\text{V}$		-10	-30		-10	-30	$\mu\text{A}$
<b>Shutdown Terminal Section</b>								
Threshold Voltage		0.95	1.00	1.05	0.95	1.00	1.05	V
Input Voltage Range		0		5	0		5	V
Minimum Latching Current (I <sub>CLSS</sub> )	(Note 5)	3	1.5		3	1.5		mA
Maximum Non-Latching Current (I <sub>CLSS</sub> )	(Note 6)		1.5	0.8		1.5	0.8	mA
Delay to Outputs	$V_{SHUTDOWN} = 0$ to $1.3\text{V}$		65	110		65	110	ns
<b>Output Section</b>								
Collector-Emitter Voltage		40			40			V
Off-State Bias Current	$V_C = 40\text{V}$			250			250	$\mu\text{A}$
Output Low Level	$I_{OUT} = 20\text{mA}$		0.1	0.5		0.1	0.5	V
	$I_{OUT} = 200\text{mA}$		0.5	2.6		0.5	2.6	V
Output High Level	$I_{OUT} = -20\text{mA}$	12.5	13.2		12.5	13.2		V
	$I_{OUT} = -200\text{mA}$	12	13.1		12	13.1		V
Rise Time	$C_1 = 1\text{nF}$		40	80		40	80	ns
Fall Time	$C_1 = 1\text{nF}$		40	80		40	80	ns
UVLO Low Saturation	$V_{IN} = 0\text{V}$ , $I_{OUT} = 20\text{mA}$		0.8	1.5		0.8	1.5	V
<b>PWM Section</b>								
Maximum Duty Cycle		45	47	50	45	47	50	%
Minimum Duty Cycle				0			0	%
<b>Under-Voltage Lockout Section</b>								
Start-Up Threshold			7.7	8.0		7.7	8.0	V
Threshold Hysteresis			0.7			0.7		V
<b>Total Standby Current</b>								
Supply Current			18	23		18	23	mA
NOTES:								
1. All voltages are with respect to GND. Currents are positive into, negative out of the specified terminal.			4. Amplifier gain defined as:			$G = \frac{\Delta V_{COMP}}{\Delta V_{+C/S}}; \Delta V_{+C/S} = 0$ to $1.0\text{V}$		
2. This parameter, although guaranteed over the recommended operating conditions is not 100% tested in production.			5. Current into CL SS guaranteed to latch circuit into shutdown state					
3. Parameter measured at trip point of latch with $V_{E/A+} = V_{REF}$ , $V_{E/A-} = 0\text{V}$ .			6. Current into CL SS guaranteed not to latch circuit into shutdown state					

APPLICATIONS DATA

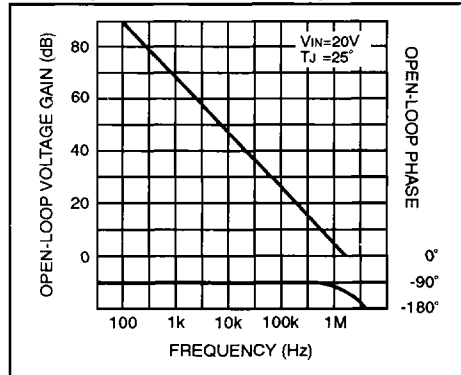
Oscillator Circuit



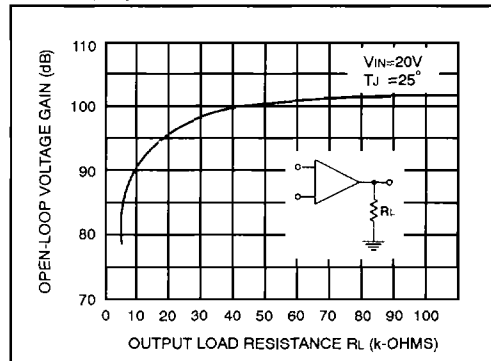
Error Amp Output Configuration



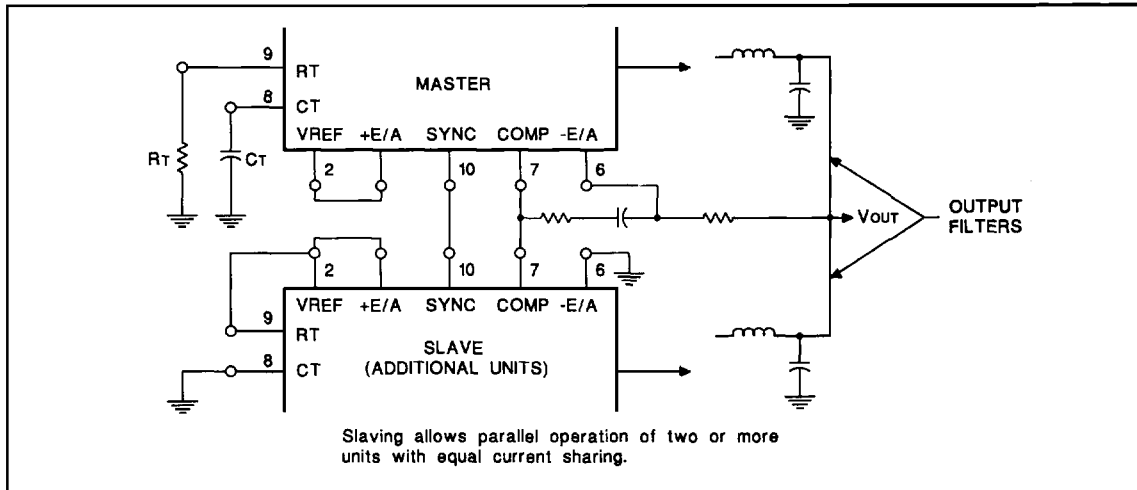
Error Amp Gain and Phase vs Frequency



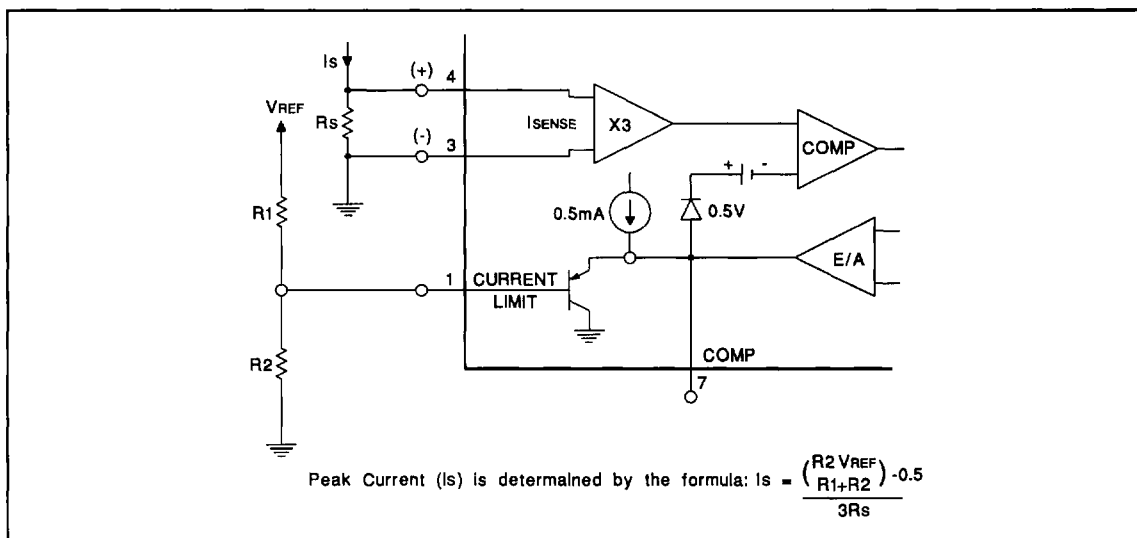
Error Amp Open-Loop D.C. Gain vs Load Resistance

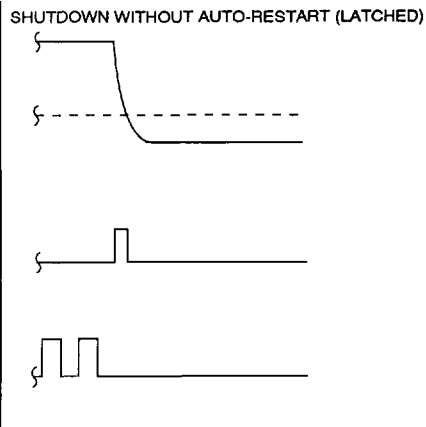
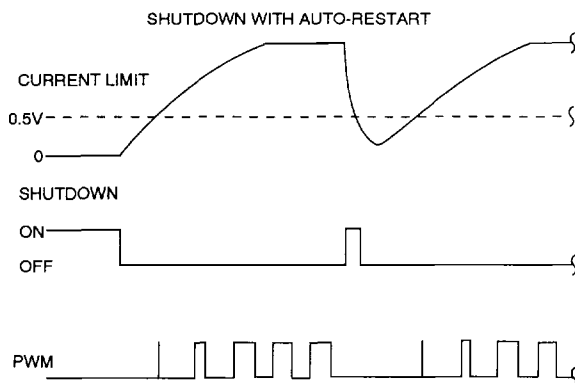
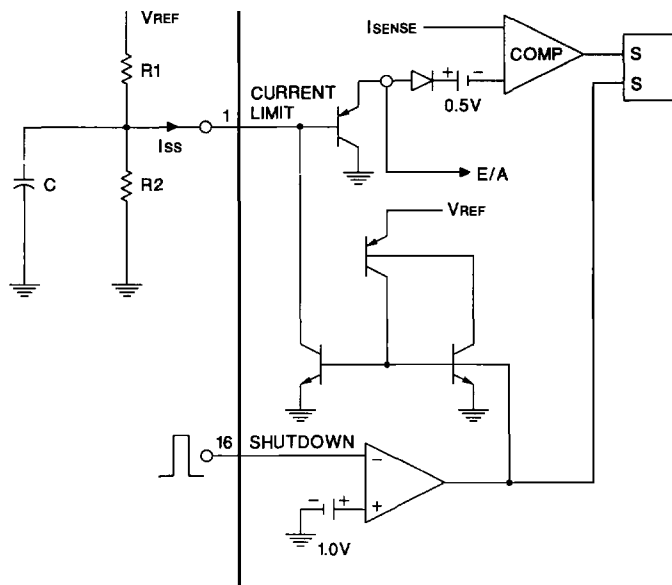


**Parallel Operation**



**Pulse by Pulse Current Limiting**

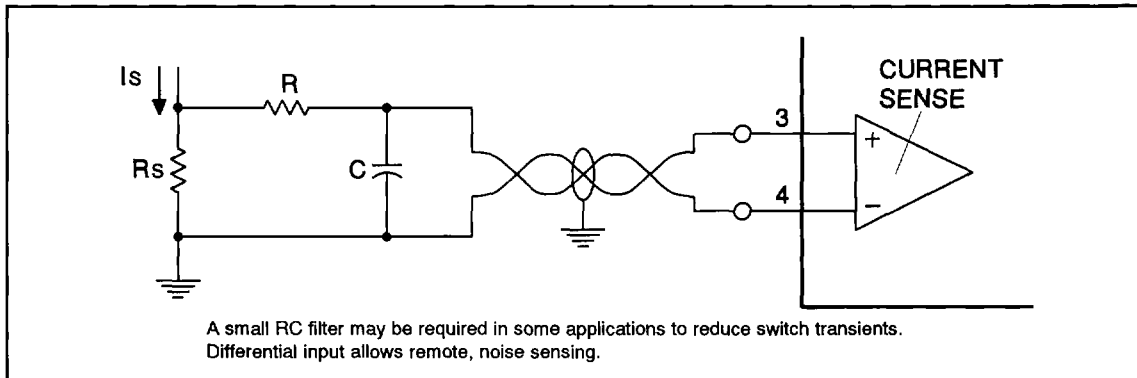




If  $\frac{V_{REF}}{R1} < 0.8\text{mA}$ , the shutdown latch will commutate when  $I_{SS} = 0.8\text{mA}$  and a restart cycle will be initiated.

If  $\frac{V_{REF}}{R1} > 3\text{mA}$ , the device will latch off until power is recycled.

**Current Sense Amp Connections**



**UC1856 Open Loop Test Circuit**

