PRELIMINARY

512Kx8 Static RAM CMOS, Module

The EDI8F8512C/LP/P is a 4096K bit CMOS Static RAM based on four 128Kx8 Static RAMs mounted on a multi-layered epoxy laminate (FR4) substrate.

Functional equivalence to the monolithic four megabit Static RAM is achieved by utilization of an on-board decoder that interprets the higher order address (A17 & A18) to select one of the128Kx8 Static RAMs.

The 32 pin DIP pinout adheres to the JEDEC standard for the four megabit device, to ensure compatibility with future monolithics.

The device is available with Low Power (P) and Low Power with Data Retention (LP).

All inputs and outputs are TTL compatible and operate from a single 5V supply. Fully asynchronous, the EDI8F8512C/LP/P requires no clocks or refreshing for operation.

Features

512Kx8 bit CMOS Static Random Access Memory

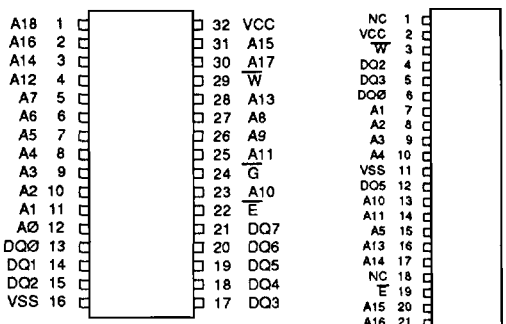
- Access Times 85 thru 150ns
- Data Retention Function (LP version)
- TTL Compatible Inputs and Outputs
- Fully Static, No Clocks

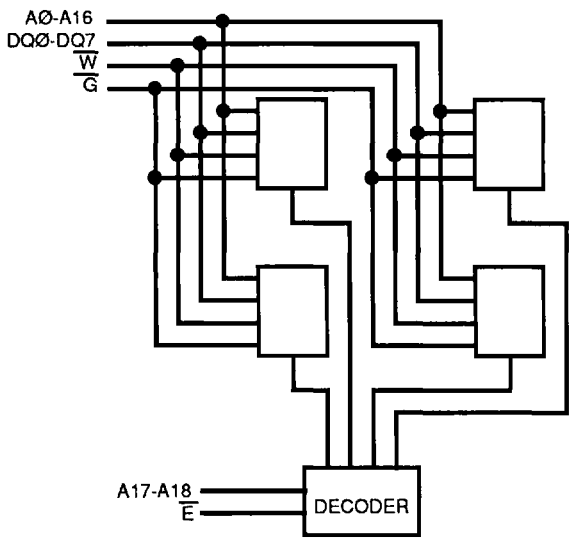
High Density Packaging

- 36 Pin SIP, No. 63
- 32 Pin DIP, JEDEC Approved Pinout, No. 91

Single +5V (±10%) Supply Operation

Pin Configurations and Block Diagram





Pin Names

AØ-A18	Address Inputs
E	Chip Enable
W	Write Enable
G	Output Enable
DQØ-DQ7	Common Data Input/Output
VCC	Power (+5V±10%)
VSS	Ground
NC	No Connection

Absolute Maximum Ratings*

Voltage on any pin relative to VSS ..... -0.5V to 7.0V
Operating Temperature TA (Ambient)
Commercial ..... 0°C to +70°C
Industrial ..... -40°C to +85°C
Storage Temperature
Plastic ..... -55°C to +125°C
Ceramic ..... -65°C to +150°C
Power Dissipation ..... 1 Watt
Output Current. ..... 20 mA

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	VCC	4.5	5.0	5.5	V
Supply Voltage	VSS	0	0	0	V
Input High Voltage	VIH	2.2	--	6.0	V
Input Low Voltage	VIL	-0.3	--	0.8	V

AC Test Conditions

Input Pulse Levels ..... VSS to 3.0V
Input Rise and Fall Times 5ns
Input and Output Timing Levels 1.5V
Output Load 45-70ns ..... 1TTL = 30pF
85-150ns ..... 1TTL, CL =100pF
(note: For TEHQZ,TGHQZ and TWLQZ, CL = 5pF)

DC Electrical Characteristics

Parameter	Sym	Conditions		Min	Typ*	Max	Units
Operating Power Supply Current	ICC1	$\overline{W}$, $\overline{E}$ = VIL, II/O = 0mA, Min Cycle		--	70	110	mA
Standby (TTL) Power Supply Current	ICC2	$\overline{E}$ ≥ VIH, VIN ≤ VIL VIN ≥ VIH		--	10	35	mA
Full Standby Power Supply Current	ICC3	$\overline{E}$ ≥ VCC-0.2V VIN ≥ VCC-0.2V or VIN ≤ 0.2V	C	--	2	5	mA
			LP/P	--	40	400	µA
Input Leakage Current	ILI	VIN = 0V to VCC		--	--	±10	µA
Output Leakage Current	ILO	V I/O = 0V to VCC		--	--	±10	µA
Output High Voltage	VOH	IOH =-1.0mA		2.4	--	--	V
Output Low Voltage	VOL	IOL = 2.1mA		--	--	0.4	V

*Typical: TA = 25°C, VCC = 5.0V

Truth Table

$\overline{G}$	$\overline{E}$	$\overline{W}$	Mode	Output	Power
X	H	X	Standby	High Z	ICC2, ICC3
H	L	H	Output Deselect	High Z	ICC1
L	L	H	Read	DOUT	ICC1
X	L	L	Write	DIN	ICC1

Capacitance

(f=1.0MHz, VIN=VCC or VSS)

Parameter	Sym	Max	Unit
Input Capacitance (Except DQ Pins)	CI	26	pF
Capacitance (DQ Pins)	CD/Q	43	pF
Input ($\overline{E}$)	CC	10	pF
Input ($\overline{W}$) Line	CW	32	pF

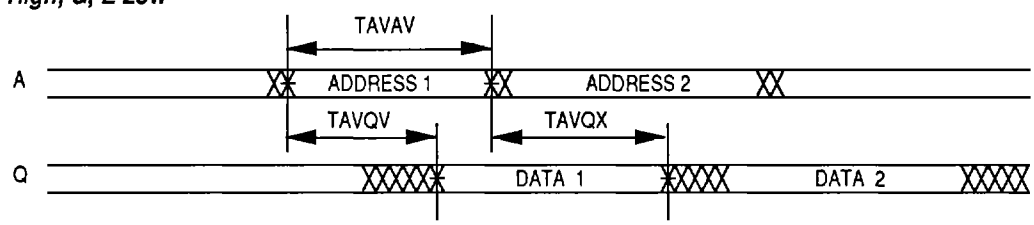
These parameters are sampled, not 100% tested.

AC Characteristics
Read Cycle

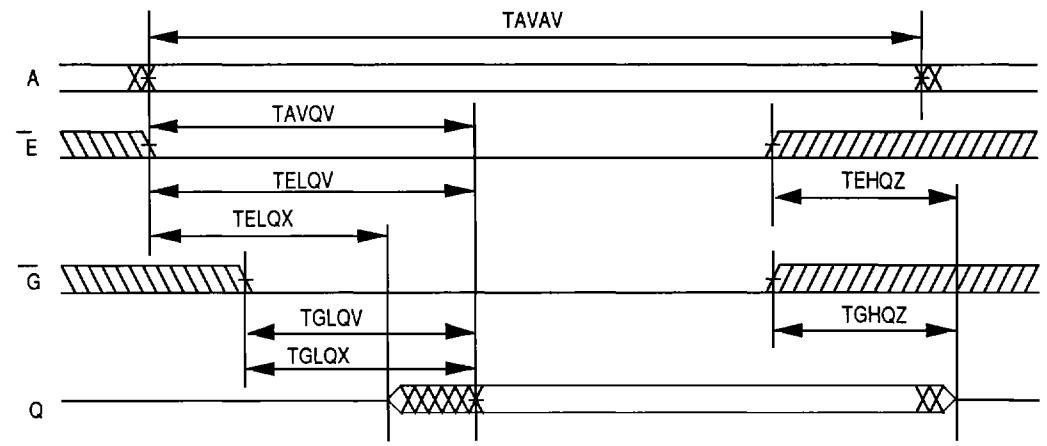
Parameter	Symbol	85ns		100ns		120ns		150ns		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	TAVAV	85		100		120		150		ns
Address Access Time	TAVQV		85		100		120		150	ns
Chip Enable Access Time	TELQV		85		100		120		150	ns
Chip Enable to Output in Low Z (1)	TELQX	5		5		5		5		ns
Output Enable to Output Valid	TGLQV		45		50		60		70	ns
Output Enable to Output in Low Z (1)	TGLQX	0		0		0		0		ns
Chip Disable to Output in High Z (1)	TEHQZ		35		40		45		50	ns
Output Disable to Output in High Z(1)	TGHQZ		35		40		45		50	ns
Output Hold from Address Change	TAVQX	3		3		3		3		ns

Note 1: Parameter guaranteed, but not tested.

Read Cycle 1
$\overline{W}$ High; $\overline{G}$, $\overline{E}$ Low



Read Cycle 2
$\overline{W}$ High

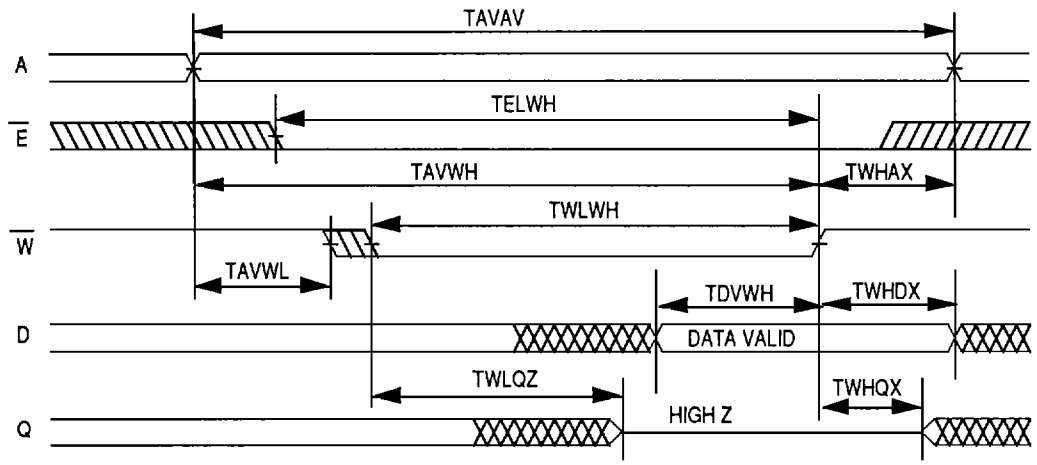


AC Characteristics
Write Cycle

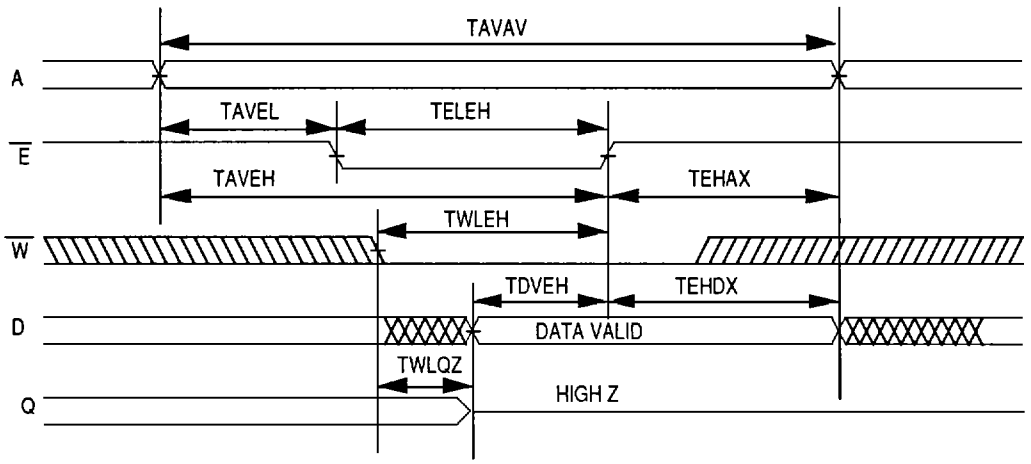
Parameter	Symbol		85ns		100ns		120ns		150ns		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	TAVAV		85		100		120		150		ns
Chip Enable to	TELWH	$\overline{W}$	70		80		100		110		ns
End of Write	TELEH	$\overline{E}$	70		80		100		110		ns
Address Setup Time	TAVWL	$\overline{W}$	0		0		0		0		ns
	TAVEL	$\overline{E}$	0		0		0		0		ns
Address Valid to	TAVWH	$\overline{W}$	70		80		100		110		ns
End of Write	TAVEH	$\overline{E}$	70		80		100		110		ns
Write Pulse Width	TWLWH	$\overline{W}$	70		80		100		110		ns
	TWLEH	$\overline{E}$	70		80		100		110		ns
Write Recovery Time	TWHAX	$\overline{W}$	0		0		0		0		ns
	TEHAX	$\overline{E}$	0		0		0		0		ns
Data Hold Time	TWHDX	$\overline{W}$	0		0		0		0		ns
	TEHDX	$\overline{E}$	0		0		0		0		ns
Write to Output in High Z (1)	TWLQZ		0	35	0	40	0	45	0	50	ns
Data to Write Time	TDVWH	$\overline{W}$	35		40		45		50		ns
	TDVEH	$\overline{E}$	35		40		45		50		ns
Output Active from End of Write (1)	TWHQX		5		5		5		5		ns

Note 1: Parameter guaranteed, but not tested.

Write Cycle 1
$\overline{W}$ Controlled



Write Cycle 2
$\overline{E}$ Controlled



Data Retention Characteristics

LP Version Only

Characteristic	Sym	Test Conditions	VDD	Min	Typ	Max		Unit
						70°C	85°C	
Data Retention Voltage	VDD	VDD = 0.2V		2	--	--	--	V
Data Retention Quiescent Current	ICCDR	$\overline{E}$ ≥ VDD -0.2V	2V	--	10	125	185	µA
		VIN ≥ VDD -0.2V	3V	--	20	200	250	µA
Chip Disable to Data Retention Time	TCDR	or VIN ≤ 0.2V		0	--	--	--	ns
Operation Recovery Time	TR			5	--	--	--	ms

Data Retention
$\overline{E}$ Controlled