# TC74HC4051AP/AF•TC74HC4052AP/AF TC74HC4053AP/AF/AFN

**TC74HC4051 8-Channel Analog Multiplexer/ Demultiplexer**

**TC74HC4052 Dual 4-Channel Analog Multiplexer/ Demultiplexer**

**TC74HC4053 Triple 2-Channel Analog Multiplexer/ Demultiplexer**

The TC74HC4051A/4052A/4053A are high speed CMOS MULTIPLEXER/DEMULTIPLEXER fabricated with silicon gate $C^2MOS$ technology. They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The TC74HC4051A has an 8 channel configuration, the TC74HC4052A has a 4 channel x 2 configuration and the TC74HC4053A has a 2 channel x 3 configuration.

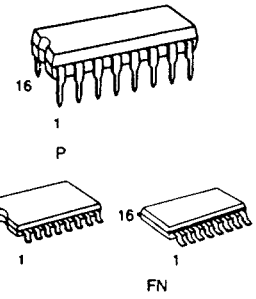
The digital signal to the control terminal turns "ON" the corresponding switch of each channel a large amplitude signal ($V_{CC}$ - $V_{EE}$) can then be switched by the small logical amplitude ($V_{CC}$ - GND) control signal.

For example, in the case of $V_{CC}$ = 5V, GND = 0V, $V_{EE}$ = -5V, signals between -5V and +5V can be switched from the logical circuit with a single power supply of 5V. As the ON-resistance of each switch is low, they can be connected to circuits with low input impedance.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

## Features

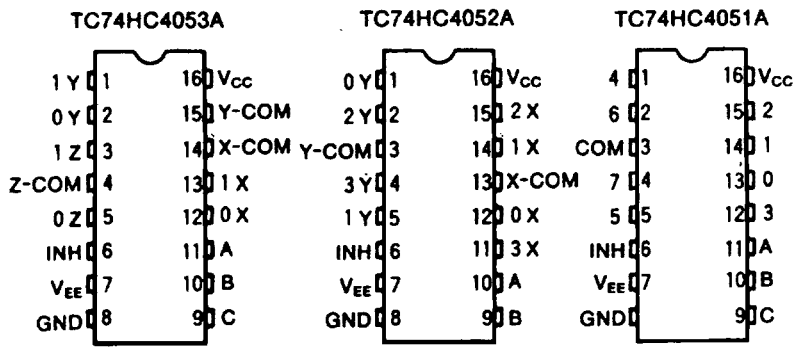
- High Speed: $t_{pd}$ = 15ns(Typ.) at $V_{CC}$ = 5V
- Low Power Dissipation: $I_{CC}$ = 4μA(Max.) at Ta = 25°C
- High Noise Immunity: $V_{NIH}$ = $V_{NIL}$ = 28% $V_{CC}$(Min.)
- Low ON Resistance: $R_{ON}$ = 50Ω(Typ.) at $V_{CC}$-$V_{EE}$ = 9V
- High Degree of Linearity: THD = 0.02%(Typ.) at $V_{CC}$-$V_{EE}$ = 9V
- Pin and Function Compatible with 4051/4052/4053B



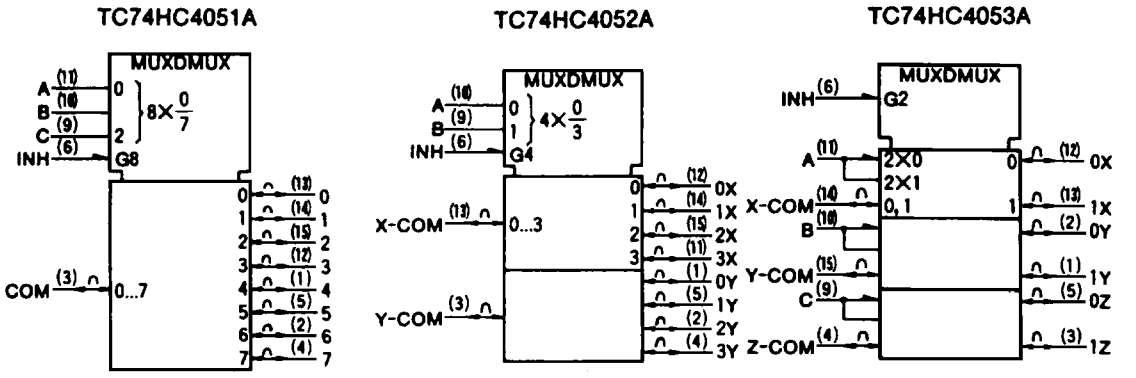

**Truth Table**

| Control Inputs | | | | "ON" Channel | | |
|---|---|---|---|---|---|---|
| Inhibit | C* | B | A | HC4051A | HC4052A | HC4053A |
| L | L | L | L | 0 | 0X, 0Y | 0X, 0Y, 0Z |
| L | L | L | H | 1 | 1X, 1Y | 1X, 0Y, 0Z |
| L | L | H | L | 2 | 2X, 2Y | 0X, 1Y, 0Z |
| L | L | H | H | 3 | 3X, 3Y | 1X, 1Y, 0Z |
| L | H | L | L | 4 | - - | 0X, 0Y, 1Z |
| L | H | L | H | 5 | - - | 1X, 0Y, 1Z |
| L | H | H | L | 6 | - - | 0X, 1Y, 1Z |
| L | H | H | H | 7 | - - | 1X, 1Y, 1Z |
| H | X | X | X | None | None | None |

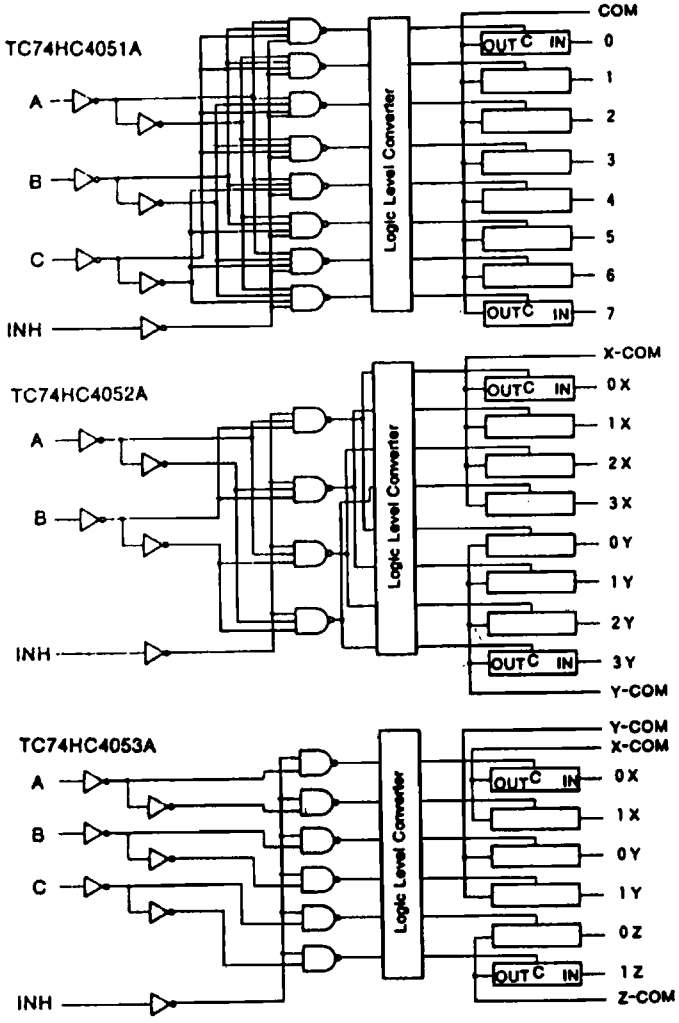
**X: Don't care, *: Except HC4052A**




**Pin Assignment**




IEC Logic Symbol




Logic Diagram

## Absolute Maximum Ratings

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Supply Voltage Range | $V_{CC}$ | -0.5 ~ 7 | V |
| Supply Voltage Range | $V_{CC}$-$V_{EE}$ | -0.5 ~ 13 | V |
| Control Input Voltage | $V_{IN}$ | -0.5 ~ $V_{CC}$ + 0.5 | V |
| Switch I/O Voltage | $V_{I/O}$ | $V_{EE}$ - 0.5 ~ $V_{CC}$ + 0.5 | V |
| Control Input Diode Current | $I_{CK}$ | ±20 | mA |
| I/O Diode Current | $I_{IOK}$ | ±20 | mA |
| Switch through Current | $I_T$ | ±25 | mA |
| DC $V_{CC}$/GND Current | $I_{CC}$ | ±50 | mA |
| Power Dissipation | $P_D$ | 500(DIP)*/180(MFP) | mW |
| Storage Temperature | $T_{stg}$ | -65 ~ 150 | °C |
| Lead Temperature 10sec | $T_L$ | 300 | °C |

*500mW in the range of Ta = -40°C ~ 65°C. From Ta = 65°C to 85°C a derating factor of -10mW/°C shall be applied until 300mW.

## Recommended Operating Conditions

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 2 ~ 6 | V |
| Supply Voltage | $V_{EE}$ | -6 ~ 0 | V |
| Supply Voltage | $V_{CC}$-$V_{EE}$ | 2 ~ 12 | V |
| Control Input Voltage | $V_{IN}$ | 0 ~ $V_{CC}$ | V |
| Switch I/O Voltage | $V_{I/O}$ | $V_{EE}$ ~ $V_{CC}$ | V |
| Operating Temperature | $T_{opr}$ | -40 ~ 85 | °C |
| Input Rise and Fall Time | $t_r$, $t_f$ | 0 ~ 1000($V_{CC}$ = 2.0V)<br>0 ~ 500($V_{CC}$ = 4.5V)<br>0 ~ 400($V_{CC}$ = 6.0V) | ns |

## DC Electrical Characteristics

| Parameter | Symbol | Test Condition | $V_{EE}$ | $V_{CC}$ | Ta = 25°C Min | Typ. | Max. | Ta = -40 ~ 85°C Min. | Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| High-Level Input Voltage | $V_{IHC}$ | – | | 2.0 | 1.5 | – | – | 1.5 | – | V |
| | | | | 4.5 | 3.15 | – | – | 3.15 | – | |
| | | | | 6.0 | 4.2 | – | – | 4.2 | – | |
| Low-Level Input Voltage | $V_{ILC}$ | – | | 2.0 | – | – | 0.5 | – | 0.5 | |
| | | | | 4.5 | – | – | 1.35 | – | 1.35 | |
| | | | | 6.0 | – | – | 1.8 | – | 1.8 | |
| ON Resistance | $R_{ON}$ | $V_{IN} = V_{ILC}$ or $V_{IHC}$<br>$V_{I/O} = V_{CC}$ to $V_{EE}$<br>$V_{I/O} \leq 2mA$ | GND | 4.5 | – | 85 | 180 | – | 225 | Ω |
| | | | - 4.5 | 4.5 | – | 55 | 120 | – | 150 | |
| | | | - 6.0 | 6.0 | – | 50 | 100 | – | 125 | |
| | | $V_{IN} = V_{ILC}$ or $V_{IHC}$<br>$V_{I/O} = V_{CC}$ to $V_{EE}$<br>$V_{I/O} \leq 2mA$ | GND | 2.0 | – | 150 | – | – | – | |
| | | | GND | 4.5 | – | 70 | 150 | – | 190 | |
| | | | - 4.5 | 4.5 | – | 50 | 100 | – | 125 | |
| | | | - 6.0 | 6.0 | – | 45 | 80 | – | 100 | |
| Difference of ON Resistance Between Switches | $\Delta R_{ON}$ | $V_{IN} = V_{ILC}$ or $V_{IHC}$<br>$V_{I/O} = V_{CC}$ to $V_{EE}$<br>$V_{I/O} \leq 2mA$ | GND | 4.5 | – | 10 | 30 | – | 35 | |
| | | | - 4.5 | 4.5 | – | 5 | 12 | – | 15 | |
| | | | - 6.0 | 6.0 | – | 5 | 10 | – | 12 | |
| Input/Output Leakage Current (Switch OFF) | $I_{OFF}$ | $V_{OS} = V_{CC}$ or GND<br>$V_{IS}$ = GND or $V_{CC}$<br>$V_{IN} = V_{ILC}$ or $V_{IHC}$ | GND | 6.0 | – | – | ±60 | – | ±600 | nA |
| | | | - 6.0 | 6.0 | – | – | ±100 | – | ±1000 | |
| Switch Input Leakage Current (Switch ON) | $I_{IZ}$ | $V_{OS} = V_{CC}$ or GND<br>$V_{INH} = V_{ILC}$ or $V_{IHC}$ | GND | 6.0 | – | – | ±60 | – | ±600 | |
| | | | - 6.0 | 6.0 | | | ±100 | | ±1000 | |
| Control Input Current | $I_{IN}$ | $V_{IN} = V_{CC}$ or GND | GND | 6.0 | – | – | ±0.1 | – | ±1.0 | μA |
| Quiescent Supply Current | $I_{CC}$ | $V_{IN} = V_{CC}$ or GND | GND | 6.0 | – | – | 4.0 | – | 40.0 | |
| | | | - 6.0 | 6.0 | – | – | 8.0 | – | 80.0 | |

## AC Electrical Characteristics ($C_L$ = 50pF, Input $t_r = t_f$ = 6ns, GND = 0V)

| Parameter | Symbol | Test Condition | | | Ta = 25°C | | | Ta = -40 ~ 85°C | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{EE}$ | $V_{CC}$ | Min. | Typ. | Max. | Min. | Max. | |
| Phase difference between Input and Output | φI/O | – | GND | 2.0 | – | 25 | 60 | – | 75 | ns |
| | | | GND | 4.5 | – | 6 | 12 | – | 15 | |
| | | | GND | 6.0 | – | 5 | 10 | – | 13 | |
| | | | -4.5 | 4.5 | – | 4 | – | – | – | |
| Output Enable Time | $t_{pZL}$ $t_{pZH}$ | *1 4051 | GND | 2.0 | – | 64 | 225 | – | 280 | |
| | | | GND | 4.5 | – | 18 | 45 | – | 56 | |
| | | | GND | 6.0 | – | 15 | 38 | – | 48 | |
| | | | -4.5 | 4.5 | – | 18 | – | – | – | |
| | | *1 4052 | GND | 2.0 | – | 64 | 225 | – | 280 | |
| | | | GND | 4.5 | – | 18 | 45 | – | 56 | |
| | | | GND | 6.0 | – | 15 | 38 | – | 48 | |
| | | | -4.5 | 4.5 | – | 18 | – | – | – | |
| | | *1 4053 | GND | 2.0 | – | 50 | 225 | – | 280 | |
| | | | GND | 4.5 | – | 14 | 45 | – | 56 | |
| | | | GND | 6.0 | – | 12 | 38 | – | 48 | |
| | | | -4,5 | 4.5 | – | 14 | – | – | – | |
| Output Disable Time | $t_{pLZ}$ $t_{pHZ}$ | *1 4051 | GND | 2.0 | – | 100 | 250 | – | 315 | |
| | | | GND | 4.5 | – | 33 | 50 | – | 63 | |
| | | | GND | 6.0 | – | 28 | 43 | – | 54 | |
| | | | -4.5 | 4.5 | – | 29 | – | – | – | |
| | | *1 4052 | GND | 2.0 | – | 100 | 250 | – | 315 | |
| | | | GND | 4.5 | – | 33 | 50 | – | 63 | |
| | | | GND | 6.0 | – | 28 | 43 | – | 54 | |
| | | | -4.5 | 4.5 | – | 29 | – | – | – | |
| | | *1 4053 | GND | 2.0 | – | 95 | 225 | – | 280 | |
| | | | GND | 4.5 | – | 30 | 45 | – | 56 | |
| | | | GND | 6.0 | – | 26 | 38 | – | 48 | |
| | | | -4.5 | 4.5 | – | 26 | – | – | – | |
| Control Input Capacitance | $C_{IN}$ | All Types | – | – | – | 5 | 10 | – | 10 | pF |
| COMMON Terminal Capacitance | $C_{IS}$ | 4051 | -5.0 | 5.0 | – | 36 | 70 | – | 70 | |
| | | 4052 | | | – | 19 | 40 | – | 40 | |
| | | 4053 | | | – | 11 | 20 | – | 20 | |
| Switch Terminal Capacitance | $C_{I/O}$ | 4051 | -5.0 | 5.0 | – | 7 | 15 | – | 15 | |
| | | 4052 | | | – | 7 | 15 | – | 15 | |
| | | 4053 | | | – | 7 | 15 | – | 15 | |
| Feedthrough Capacitance | $C_{IOS}$ | 4051 | -5.0 | 5.0 | – | 0.95 | 2 | – | 2 | |
| | | 4052 | | | – | 0.85 | 2 | – | 2 | |
| | | 4053 | | | – | 0.75 | 2 | – | 2 | |
| Power Dissipation Capacitance | $C_{PD}$ | *2 4051 | GND | 5.0 | – | 70 | – | – | – | |
| | | 4052 | | | – | 71 | – | – | – | |
| | | 4053 | | | – | 67 | – | – | – | |

Note (1) $R_L$ = kΩ

(2) $C_{PD}$ is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation:

$I_{CC(opr)} = C_{PD} \bullet V_{CC} \bullet f_{IN} + I_{CC}$

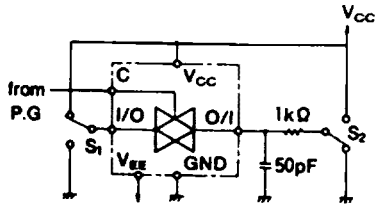
## Analog Switch Characteristics (GND = 0V, Ta = 25°C)

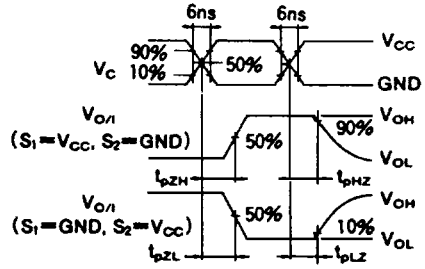
| Parameter | Symbol | Test Condition | | $V_{EE}$ | $V_{CC}$ | Typ. | Unit |
|---|---|---|---|---|---|---|---|
| Sine Wave Distortion (T.H.D) | | $R_L$ = 10kΩ, $C_L$ = 50pF, $f_{IN}$ = 1kHz | $V_{IN}$ = 4.0$V_{P-P}$ | -2.25 | 2.25 | 0.025 | % |
| | | | $V_{IN}$ = 8.0$V_{P-P}$ | -4.5 | 4.5 | 0.020 | |
| | | | $V_{CC}$ = 11.0$V_{P-P}$ | -6.0 | 6.0 | 0.018 | |
| Frequency Response (Switch ON) | $f_{MAX}$ | Adjust $f_{IN}$ Voltage to obtain 0dBm at $V_{OS}$; Increase $f_{IN}$ Frequency until dB Meter reads -3dB; $R_L$ = 50Ω, $C_L$ = 10pF, $f_{IN}$ = 1MHz, Sine Wave | *1 ALL | -2.25 | 2.25 | 120 | MHz |
| | | | *2 4051 | | | 45 | |
| | | | 4052 | | | 70 | |
| | | | 4053 | | | 95 | |
| | | | *1 ALL | -4.5 | 4.5 | 190 | |
| | | | *2 4051 | | | 70 | |
| | | | 4052 | | | 110 | |
| | | | 4053 | | | 150 | |
| | | | *1 ALL | -6.0 | 6.0 | 200 | |
| | | | *2 4051 | | | 85 | |
| | | | 4052 | | | 140 | |
| | | | 4053 | | | 190 | |
| Feedthrough Attenuation (Switch OFF) | | $V_{in}$ is centered at ($V_{CC}$ - $V_{EE}$); Adjust input for 0dBm; $R_L$ = 600Ω, $C_L$ = 50pF, $f_{IN}$ = 1MHz, Sine Wave | | -2.25 | 2.25 | -50 | dB |
| | | | | -4.5 | 4.5 | -50 | |
| | | | | -6.0 | 6.0 | -50 | |
| Crosstalk (Control Input to Signal Output) | | $R_L$ = 600Ω, $C_L$ = 50pF, $f_{IN}$ = 1MHz, Square Wave ($t_r$ = $t_f$ = 6ns) | | -2.25 | 2.25 | 60 | mV |
| | | | | -4.5 | 4.5 | 140 | |
| | | | | -6.0 | 6.0 | 200 | |
| Crosstalk (Between any switches) | | Adjust $V_{IN}$ to obtain 0dBm at Input; $R_L$ = 600Ω, $C_L$ = 50pF, $f_{IN}$ = 1MHz, Sine Wave | | -2.25 | 2.25 | -50 | dB |
| | | | | -4.5 | 4.5 | -50 | |
| | | | | -6.0 | 6.0 | -50 | |

* 1: Input COMMON Terminal, and measured at SWITCH Terminal.
* 2: Input SWITCH Terminal, and measured at COMMON Terminal.

Note: These characteristics are determined by design of devices.

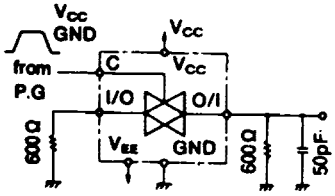
1. $t_{PLZ}$, $t_{PHZ}$, $t_{PZL}$, $t_{PZH}$



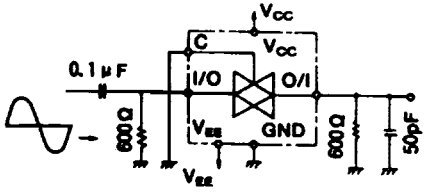




2. CROSS TALK (CONTROL INPUT-SWITCH OUTPUT)

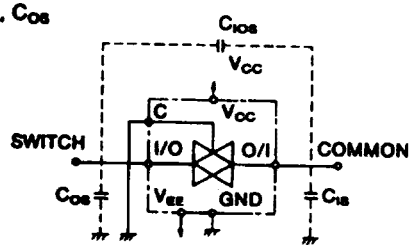
fin=1MHz duty=50% tr=tf=6ns



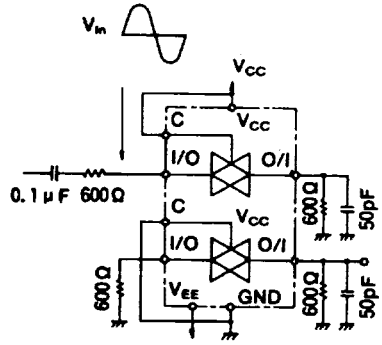

3. FEEDTHROUGH ATTENUATION



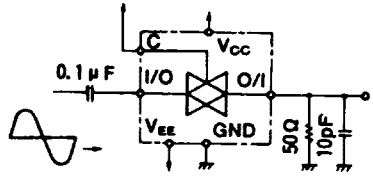

4. $C_{IOS}$, $C_{IS}$, $C_{OS}$




5. CROSSTALK (BETWEEN ANY TWO SWITCHE




6. FREQUENCY RESPONSE (SWITCH ON)




Switching Characteristics Test Circuits

Notes