

Transceiver

54F657

FEATURES

- High-impedance NPN base input for reduced loading (20 in High and Low states)
- Ideal in applications where high output drive and light bus loading are required (I_{HL} is 20 μ A vs FAST std of 600 μ A)
- 24-pin slim dip (300-mil) package
- 3-State outputs

- Outputs sink 48mA
- 12mA source current
- Input diodes for termination effects

DESCRIPTION

The 54F657 contains eight non-inverting buffers with 3-State outputs and an 8-bit parity generator/checker, and is intended for

bus-oriented applications. The buffers have a guaranteed current sinking capability of 20mA at the A ports and 48mA at the B ports. The Transmit/Receive (T/R) input determines the direction of the data flow through the bidirectional transceivers. Transmit (active High) enables data from A ports to B ports; Receive (active Low) enables data from B ports to A ports.

ORDERING INFORMATION

DESCRIPTION	ORDER CODE	PACKAGE DESIGNATOR*
24-Pin Ceramic DIP	54F657/BLA	GDIP3-T24
24-Pin Ceramic FlatPack	54F657/BKA	GDFF2-F24
28-Pin Ceramic LLCC	54F657/B3A	CQCC2-N28

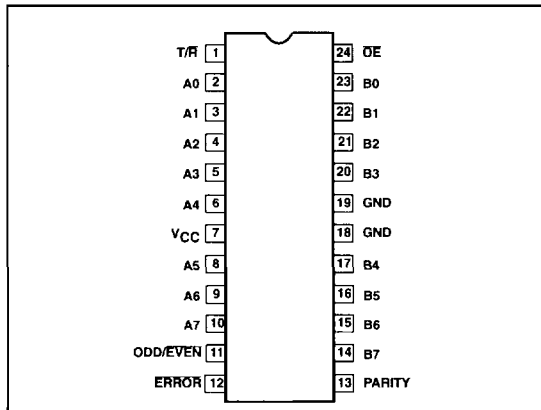
* MIL-STD 1835 or Appendix A of 1995 Military Data Handbook

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

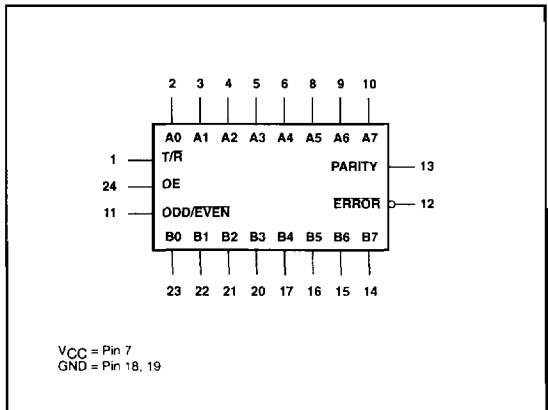
PINS	DESCRIPTION	54F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A0 - A7	A ports 3-State inputs	5.0/0.167	100 μ A/100 μ A
B0 - B7	B ports 3-State inputs	3.5/0.117	70 μ A/70 μ A
PARITY	Parity input	3.5/0.117	70 μ A/70 μ A
T/R	Transmit/receive input	2.0/0.066	40 μ A/40 μ A
ODD/EVEN	ODD/EVEN input	1.0/0.033	20 μ A/20 μ A
OE	Output enable input (active Low)	2.0/0.066	40 μ A/40 μ A
A0 - A7	A ports 3-State outputs	150/33.3	3mA/20mA
B0 - B7	B ports 3-State outputs	600/80	12mA/48mA
PARITY	Parity output	150/33.3	3mA/20mA
ERROR	Error output	150/33.3	3mA/20mA

NOTE: One (1.0) FAST Unit Load is defined as 20 μ A in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



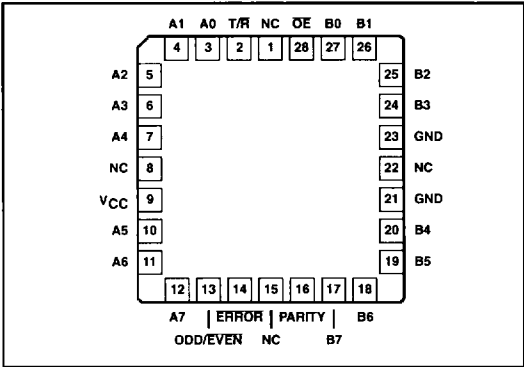
LOGIC SYMBOL



Transceiver

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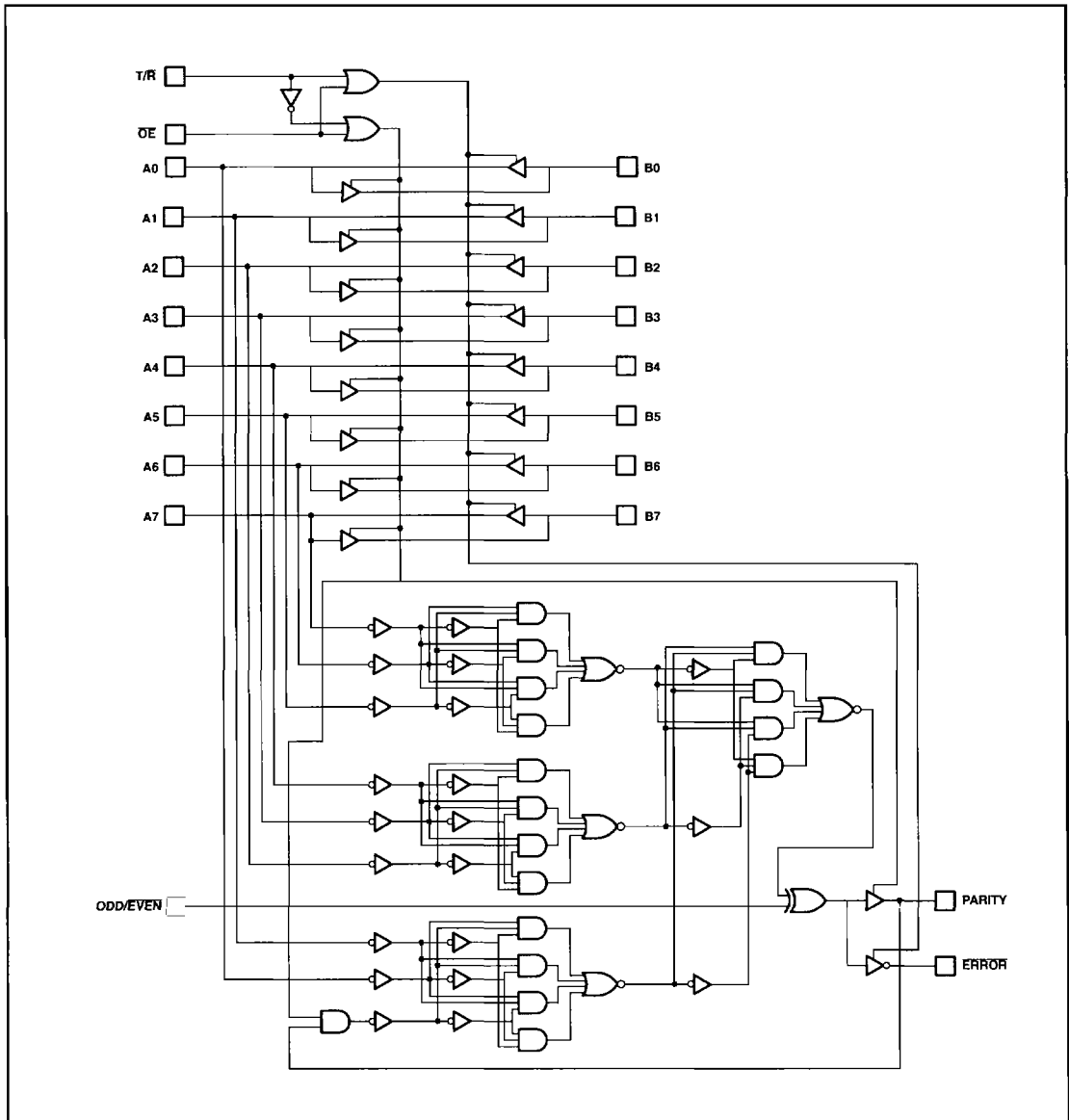
LLCC LEAD CONFIGURATION



Transceiver

54F657

LOGIC DIAGRAM



Transceiver

54F657

The Output Enable inputs disable both the A and B ports by placing them in a High-Z condition when either the OE input is High or the OE input is Low.

The parity generator detects whether an even or odd number of bits on the A ports are High, depending on the condition of the Parity Select input. If the Even input is active High and an even number of A inputs are High, the Parity output is High. The parity of the data received on the B ports is compared with the Parity Select input and the Error output is Low if not equal.

FUNCTION TABLE

NUMBER OF INPUTS THAT ARE HIGH	INPUTS			INPUT/OUTPUT	OUTPUTS	
	OE	T/R	ODD/EVEN	PARITY	ERROR	OUTPUTS MODE
0, 2, 4, 6, 8	L	H	H	H	(Z)	Transmit
	L	H	L	L	(Z)	Transmit
	L	L	H	H	H	Receive
	L	L	H	L	L	Receive
	L	L	L	H	L	Receive
	L	L	L	L	H	Receive
1, 3, 5, 7	L	H	H	L	(Z)	Transmit
	L	H	L	H	(Z)	Transmit
	L	L	H	H	L	Receive
	L	L	H	L	H	Receive
	L	L	L	H	H	Receive
	L	L	L	L	L	Receive
Don't care	H	X	X	(Z)	(Z)	(Z)

H = High voltage level
 L = Low voltage level
 X = Don't care
 (Z)= High impedance state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V _{CC}	Supply voltage range	-0.5 to +7.0	V
V _I	Input voltage range	-0.5 to +7.0	V
I _I	Input current range	-30 to +5	mA
V _O	Voltage applied to output in High output state range	-0.5 to V _{CC}	V
I _O	Current applied to output in Low output state	A0 - A7	40
		B0 - B7, PARITY, ERROR	96
T _{STG}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5.0	5.5	V
V _{IH}	High-level input voltage ⁴	2.0			V
V _{IL}	Low-level input voltage ⁴			0.8	V
I _{IK}	Input clamp current			-18	mA
I _{OH2}	High-level output current	A0 - A7 & B0 - B7		-3	mA
		B0 - B7, PARITY, ERROR		-12	mA
I _{OH1}	High-level output current	A0 - A7 & B0 - B7		-1	mA
I _{OL}	Low-level output current	A0 - A7		20	mA
		B0 - B7, PARITY, ERROR		48	mA
T _A	Operating free-air temperature range	-55		+125	°C

Transceiver

54F657

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS ¹		LIMITS			UNIT
					MIN	TYP ²	MAX	
V _{OH}	High-level output voltage	All outputs	V _{CC} = MIN,	I _{OH} = -3mA	2.4			V
		B0 - B7, PARITY ERROR	V _{IL} = MAX,	I _{OH} = -1mA	2.5	3.4		V
			V _{IH} = MIN	I _{OH} = -12mA	2.0			V
V _{OL}	Low-level output voltage	A0 - A7	V _{CC} = MIN,	I _{OL} = 20mA		.35	.50	V
		B0 - B7, PARITY ERROR	V _{IL} = MAX, V _{IH} = MIN	I _{OL} = 48mA		.40	.55	V
V _{IK}	Input clamp voltage		V _{CC} = MIN, I _I = I _{IK}			-0.73	-1.2	V
I _{IH2}	Input current at maximum input voltage	T/R, \overline{OE} , ODD/EVEN	V _{CC} = 0.0V, V _I = 7.0V				100	μ A
		A0 - A7	V _{CC} = 5.5V, V _I = 5.5V				2	mA
		B0 - B7	V _{CC} = 5.5V, V _I = 5.5V				1	mA
I _{IH1}	High-level input current	ODD/EVEN	V _{CC} = MAX, V _I = 2.7V				20	μ A
		T/R, \overline{OE}					40	μ A
I _{IL}	Low-level input current	ODD/EVEN	V _{CC} = MAX, V _I = 0.5V				-20	μ A
		T/R, \overline{OE}					-40	μ A
I _{IH} + I _{OZH}	Off-state current High level voltage applied	A0 - A7	V _{CC} = MAX, V _{IH} = MIN, V _O = 2.7V				100	μ A
I _{IL} + I _{OZL}	Off-state current Low level voltage applied		V _{CC} = MAX, V _{IH} = MIN, V _O = 0.5V				-100	μ A
I _{IH} + I _{OZH}	Off-state current High level voltage applied	B0 - B7	V _{CC} = MAX, V _{IH} = MIN, V _O = 2.7V				70	μ A
I _{IL} + I _{OZL}	Off-state current Low level voltage applied		V _{CC} = MAX, V _{IH} = MIN, V _O = 0.5V				-70	μ A
I _{OZH}	Off-state current High level voltage applied	ERROR	V _{CC} = MAX, V _{IH} = MIN, V _O = 2.7V				50	μ A
I _{OZL}	Off-state current Low level voltage applied		V _{CC} = MAX, V _{IH} = MIN, V _O = 0.5V				-50	μ A
I _{OS}	Short-circuit output current ³	A0 - A7	V _{CC} = MAX		-60		-150	mA
		B0 - B7			-100		-225	mA
I _{CC}	Supply current (total)	I _{CCH}	V _{CC} = MAX			90	125	mA
		I _{CCL}				106	150	mA
		I _{CCZ}				98	145	mA

Transceiver

54F657

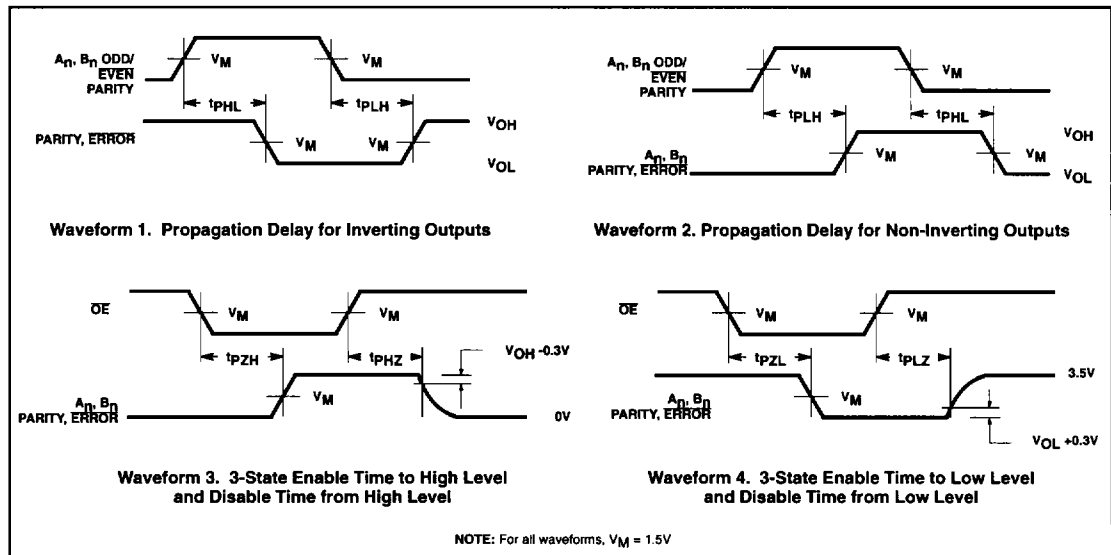
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T _{amb} = +25°C V _{CC} = +5.0V C _L = 50pF, R _L = 500Ω			T _{amb} = -55°C to +125°C V _{CC} = +5.0V ± 10% C _L = 50pF, R _L = 500Ω		
			MIN	TYP ²	MAX	MIN	MAX	
t _{PLH1} t _{PHL1}	Propagation delay A _n to B _n , B _n to A _n	Waveform 2	2.5 3.0	5.5 6.0	7.5 7.5	2.5 3.0	8.5 8.5	ns ns
t _{PLH2} t _{PHL2}	Propagation delay A _n to PARITY	Waveform 1, 2	7.0 7.0	10.0 10.0	14.0 14.0	6.5 6.5	18.0 18.5	ns ns
t _{PLH3} t _{PHL3}	Propagation delay ODD/EVEN to PARITY, ERROR	Waveform 1, 2	4.5 4.5	7.5 8.0	11.0 11.5	4.0 4.0	13.0 14.5	ns ns
t _{PLH4} t _{PHL4}	Propagation delay B _n to ERROR	Waveform 1, 2	8.0 8.0	14.0 14.0	20.5 20.5	7.0 7.0	24.0 25.5	ns ns
t _{PLH5} t _{PHL5}	Propagation delay PARITY to ERROR	Waveform 1, 2	8.0 8.0	11.5 12.0	15.5 15.5	7.0 7.5	18.0 19.5	ns ns
t _{PZH} t _{PZL}	Output enable time ⁵ to High or Low level	Waveform 3 Waveform 4	3.0 4.0	5.5 7.0	8.0 9.5	3.0 4.0	9.5 12.5	ns ns
t _{PHZ} t _{PLZ}	Output disable time from High or Low level	Waveform 3 Waveform 4	2.0 2.0	4.5 4.0	7.5 6.0	2.0 2.0	8.5 8.0	ns ns

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type and function table operating mode.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
- When testing devices to the functional table specified refer to the "Recommended Operating Conditions" section of the Applications Note 202, "Testing and Specifying FAST Logic".
- These delay times reflect the 3-state recovery time only and not the signal through the buffers or the parity check circuitry. To assure VALID information at the ERROR pin, time must be allowed for the signal to propagate through the drivers (B to A), through the parity check circuitry (same as A to PARITY), and to the ERROR. VALID data at the ERROR pin ≥ (B to A) + (A to PARITY).

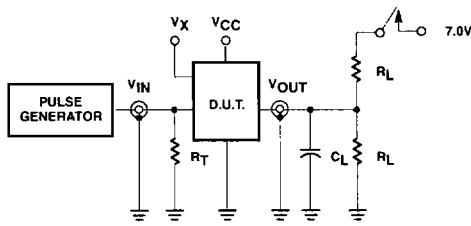
AC WAVEFORMS



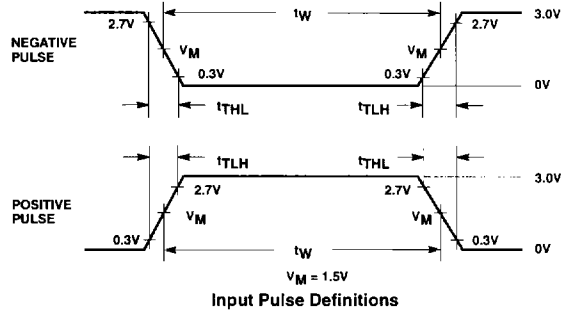
Transceiver

54F657

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs and Open Collector Outputs



SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{pZL}	closed
All other	open

INPUT PULSE CHARACTERISTICS				
Family	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54F	1MHz	500ns	$\leq 2.5ns$	$\leq 2.5ns$

DEFINITIONS:

- R_L = Load Resistor; see AC Characteristics for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
- R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
- V_X = Unlocked pins must be held at: $\leq 0.8V$, $\geq 2.7V$ or open per FunctionTable.