ADVANCED ANALOG

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DACHK

HIGH SPEED 12-BIT D/A CONVERTER

DESCRIPTION

The DACHK is a complete, high performance 12-bit D/A converter with fast settling time. The controlled input storage register is ideal for data bus interface applications.

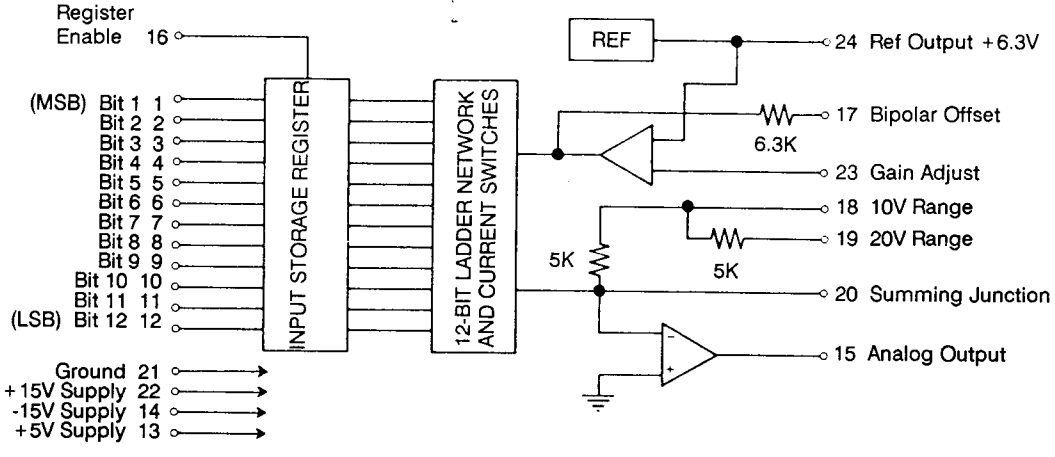
Coding options include binary or two's complement. The five output voltage ranges are user selectable and. the output settling time is 4 μsec. for a 20V step to .01%.

The DACHK requires ±15V and +5V supplies and power consumption is a low 380 mW (typ.) It is packaged in a 24-pin DIP and military screening is available.

FEATURES

- **Complete: Internal register**
  Internal reference
  Internal amplifier
- **± 1/2 LSB max. linearity error**
- **Monotonic over temperature**
- **Fast settling time - 4 μsec.**
- **40 ns data setup time**
- **Five output ranges**
- **Small side-brazed package**
- **Low power - 380 mW typ.**
- **Military screening available**

BLOCK DIAGRAM



SPECIFICATIONS

Supply voltages ±15VDC and +5VDC unless otherwise specified.

Characteristics	DACHK Conditions	DACHK Min	DACHK Typ	DACHK Max	DACHK-2 Min	DACHK-2 Typ	DACHK-2 Max	Units
RESOLUTION								
ANALOG OUTPUT		12			*			Bits
Output Voltage Ranges								
Unipolar		0 to +5, 0 to +10				*		V
Bipolar		±2.5, ±5, ±10				*		V
Output Impedance				.05			*	Ω
Output Current		±5			*			mA
DIGITAL INPUTS								
Register Enable								
Negative Pulse Width		60			*			nsec
Set-up Time - Digital Data to Register Enable		40			*			nsec
Logic Loading (all digital inputs)				1			*	HCT Load[1]
Logic Levels (all digital inputs)								
Logic "1"		2			*			V
Logic "0"				0.8			*	V
Parallel Data Coding[2]								
Unipolar Ranges			BIN			2's CBIN		
Bipolar Ranges			OBIN			2's COBIN		
TRANSFER CHARACTERISTICS								
Zero Error, Bipolar[3]	TA = +25°C		±.05	±.1		*	*	%FSR[4]
	Drift			±10			*	ppm/°C
Gain Error[3]	+25°C			±.1			*	%
	Drift[5]			±20			*	ppm/°C
Zero Error, Unipolar[3]	+25°C			.1			*	%FSR
	Drift			±5			*	ppm/°C
Linearity Error	+25°C			±1/2			*	LSB[6]
	T_A min to T_A max			±1/2			*	LSB
	Drift			±2			*	ppm/°C
Monotonicity		Guaranteed over temperature				*		
DYNAMIC CHARACTERISTICS								
Settling Time to .01%								
20V Step			4	5		*	*	μsec
10V Step			3	4		*	*	μsec
1 LSB Step			0.8	1.0		*	*	μsec
Slew Rate			20			*		V/μsec
REFERENCE								
Internal Reference								
Voltage		+6.17	+6.3	+6.43	*	*	*	V
Drift			±5			*		ppm/°C
External Current				1.0			*	mA[7]
POWER SUPPLY								
Power Supply Range								
+15V Supply		±11.4	±12, ±15	±16.5	*	*	*	V
+5V Supply		+4.5	+5.0	+5.5	*	*	*	V
Quiescent Current								
+15V			8	13		*	*	mA
-15V			-14	-25		*	*	mA
+5V			10	12		*	*	mA
Power Consumption	Quiescent		380	630		*	*	mW
Power Supply Rejection								
+15VDC			±0.002			*		±FSR/%VS
-15VDC			±0.002			*		±FSR/%VS
+5VDC			±0.002			*		±FSR/%VS
THERMAL CHARACTERISTICS								
Operating Temp	Ambient	See Ordering Information				*		
Storage Temp Range	Ambient	-65		+150	*		*	°C
Thermal Impedance								
Case to Ambient, θ_{CA}			20			*		°C/W
Junction to Case, θ_{JC}			17			*		°C/W

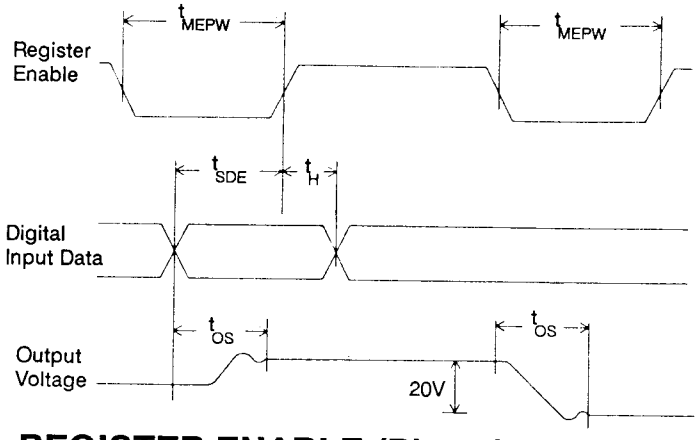
* Specifications are the same as DACHK.

Notes:

1. An HCT load is defined as ± 5 μA max. at OV < V_{IN} < V_{LOGIC}, 10 pF max. A TTL load is defined as 4-μA max. at V_{IN} = 2.4V and -1.6mA max. at V_{IN} = 0.4V.
2. BIN = Binary; OBIN = Offset Binary; 2's CBIN = Two's Complement Binary; 2's COBIN = Two's Complement Offset Binary.
3. Externally adjustable to zero. This specification is without external adjustment.
4. FSR= Full Scale Range. The ± 10V analog output range is a 20V FSR. The ± 5V or 0 to 10V output range is a 10V FSR.
5. Gain drift is defined as the absolute value of the change from +25° C to the hot temperature, plus the absolute value of the change from +25 °C to the cold temperature, and that quantity is divided by the temperature span. This is a 3-point drift with the change to hot usually greater than the change to cold.
6. ± 1 LSB = ± 0.024% FSR.
7. External current is for constant load. A dynamic load may degrade performance.

ABSOLUTE MAXIMUM RATINGS	
Supply Voltage	± 16.5VDC
Logic Supply Voltage	+7VDC
Digital Inputs	+5.5VDC
Storage Temperature	-65° C to +150° C
Lead Temperature (Soldering, 60 sec.)	+300° C
Junction Temperature	+150° C

TIMING DIAGRAM



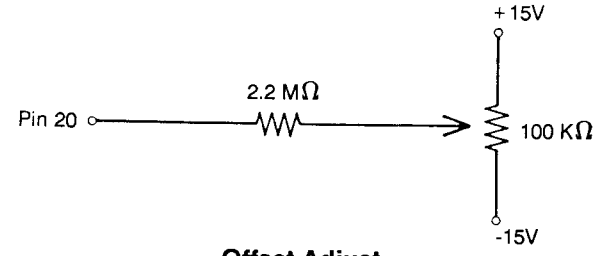
REGISTER ENABLE (Pin 16)

When Register Enable is high (hold mode) the digital data in the input register will be latched. When Register Enable is low (track mode) the converter's output will follow its input. To latch new data into the register, Register Enable must go low for 60 nsec. minimum. Digital input data must be valid for 40 nsec. minimum prior to Register Enable going high again.

t_{MEPW} - Enable pulse width is 60 nsec. minimum.
t_{SDE} - Setup time for digital input data to enable is 40 nsec. minimum.
t_H - Hold time is zero.
t_{OS} - Output settling time.

OFFSET AND GAIN CALIBRATION (OPTIONAL)

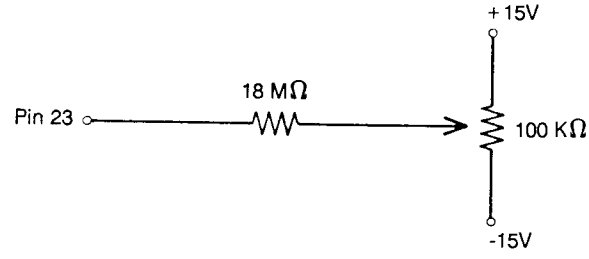
Offset and gain errors may be trimmed to zero by using potentiometers. Use a multiturn potentiometer with 100ppm/ °C or better TCR and series resistors that have ±20% carbon composition or better.



Offset Adjust

Unipolar: Apply all "0's" to the digital inputs. Adjust the potentiometer until the analog output is equal to zero volts.

Bipolar: Offset binary - Apply all "0's" to the digital inputs. Adjust the potentiometer until the analog output is equal to minus full scale voltage. Two's complement - Apply a "1" and all "0's" to the digital inputs. Adjust the potentiometer until the analog output is equal to minus full scale voltage.



Gain Adjust

Unipolar: Apply all "1's" to the digital inputs. Adjust the potentiometer until the analog output is equal to the maximum positive voltage for the selected output range.

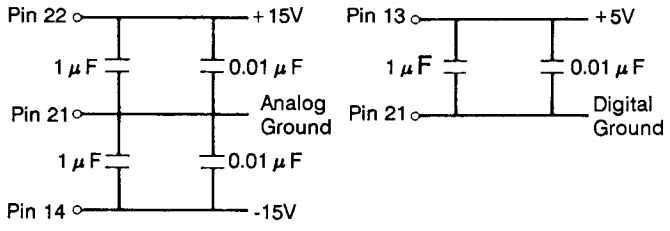
Bipolar: Offset binary - Apply all "1's" to the digital inputs. Adjust the potentiometer until the analog output is equal to the maximum positive voltage for the selected output range. Two's complement - Apply a "0" and all "1's" to the digital inputs. Adjust the potentiometer until the analog output is equal to the maximum positive voltage for the selected output range.

PIN DESIGNATIONS

Pin 1	Bit 1 (MSB)	Pin 24	Ref out (+6.3V)
Pin 2	Bit 2	Pin 23	Gain adjust
Pin 3	Bit 3	Pin 22	+15V supply
Pin 4	Bit 4	Pin 21	Ground
Pin 5	Bit 5	Pin 20	Summing Junction
Pin 6	Bit 6	Pin 19	20V range
Pin 7	Bit 7	Pin 18	10V range
Pin 8	Bit 8	Pin 17	Bipolar offset
Pin 9	Bit 9	Pin 16	Register enable
Pin 10	Bit 10	Pin 15	Analog output
Pin 11	Bit 11	Pin 14	-15V supply
Pin 12	Bit 12 (LSB)	Pin 13	+5V supply

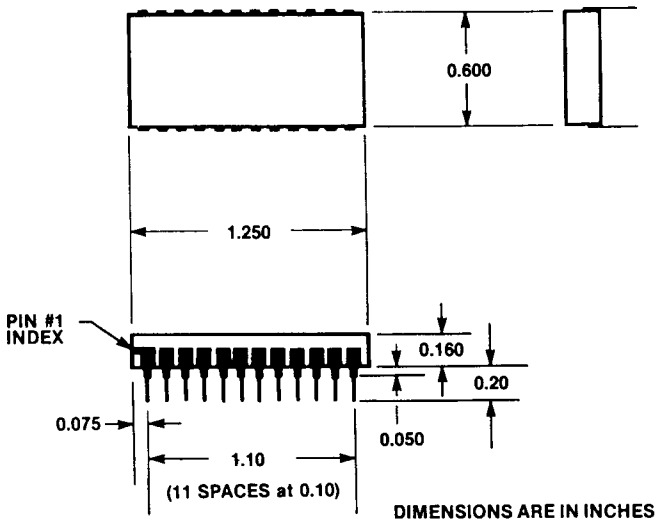
HANDLING OF GROUNDS

Power supplies should be decoupled by using tantalum or electrolytic capacitors. An optimal configuration is achieved by using 1 μF capacitors in parallel with 0.01 μF ceramic capacitors.



Power Supply Decoupling

MECHANICAL OUTLINE



PART NUMBER

DACHK - x x /x

Code
-2 - Two's complement
Omit for binary

Temperature
E - -25°C to +85°C
H - -55°C to +125°C
Omit for 0°C to +70°C

/ B - Military screening
("H" temp range only)
Omit for standard screening

INPUT LOGIC CODING

STRAIGHT BINARY MSB LSB	OUTPUT RANGES 0 to +5V	0 to +10V
1111 1111 1111	+4.9988	+9.9976
1100 0000 0000	+3.7500	+7.5000
1000 0000 0000	+2.5000	+5.0000
0100 0000 0000	+1.2500	+2.5000
0000 0000 0001	+0.0012	+0.0024
0000 0000 0000	0.0000	0.0000

OFFSET BINARY MSB LSB	TWO's COMPLEMENT MSB LSB	OUTPUT RANGES ±2.5V	±5V	±10V
1111 1111 1111	0111 1111 1111	+2.4988	+4.9976	+9.9951
1100 0000 0000	0100 0000 0000	+1.2500	+2.5000	+5.0000
1000 0000 0000	0000 0000 0000	0.0000	0.0000	0.0000
0100 0000 0000	1100 0000 0000	-1.2500	-2.5000	-5.0000
0000 0000 0001	1000 0000 0001	-2.4988	-4.9976	-9.9951
0000 0000 0000	1000 0000 0000	-2.5000	-5.0000	-10.0000

OUTPUT RANGE SELECTION

Pin Connections Output Range	0 to +5V	0 to +10V	±2.5V	±5V	±10V
Connect pin 15 to	18	18	18	18	19
Connect Pin 17 to	21	21	20	20	20
Connect Pin 19 to	20	-	20	-	15

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