REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
C	Add device types 03, 04, 05, 06, and 07. Add approved source CAGE 66632. Add case outline Y. Editorial changes throughout. Change to military drawing format and new code ident. no. 67268.	1987 OCT 23	M. A. Frye
D	Make changes to table I, table II, 1.2.2, 3.3, 4.3.1, 4.3.2, and figures 1, 2, 3, and 4.	1989 JAN 03	M. A. Frye
E	Added devices 08 and 09. Remove CAGE number 66632 as a supplier. Updated boilerplate, editorial changes throughout.	1993 OCT 12	M. A. Frye

DEVICES 8102401VX AND 8102402VX ARE INACTIVE FOR NEW DESIGN AS OF 22 OCT 1985. USE M38510/24501BVX or M38510/24502BVX.

THE ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED.

REV																			
SHEET																			
REV	D	D	D	D	D	D	D	C	E	E	E	E	E						
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27						

REV STATUS OF SHEETS	REV	E	E	E	E	E	E	E	E	E	E	E	E	D	D
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
Kenneth Rice

CHECKED BY
Ray Monnin

APPROVED BY
Michael A. Frye

DRAWING APPROVAL DATE
10 AUGUST 1982

REVISION LEVEL
E

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, DIGITAL, CMOS, 4096 BIT, STATIC RANDOM ACCESS MEMORY (SRAM), MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	81024

SHEET 1 OF 27

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:

1.2.1 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number 1/	Access time	Circuit
01		120 ns	4096-word x 1-bit static random access memory
02		120 ns	1024-word x 4-bit static random access memory
03		200 ns	4096-word x 1-bit static random access memory
04		200 ns	1024-word x 4-bit static random access memory
05		300 ns	4096-word x 1-bit static random access memory
06		300 ns	1024-word x 4-bit static random access memory
07		55 ns	4096-word x 1-bit static random access memory
08		80 ns	4096-word x 1-bit static random access memory
09		80 ns	4096-word x 1-bit static random access memory

1.2.2 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
V	GDIP1-T18 or CDIP2-T18	18	Dual-in-line package
X	CQCC1-N18	18	Rectangular chip carrier package
Y	See figure 1	18	Flat package

1.2.3 Lead finish. The lead finish shall be as specified in MIL-M-38510. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings.

Supply voltage range (V_{DD}) (device type 07, 08, and 09)	V_{SS} -0.5 V to +7.0 V
Supply voltage range (V_{DD}) (device type 01-06)	V_{SS} -0.3 V to +8.0 V
Temperature under bias	-55°C to +125°C
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D) 2/	200 mW
Lead temperature (soldering, 10 seconds)	+260°C
Thermal resistance, junction-to-case (O_{JC}):	
Cases V and X	See MIL-STD-1835
Case Y	40°C/W 3/
Junction temperature (T_J)	+150°C
All input or output voltages with respect to ground	V_{SS} -0.3 V to V_{CC} +0.3 V

1/ Generic numbers are listed on the Standardized Military Drawing Source Approval Bulletin at the end of this document and will also be listed in MIL-BUL-103.
2/ Must withstand the added P_D due to short circuit test; e.g., I_{OS}.
3/ When the thermal resistance for this case is specified in MIL-STD-1835, that value shall supersede the value indicated herein.

1.4 Recommended operating conditions.

Supply voltage range (V_{DD} - V_{SS})	4.5 V dc to 5.5 V dc
Input low (V_{IL}) voltage range	V_{SS} -0.3 V dc to V_{SS} +0.8 V dc
Input high (V_{IH}) voltage range	V_{DD} -2.0 V dc to V_{DD} +0.3 V dc
Input high (V_{IH}) voltage range	2.0 V dc to 6.0 V dc
Case operating temperature range (T_C)	-55°C to +125°C
Chip enable output enable time (TELQX)	5 ns minimum
Chip enable output disable time (TEHQZ):	
Device types 01 and 02	70 ns maximum
Device types 03 and 04	80 ns maximum
Device types 05 and 06	100 ns maximum
Device type 07, 08, 09	30 ns maximum

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and bulletin. Unless otherwise specified, the following specification, standards, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

(Copies of the specification, standards, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Logic diagram(s). The logic diagram(s) shall be as specified on figure 3.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103 (see 6.6 herein).

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.6 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-EC shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance.

d. Subgroups 7 and 8 shall include verification of the truth table.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions V_{SS} = 0 V, 4.5 V ≤ V_{DD} ≤ 5.5 V, -55°C ≤ T_C ≤ +125°C 1/ unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Low level output voltage	V_{OL}	V_{DD} = 4.5 V, I_{OL} = 2 mA	1, 2, 3	All		0.4	V
High level output voltage	V_{OH}	V_{DD} = 4.5 V, I_{OH} = -1 mA	1, 2, 3	All	2.4		V
Positive clamping input to V_{DD}	V_{IC} (pos)	T_C = +25°C, V_{SS} = 0.0 V, I_{IN} = 100 µA	1	01, 02, 03, 04, 05, 06	0.2	2.0	V
Negative clamping input to V_{SS}	V_{IC} (neg)	T_C = +25°C, V_{SS} = 0.0 V, I_{IN} = -100 µA	1	01, 02, 03, 04, 05, 06	-0.2	-2.0	V
Input leakage current	I_{IH}, I_{IL}	V_{DD} = 5.5 V, V_{IN} = 0.0 V or 5.5 V	1, 2, 3	01, 02, 03, 04, 05, 06	-0.1	1.0	µA
				07,08,09	-10.0	10.0	
High impedance output leakage current	I_{OZ}	V_{DD} = 5.5 V, V_O = V_{DD}	1, 2, 3	01, 02, 03, 04, 05, 06	-1.0	1.0	µA
				07,08,09	-10	10	
Quiescent supply current	I_{DD}	V_{DD} = 5.5 V, V_{IN} = V_{DD} and GND, I_O = 0.0 mA; $\overline{CE}$ = V_{DD} -0.3 V	1, 2, 3	01, 02, 03, 04, 05, 06		50	µA
			1	07,08,09		100	
			2, 3			1000	
Data retention supply current	I_{DR}	V_{DD} = 2.0 V minimum, V_{IN} = V_{DD} and GND, I_O = 0.0 mA, $\overline{CE}$ = V_{DD}	1, 2, 3	01, 02, 03, 04, 05, 06		25	µA
		V_{DD} = 2.5 V minimum	1	08, 09		40	
			2, 3			400	
Operating current	I_{DDOP}	V_{DD} = 5.5 V, f = 1 MHz, I_O = 0 mA, V_{IN} = V_{DD} 2/	1, 2, 3	01, 02, 03, 04, 05, 06		7	mA
Output short circuit current 3/	I_{OS}	V_{DD} = 5.5 V, V_{OUT} = GND	1, 2, 3	07		-350	mA
Operating supply current	I_{DD}	V_{DD} = 5.5 V, I_O = 0 mA	1, 2, 3	07		140	mA
				08, 09		4.5	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions V_{SS} = 0 V, 4.5 V ≤ V_{DD} ≤ 5.5 V, -55°C ≤ T_C ≤ +125°C 1/ unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Automatic $\overline{CE}$ power down current 4/	I_{SB}	V_{DD} = 5.5 V, $\overline{CE}$ = 2.0 V	1, 2, 3	07		25	mA
Data retention supply voltage	V_{DR}	$\overline{CE}$ = V_{DD}	1, 2, 3	01, 02, 03, 04, 05, 06, 08, 09	2.0		V
Input capacitance	C_{IN}	f = 1 MHz, T_A = +25°C, All measurements referenced to device ground See 4.3.1c	4	01, 02, 03, 04, 05, 06 07, 08, 09		8.0	pF
Output capacitance	C_{OUT}	f = 1 MHz, T_A = +25°C, All measurements referenced to device ground See 4.3.1c	4	01, 02, 03, 04, 05, 06 07, 08, 09		10.0	pF
Functional test		V_{DD} = 4.5 V and 5.5 V 5/ 6/ See 4.3.1d	7,8A,8B	All			
Address access time	TAVQV	V_{DD} = 4.5 V and 5.5 V 7/ 8/	9, 10, 11	01, 02		120	ns
				03, 04		220	
				05, 06		320	
				07,		55	
Chip enable access time	TELQV	V_{DD} = 4.5 V and 5.5 V 7/ 8/	9, 10, 11	01, 02		120	ns
				03, 04		200	
				05, 06		300	
				07,		55	
				08, 09		80	
Chip enable pulse negative width	TELEH	V_{DD} = 4.5 V and 5.5 V 7/ 8/	9, 10, 11	01, 02	120		ns
				03, 04	200		
				05, 06	300		
				07	55		
				08, 09	80		
Chip enable pulse positive width	TEHEL	V_{DD} = 4.5 V and 5.5 V 7/ 8/	9, 10, 11	01, 02	50		ns
				03, 04	90		
				05, 06	120		
				08, 09	40		
Address setup time	TAVEL	V_{DD} = 4.5 V and 5.5 V 7/ 8/	9, 10, 11	01, 02	0		ns
				03, 04 05, 06	20		
				08, 09	15		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions V_{SS} = 0 V, 4.5 V ≤ V_{DD} ≤ 5.5 V, -55°C ≤ T_C ≤ +125°C 1/ unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Address hold time	TELAX	V_{DD} = 4.5 V and 5.5 V 7/ 8/	9, 10, 11	01, 02	40		ns
				03, 04, 05, 06	50		
				09	15		
Address hold time	TEHAX	V_{DD} = 4.5 V and 5.5 V 7/ 8/	9, 10, 11	08	15		ns
Write enable pulse width	TWLWH	V_{DD} = 4.5 V and 5.5 V 7/ 8/	9, 10, 11	01	20		ns
				02	120		
				03	60		
				04	200		
				05	80		
				06	300		
				07	25		
				08, 09	70		
Write enable pulse setup time	TWLEH	V_{DD} = 4.5 V and 5.5 V 7/ 8/	9, 10, 11	01	70		ns
				02	120		
				03	150		
				04, 05	200		
				06	300		
				08, 09	70		
Early write pulse setup time	TWLEL	V_{DD} = 4.5 V and 5.5 V 7/ 8/	9, 10, 11	01, 02, 03, 04, 05, 06	0		ns
Write enable pulse hold time	TELWH	V_{DD} = 4.5 V and 5.5 V 7/ 8/	9, 10, 11	01	40		ns
				02	120		
				03	60		
				04	200		
				05	80		
				06	300		
				07	45		
				08, 09	70		
Read or write 9/ cycle time	TELEL	V_{DD} = 4.5 V and 5.5 V 7/ 8/	9, 10, 11	01, 02	170		ns
				03, 04	290		
				05, 06	420		
				08, 09	135		
Data setup time	TDVWL	V_{DD} = 4.5 V and 5.5 V 7/ 8/	9, 10, 11	01, 03, 05	0		ns
				02	50		
	TDVWH			04	120		
				06	200		
				08, 09	60		
Data hold time	TWLDX	V_{DD} = 4.5 V and 5.5 V 7/ 8/	9, 10, 11	01	25		ns
				03	60		
				05	80		
				07	10		
	TWHDX			02, 04, 06	0		
				08, 09	15		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions V_{SS} = 0 V, 4.5 V ≤ V_{DD} ≤ 5.5 V, -55°C ≤ T_C ≤ +125°C 1/ unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Early write data setup time	TDVEL	V_{DD} = 4.5 V and 5.5 V 7/ 8/	9, 10, 11	01, 03, 05	0		ns
Early write data hold time	TELDX	V_{DD} = 4.5 V and 5.5 V 7/ 8/	9, 10, 11	01	25		ns
				03	60		
				05	80		
Write data delay time	TWLDV	V_{DD} = 4.5 V and 5.5 V 7/ 8/	9, 10, 11	02	70		ns
				04	80		
				06	100		
Late output disable time	TEHWH	V_{DD} = 4.5 V and 5.5 V 7/ 8/	9, 10, 11	02, 04, 06	0		ns
Read cycle 9/ 10/ time 11/	TAVAV		9, 10, 11	07	55		ns
Data hold from 10/ address time 11/	TAVQX		9, 10, 11	07	5		ns
$\overline{CE}$ low to low Z 10/ 11/	TELQX		9, 10, 11	All	5		ns
$\overline{CE}$ high to high Z 12/	TEHQZ		9, 10, 11	01, 02		70	ns
				03, 04		80	
				05, 06		100	
				07,08,09		30	
$\overline{CE}$ low to power-up 10/ 11/	TPU		9, 10, 11	07	0		ns
$\overline{CE}$ high to power-down 10/ 11/	TPD		9, 10, 11	07		20	ns
Address setup to write end 10/ 11/	TAZEL+ TELWH		9, 10, 11	07	45		ns
Address hold from write end 10/ 11/	TWHAX		9, 10, 11	07	10		ns
Data setup to write end 10/ 11/	TDVWH		9, 10, 11	07	25		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions V_{SS} = 0 V, 4.5 V ≤ V_{DD} ≤ 5.5 V, -55°C ≤ T_C ≤ +125°C 1/ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
$\overline{WE}$ high to low 10/ 11/	TWHQX		9, 10, 11	07	0		ns
$\overline{WE}$ low to high Z 12/	TWLQZ		9, 10, 11	07	0	25	ns

1/ All voltages referenced to GND.

2/ Operating supply current is proportional to operating frequency.

3/ Duration of short circuit not to exceed 30 seconds.

4/ A pull-up resistor to V_{DD} on the $\overline{CE}$ input is required to keep the device deselected during V_{DD} power-up, otherwise I_{SB} will exceed values given.

5/ Performed during ac switching testing.

6/ Tested as follows: f = 3 MHz, V_{IH} = 2.4 V, V_{IL} = 0.4 V, I_{OH} = -4.0 mA, I_{OL} = 4.0 mA V_{OH} ≥ 1.5 V, and V_{OL} ≤ 1.5 V.

7/ See figure 4 for ac waveforms.

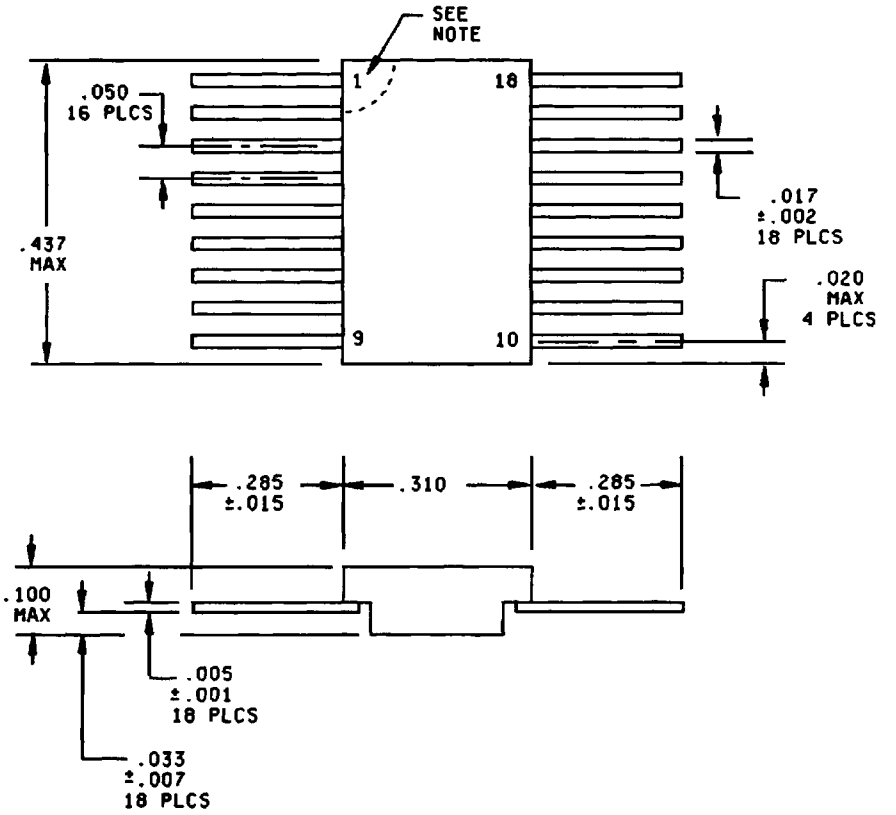
8/ $t_{TLH} = t_{THL} \leq 5$ ns; output load: C_L = 50 to 300 pF; for C_L > 50 pF, access times are derated .15 ns/pF; $V_{IH} = V_{DD} - 2.0$ V; and V_{IL} = 0.8 V.

9/ The internal write time of the memory is defined by the overlap of $\overline{CE}$ low and $\overline{WE}$ low. Both signals must be low to initiate a write and either signal can terminate a write by going high. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.

10/ Test conditions assume signal transistion times of 5 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V and output loading of the specified I_{OL}/I_{OH}. See figure 4 for ac switching test circuits and waveforms. C_L = 30 pF unless otherwise specified.

11/ Tests may be performed at V_{DD} = 4.5 V, provided the manufacturer guarantees that the devices meet limits specified when tested at V_{DD} = 4.5 V to 5.5 V.

12/ TEHQZ and TWLQZ are tested with C_L = 5 pF. Transistion is measured ±500 mA from steady-state voltage.



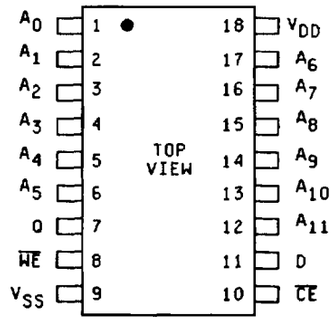
Inches	mm
.001	0.03
.002	0.05
.005	0.13
.007	0.18
.015	0.38
.017	0.43
.020	0.51
.033	0.84
.050	1.27
.100	2.54
.285	7.24
.310	7.87
.437	11.10

NOTE: Terminal one shall be identified by a mechanical index on the lead or body, or a mark on the top surface within the regional shown.

FIGURE 1. Case outline Y flat package.

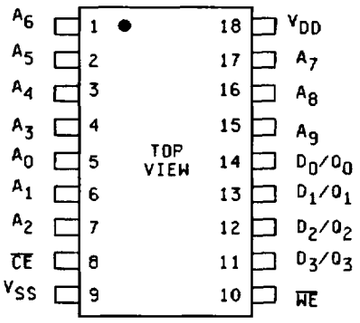
Device types 01, 03, 05, 07, 08, and 09

CASE V



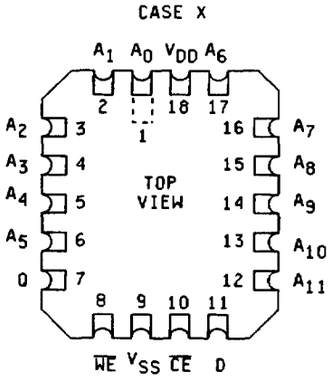
Device types 02, 04, and 06

CASE V



Device types 01, 03, 05 and 07

CASE X



Device types 02, 04, and 06

CASE X

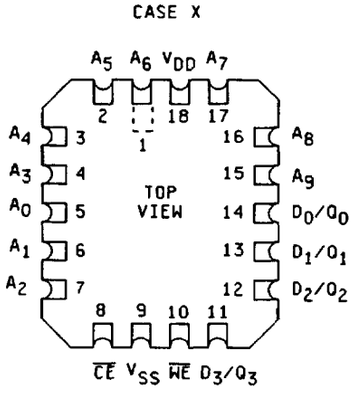


FIGURE 2. Terminal connections.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		81024
		REVISION LEVEL E	SHEET 11

Device types 01, 03, 05, 07, 08, and 09

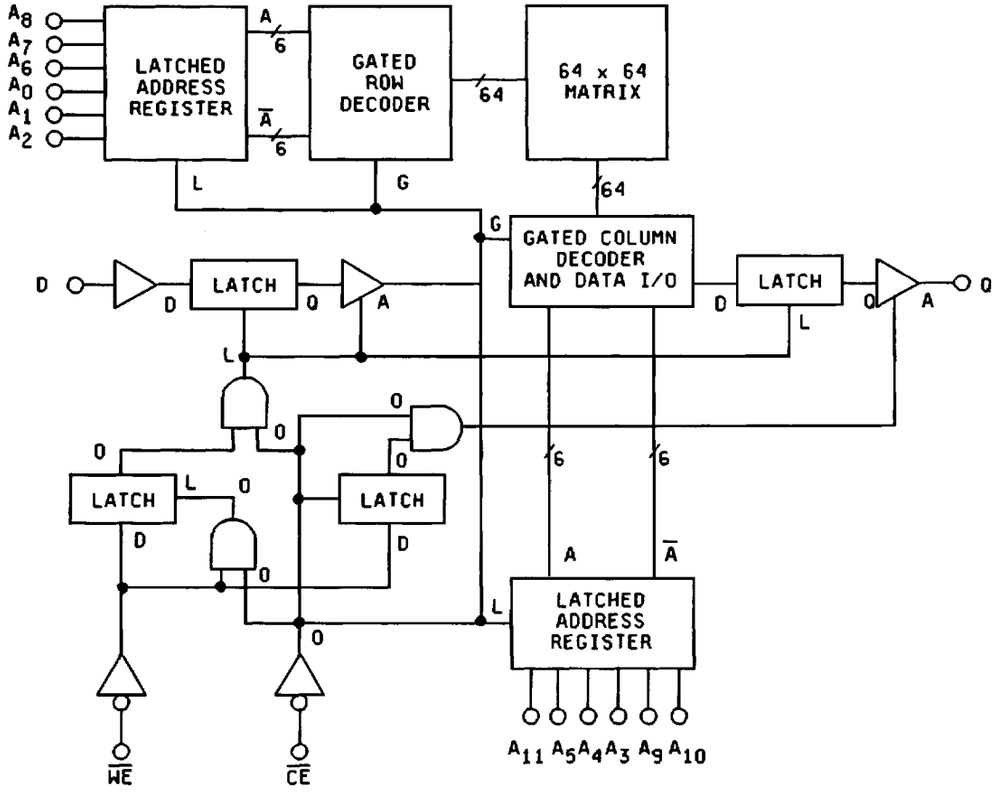


FIGURE 3. Logic diagrams.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		81024
		REVISION LEVEL E	SHEET 12

Device types 02, 04, and 06

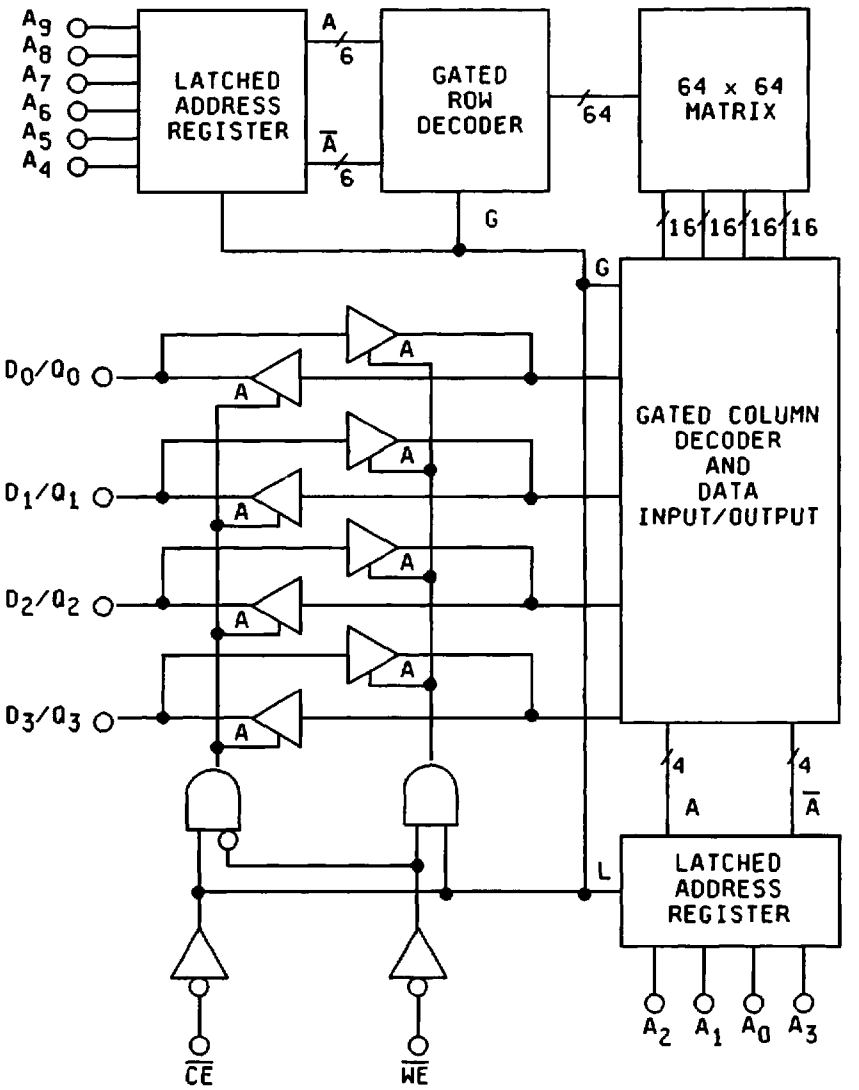
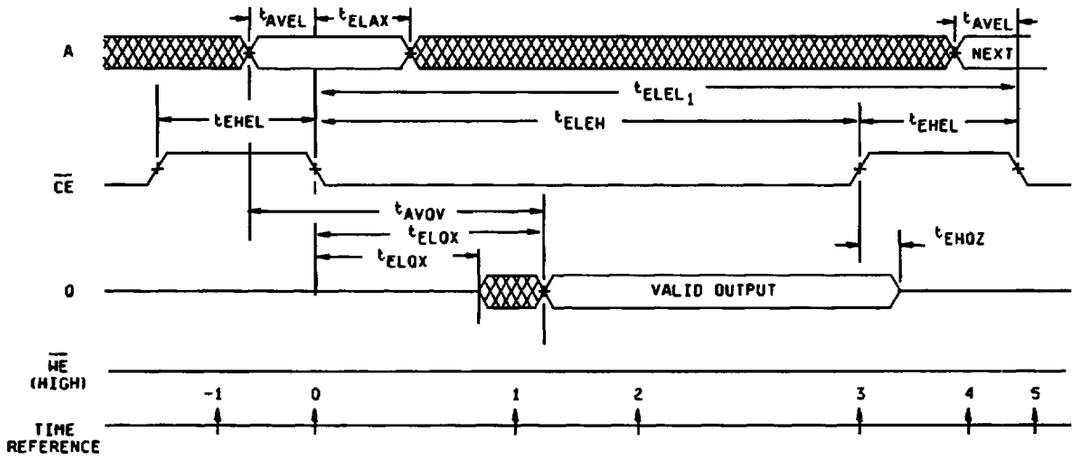


FIGURE 3. Logic diagrams - Continued.

Device types 01, 03, and 05



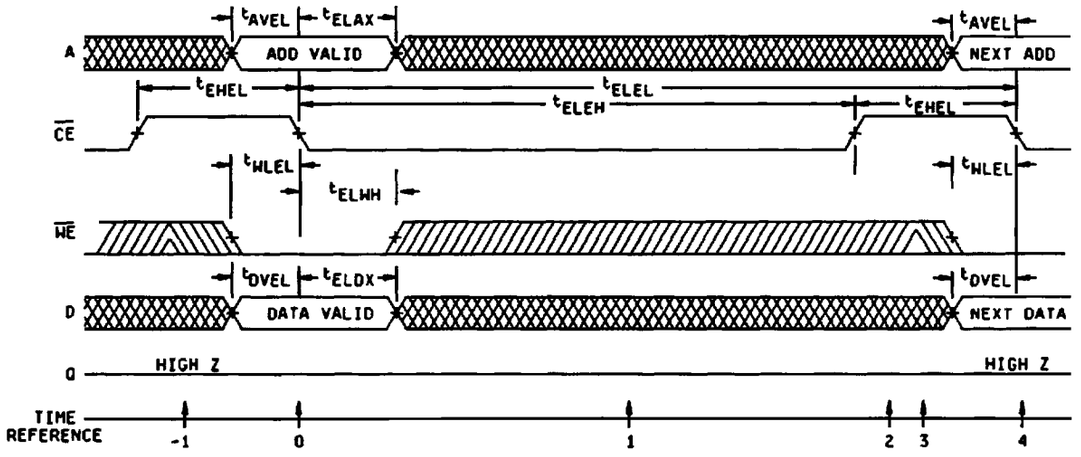
Truth table

Time reference	Inputs CE	WE	A	Output Q	Function
-1	H	X	X	Z	Memory disable
0	↓	H	V	Z	Cycle begins, addresses are latched
1	L	H	X	X	Output enable
2	L	H	X	V	Output valid
3	↑	H	X	V	Read accomplished
4	H	X	X	Z	Prepare for next cycle (same as -1)
5	↓	H	V	Z	Cycle ends, next cycle begins (same as 0)

The address information is latched in the on chip registers on the falling edge of CE (T = 0). Minimum address set up and hold time requirements must be met. After the required hold time, the addresses may change state without affecting device operation. During time (T = 1) the output becomes enabled but data is not valid until during time (T = 2). WE must remain high until after time (T = 2). After the output data has been read, CE may return high (T = 3). This will disable the output buffer and ready the RAM for the next memory cycle (T = 4).

FIGURE 4. Read cycle, write cycle, read/modify/write cycle waveforms and truth tables.

Device types 01, 03, and 05



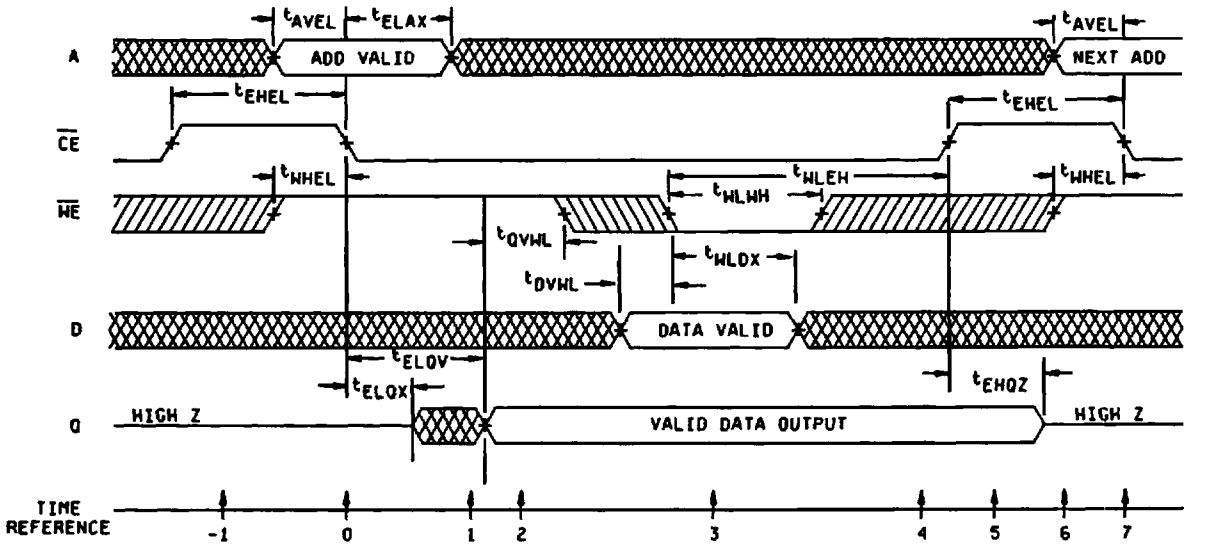
Truth table

Time reference	Inputs $\overline{CE}$	$\overline{WE}$	A	D	Output Q	Function
-1	H	X	X	X	Z	Memory disabled
0	↓	L	V	V	Z	Cycle begins, addresses are latched
1	L	X	X	X	Z	Write in progress internally
2	↑	X	X	X	Z	Write completed
3	H	X	X	X	Z	Prepare for next cycle (same as -1)
4	↓	L	V	V	Z	Cycle ends, next cycle begins (same as 0)

The early write cycle is the only cycle where the output is guaranteed not to become active. On the falling edge of $\overline{CE}$ (T = 0), the addresses, the write signal, and the data input are latched in on chip registers. The logic value of $\overline{WE}$ at the time $\overline{CE}$ falls determines the state of the output buffer for that cycle. Since $\overline{WE}$ is low in the early write cycle the output buffer is latched into the high impedance state and will remain in the state until CE returns high (T = 2). For this cycle, the data input is latched by $\overline{CE}$ going low; therefore data set up and hold times should be referenced to CE. When CE (T = 2) returns to the high state the output buffer disables and signals are unlatched. The device is now ready for the next cycle.

FIGURE 4. Read cycle, write cycle, read/modify/write cycle waveforms and truth tables - Continued.

Device types 01, 03, and 05



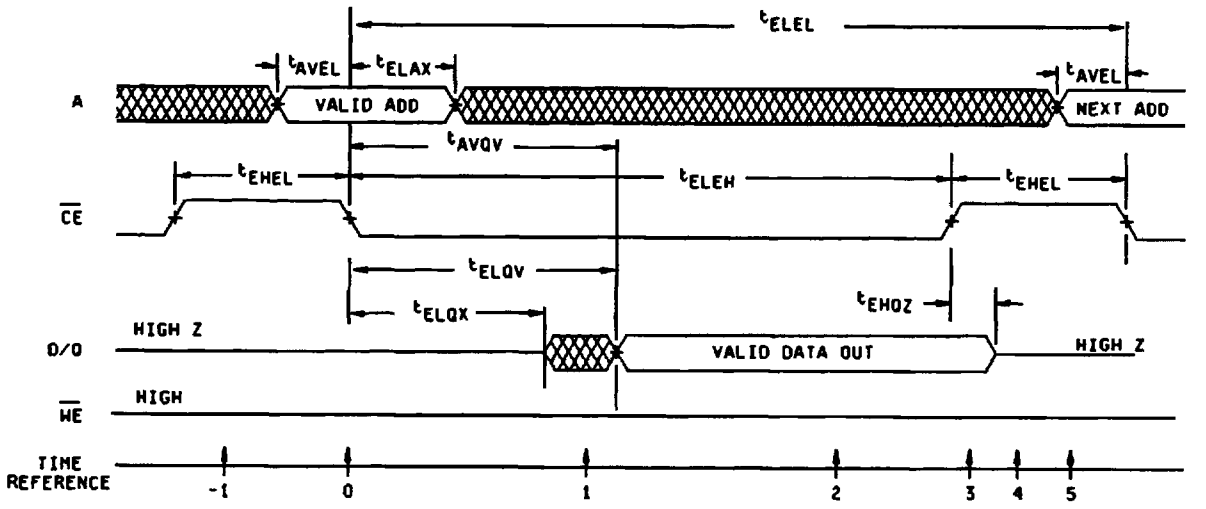
Truth table

Time reference	Inputs CE	WE	A	D	Output Q	Function
-1	H	X	X	X	Z	Memory disabled
0	↓	H	V	X	Z	Cycle begins, addresses are latched
1	L	H	X	X	X	Output disabled
2	L	H	X	X	V	Output valid, read and modify time
3	L	↓	X	V	V	Write begins, data is latched
4	L	X	X	X	V	Write in progress internally
5	↑	X	X	X	V	Write completed
6	H	X	X	X	Z	Prepare for next cycle (same as -1)
7	↓	H	V	X	Z	Cycle ends, next cycle begins (same as 0)

The ready modify write cycle begins at all other cycles on the falling edge of $\overline{CE}$ (T = 0). The $\overline{WE}$ line should be high at (T = 0) in order to latch the output buffers in the active state. During (T = 1) the output will be active but not valid until (T = 2). On the falling edge of the $\overline{WE}$ (T = 3) the data present at the output and input are latched. The $\overline{WE}$ signal also latches itself on its low going edge. All input signals excluding $\overline{CE}$ have been latched and have no further effect on the RAM. The rising edge of $\overline{CE}$ (T = 5) completes the write portion of the cycle and unlatches all inputs and the output. The output goes to a high impedance and the RAM is ready for the next cycle.

FIGURE 4. Read cycle, write cycle, read/modify/write cycle waveforms and truth tables - Continued.

Device types 02, 04, and 06

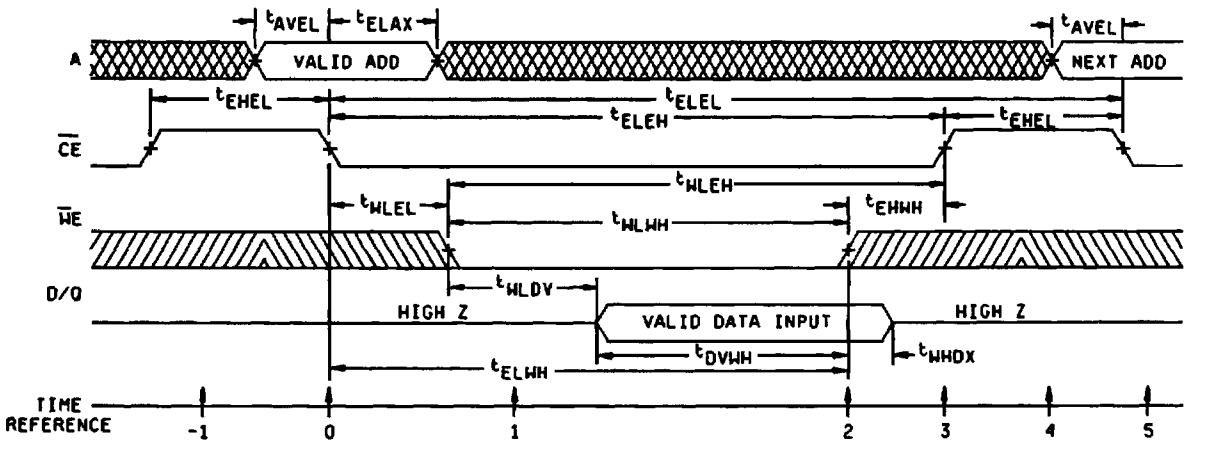


Truth table

Time reference	Inputs CE	WE	A	Data I/O D/Q	Function
-1	H	X	X	Z	Memory disable
0	↓	H	V	Z	Cycle begins, addresses are latched
1	L	H	X	X	Output enabled
2	L	H	X	V	Output valid
3	↑	H	X	V	Read accomplished
4	H	X	X	Z	Prepare for next cycle (same as -1)
5	↓	H	V	Z	Cycle ends, next cycle begins (same as 0)

The address information is latched in the on chip registers on the falling edge of $\overline{CE}$ (T = 0). Minimum address set up and hold time requirements must be met. After the required hold time, the addresses may change state without affecting device operation. During time (T = 1) the output becomes enabled but data is not valid until time (T = 2). $\overline{WE}$ must remain high throughout the read cycle. After the data has been read, $\overline{CE}$ may return high (T = 3). This will force the output buffers into a high impedance mode at times (T = 4). The memory is now ready for the next cycle.

FIGURE 4. Read cycle, write cycle, read/modify/write cycle waveforms and truth tables - Continued.



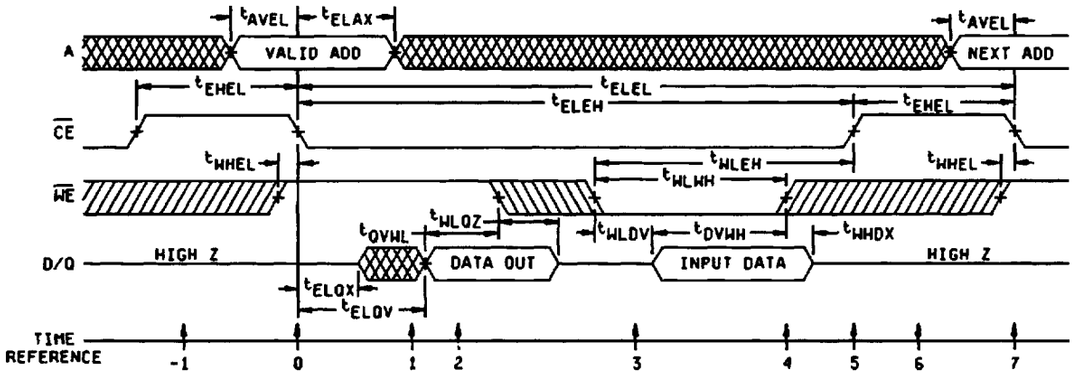
Truth table I

Time reference	Inputs $\overline{CE}$	$\overline{WE}$	A	D/Q	Function
-1	H	X	X	Z	Memory disabled
0	↓	H	V	Z	Cycle begins, addresses are latched
1	L	L	X	Z	Write period begins
2	L	↑	X	V	Data in is written
3	↑	H	X	Z	Write completed
4	H	X	X	Z	Prepare for next cycle (same as -1)
5	↓	H	V		Cycle ends, next cycle begins (same as 0)

The write cycle is initiated on the falling edge of $\overline{CE}$ (T = 0), which latches the address information in on chip registers. If a dedicated write cycle is to be performed and the outputs are not to become active TWLEL amd TEHWH must be met. Under these conditions TWLDV is unnecessary and input data may be applied at any convenient time as long as TDVWH is still met. If TWLEL is not met then the outputs may become enabled momentarily near the beginning of the cycle and a disable time (TELQZ) must be met before the input data is applied (TWLQZ = TWLDV). Similiarly, if TEHWH is not met the outputs may enable briefly near the end of the cycle.

The write operation is terminated by the first rising edge of $\overline{WE}$ (T = 2) or $\overline{CE}$ (T = 3). After the minimum required $\overline{CE}$ high time (TEHEL) the next cycle may begin. If a series of consecutive write cycles are to be performed, the WE line may be held low until all desired locations have been written. In this case, data setup and hold times must be referenced to the rising edge of $\overline{CE}$.

FIGURE 4. Read cycle, write cycle, read/modify/write cycle waveforms and truth tables - Continued.

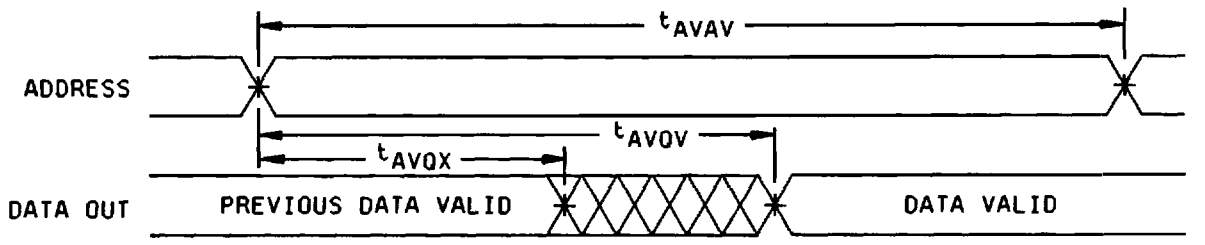


Truth table

Time reference	Inputs $\overline{CE}$	Inputs $\overline{WE}$	Inputs A	Data I/O D/Q	Function
-1	H	X	X	Z	Memory disabled
0	↓	H	V	Z	Cycle begins, addresses are latched
1	L	H	X	X	Read mode, output enabled
2	L	H	X	V	Read mode, output valid
3	L	L	X	Z	Write mode, output high Z
4	L	↑	X	V	Write mode, data is written
5	↑	H	X	V	Write completed
6	H	X	X	Z	Prepare for next cycle (same as -1)
7	↓	H	V	Z	Cycle ends, next cycle begins (same as 0)

If the pulse width of $\overline{WE}$ is relatively short in relation to that of $\overline{CE}$ as combination read-write cycle may be performed. If $\overline{WE}$ remains high for the first part of the cycle, the outputs will become active during time (T = 1). Data out will be valid during time (T = 2). After the data is read, $\overline{WE}$ can go low. After minimum TWLWH, $\overline{WE}$ may return high. The information just written may not be read or $\overline{CE}$ may return high, disabling the output buffers and preparing the device for the next cycle. Any number of sequence of read-write operations may be performed while $\overline{CE}$ is low providing all timing requirements are met.

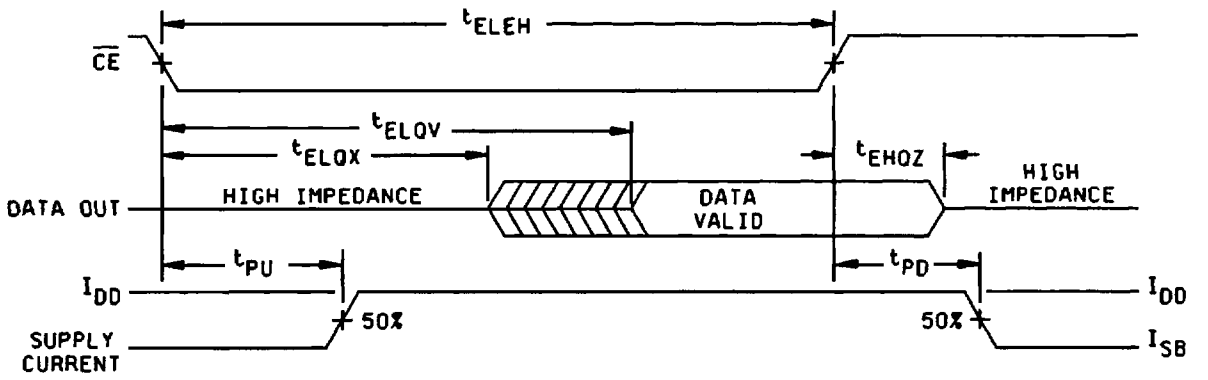
FIGURE 4. Read cycle, write cycle, read/modify/write cycle waveforms and truth tables - Continued.



$\overline{WE}$ is high for read cycle.
Device is continuously selected, $\overline{CE}$ = V_{IL}.

$\overline{CE}$	$\overline{WE}$	Mode	Output	Power
H	X	Not selected	High Z	Standby
L	L	Write	High Z	Active
L	H	Read	DO	Active

FIGURE 4. Read cycle, waveform - Continued.



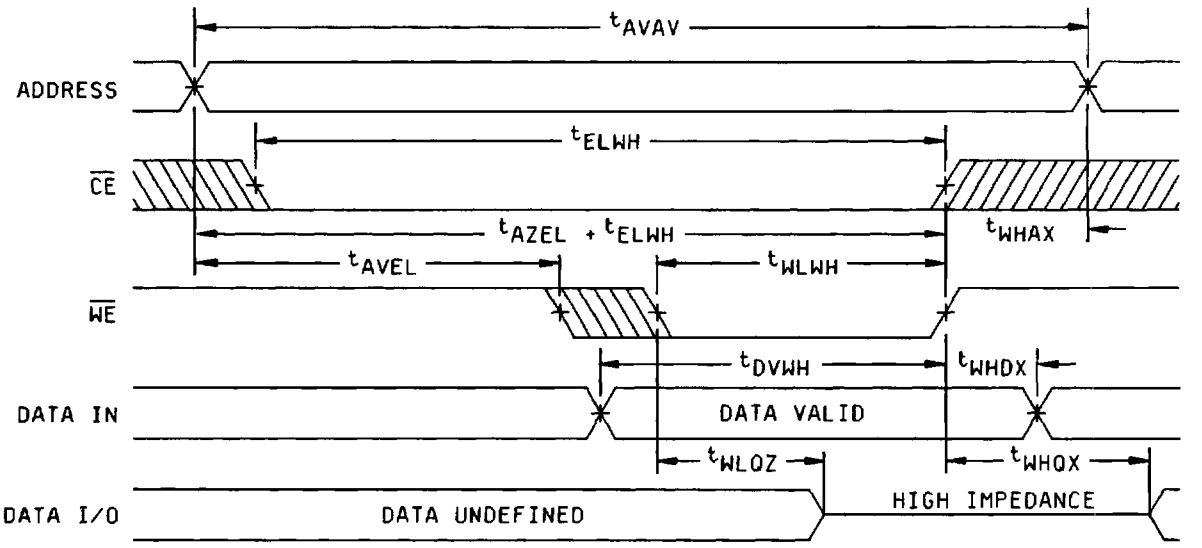
$\overline{WE}$ is high for read cycle.
Address valid prior to or coincident with $\overline{CE}$ transition low.

$\overline{CE}$	$\overline{WE}$	Mode	Output	Power
H	X	Not selected	High Z	Standby
L	L	Write	High Z	Active
L	H	Read	DO	Active

FIGURE 4. Read cycle, waveform - Continued.

Device type 07

$\overline{WE}$ (controlled)

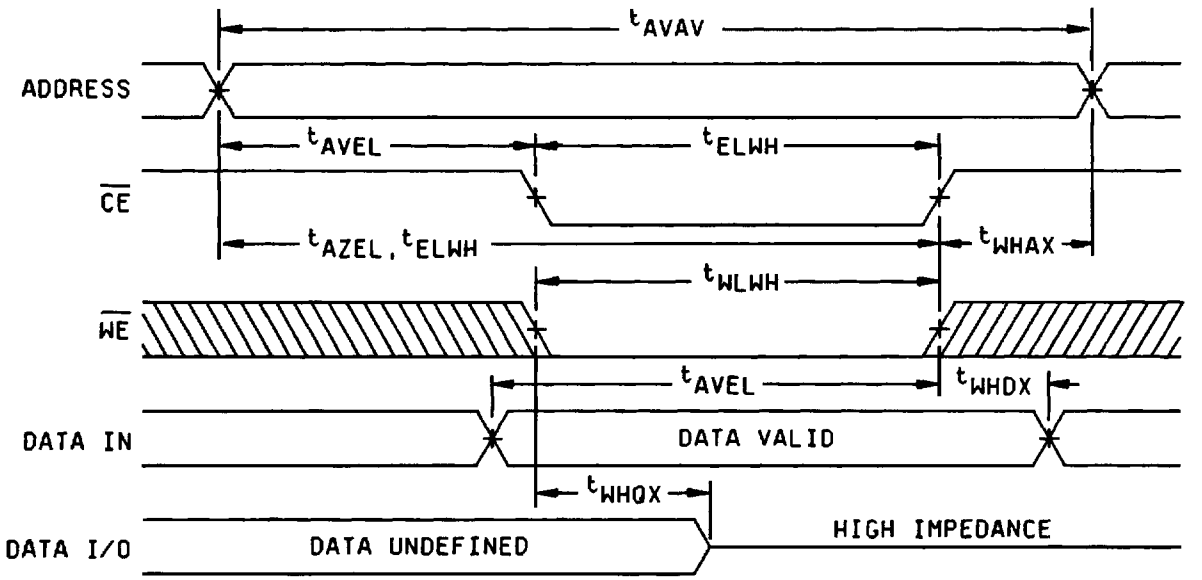


$\overline{CE}$	$\overline{WE}$	Mode	Output	Power
H	X	Not selected	High Z	Standby
L	L	Write	High Z	Active
L	H	Read	DO	Active

FIGURE 4. Write cycle, waveform - Continued.

Device type 07

$\overline{CE}$ (controlled)

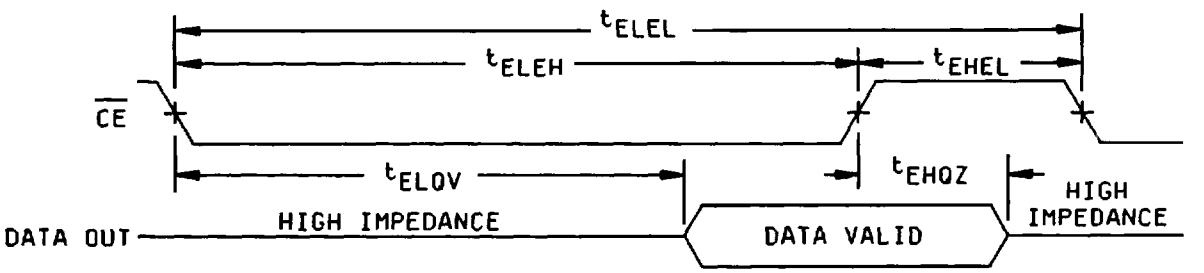


If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high impedance state.

$\overline{CE}$	$\overline{WE}$	Mode	Output	Power
H	X	Not selected	High Z	Standby
L	L	Write	High Z	Active
L	H	Read	DO	Active

FIGURE 4. Write cycle, waveform - Continued.

Device types 08 and 09

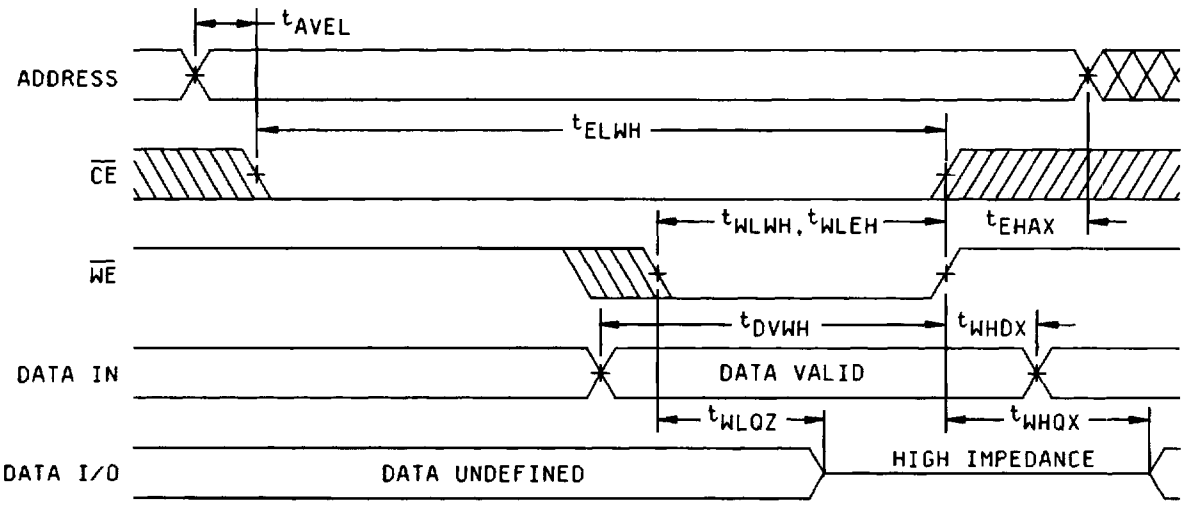


$\overline{WE}$ is high for read cycle

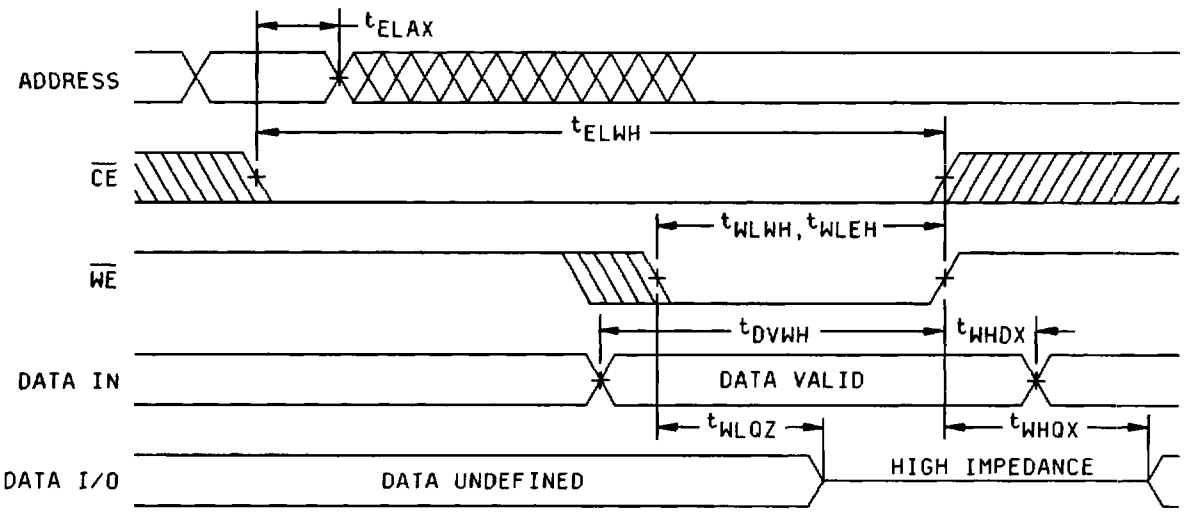
$\overline{CE}$	$\overline{WE}$	Mode	Output	Power
H	X	Not selected	High Z	Standby
L	L	Write	High Z	Active
L	H	Read	DO	Active

FIGURE 4. Read cycle, waveform - Continued.

Device type 08



Device type 09



$\overline{CE}$	$\overline{WE}$	Mode	Output	Power
H	X	Not selected	High Z	Standby
L	L	Write	High Z	Active
L	H	Read	DO	Active

FIGURE 4. Write cycle, waveform - Continued.

TABLE II. Electrical test requirements. 1/ 2/ 3/

MIL-STD-883 test requirements	Subgroups (in accordance with method 5005, table I)
Interim electrical parameters (method 5004)	1, 7
Final electrical test parameters (method 5004)	1 4/, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3, or 1, 7, 9

1/ TELQX, TEHQZ, TWHQX, and TWLQZ, if not tested, shall be guaranteed to meet or exceed the conditions and limits specified in table I herein.
2/ Subgroups 10 and 11, if not tested, shall be guaranteed to meet or exceed the conditions and limits specified in table I herein.
3/ Individual test, conditions, and limits required in each group A subgroups shall be as shown in table I of this drawing.
4/ PDA applies to subgroup 1.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for original equipment manufacturer application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.5 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444, or telephone (513) 296-5377.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.

STANDARDIZED MILITARY DRAWING SOURCE APPROVAL BULLETIN

DATE: 93-10-12

Approved sources of supply for SMD 81024 are listed below for immediate acquisition only and shall be added to MIL-BUL-103 during the next revision. MIL-BUL-103 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DESC-EC. This bulletin is superseded by the next dated revision of MIL-BUL-103.

Standardized military drawing PIN	Vendor CAGE number	Vendor similar PIN 1/	Replacement military specification part number
8102401VX 2/	34371	HM1-6504S-8	M38510/24501BVX
8102401XX	3/	HM4-6504S-8	M38510/24501BXX
8102402VX 2/	34371	HM1-6514S-8	M38510/24502BVX
8102402XX	3/	HM4-6514S-8	M38510/24502BXX
8102403VX	34371	HM1-6504B-8	
8102403XX	3/	HM4-6504B-8	
8102404VX	34371	HM1-6514B-8	
8102404XX	3/	HM4-6514B-8	
8102405VX	34371	HM1-6504-8	
8102405XX	3/	HM4-6504-8	
8102406VX	34371	HM1-6514-8	
8102406XX	3/	HM4-6514-8	

Standardized military drawing PIN	Vendor CAGE number	Vendor similar PIN 1/	Replacement military specification part number
8102407YX	3/	5403004	
8102408VX	61203	3611143-1002	
8102409VX	61203	3611150-1002	

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

2/ Inactive for new design for the V case outline only. Use applicable QPL M38510 device.

3/ No available source.

Vendor CAGE number	Vendor name and address
34371	Harris Semiconductor P. O. Box 883 Melbourne, FL 32901
61203	Allied Signal Aerospace Company Microelectronic Center 9140 Old Annapolis Road Columbia, MD 21045