



**Document Title**  
4Bank x 1M x 16bits Synchronous DRAM

**Revision History**

Revision No.	History	Draft Date	Remark
0.1	Initial Draft	FEBRUARY 2004	Preliminary



**Preliminary**  
**HY5V66D(L)F(P) Series**  
**4Banks x 1M x 16bits Synchronous DRAM**

**DESCRIPTION**

The Hynix HY5V66D(L)F(P) series is a 67,108,864bit CMOS Synchronous DRAM, ideally suited for the memory applications which require wide data I/O and high bandwidth. HY5V66DF6 is organized as 4banks of 1,048,576x16.

HY5V66D(L)F(P) is offering fully synchronous operation referenced to a positive edge of the clock. All inputs and outputs are synchronized with the rising edge of the clock input. The data paths are internally pipelined to achieve very high bandwidth. All input and output voltage levels are compatible with LVTTTL.

Programmable options include the length of pipeline (Read latency of 2 or 3), the number of consecutive read or write cycles initiated by a single control command (Burst length of 1,2,4,8 or full page), and the burst count sequence(sequential or interleave). A burst of read or write cycles in progress can be terminated by a burst terminate command or can be interrupted and replaced by a new burst read or write command on any cycle. (This pipelined design is not restricted by a '2N' rule)

**FEATURES**

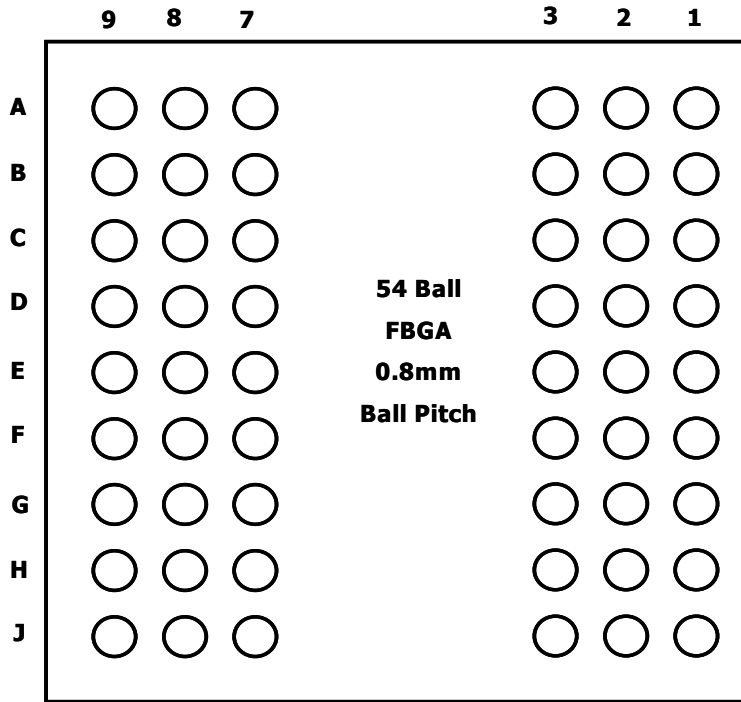
- Voltage : VDD, VDDQ 3.3V supply voltage
- All device pins are compatible with LVTTTL interface
- 54Ball FBGA
- All inputs and outputs referenced to positive edge of system clock
- Data mask function by UDQM, LDQM
- Internal four banks operation
- Auto refresh and self refresh
- 4096 Refresh cycles / 64ms
- Programmable Burst Length and Burst Type
  - 1, 2, 4, 8 or full page for Sequential Burst
  - 1, 2, 4 or 8 for Interleave Burst
- Programmable  $\overline{\text{CAS}}$  Latency ; 2, 3 Clocks
- Burst Read Single Write operation

**ORDERING INFORMATION**

Part No.	Clock Frequency	CAS Latency	Organization	Interface	Power	Package
HY5V66DF-K	133MHz	2	4Banks x 1Mbits x16	LVTTTL	Normal	54Ball FBGA, Lead
HY5V66DF-H	133MHz	3				
HY5V66DF-P	100MHz	2				
HY5V66DF-S	100MHz	3				
HY5V66DFP-K	133MHz	2				
HY5V66DFP-H	133MHz	3				
HY5V66DFP-P	100MHz	2			Low Power	54Ball FBGA, Lead Free
HY5V66DFP-S	100MHz	3				
HY5V66DLF-K	133MHz	2				
HY5V66DLF-H	133MHz	3				
HY5V66DLF-P	100MHz	2				
HY5V66DLF-S	100MHz	3				
HY5V66DLFP-K	133MHz	2			54Ball FBGA, Lead	
HY5V66DLFP-H	133MHz	3				
HY5V66DLFP-P	100MHz	2				
HY5V66DLFP-S	100MHz	3				
						54Ball FBGA, Lead Free

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### BALL ASSIGNMENTS



**<Bottom View>**

1	2	3	A	7	8	9
VSS	DQ15	VSSQ	A	VDDQ	DQ0	VDD
DQ14	DQ13	VDDQ	B	VSSQ	DQ2	DQ1
DQ12	DQ11	VSSQ	C	VDDQ	DQ4	DQ3
DQ10	DQ9	VDDQ	D	VSSQ	DQ6	DQ5
DQ8	NC	VSS	E	VDD	LDQM	DQ7
UDQM	CLK	CKE	F	/CAS	/RAS	/WE
NC	A11	A9	G	BA0	BA1	/CS
A8	A7	A6	H	A0	A1	A10
VSS	A5	A4	J	A3	A2	VDD

**< Top View >**



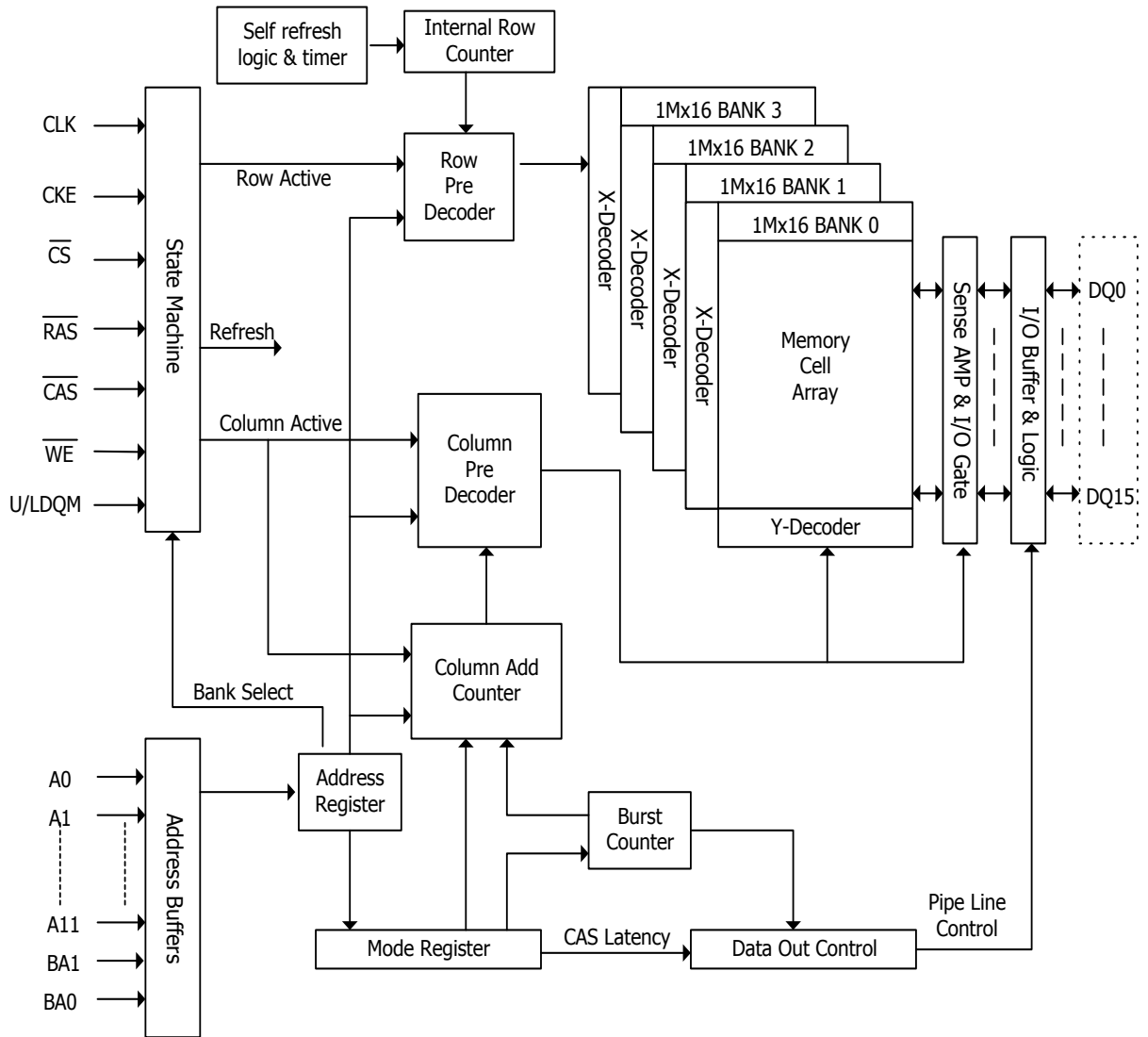
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### BALL DESCRIPTION

Ball Out	SYMBOL	TYPE	DESCRIPTION
F2	CLK	INPUT	Clock : The system clock input. All other inputs are registered to the SDRAM on the rising edge of CLK
F3	CKE	INPUT	Clock Enable : Controls internal clock signal and when deactivated, the SDRAM will be one of the states among (deep) power down, suspend or self refresh
G9	$\overline{CS}$	INPUT	Chip Select : Enables or disables all inputs except CLK, CKE, UDQM and LDQM
G7,G8	BA0, BA1	INPUT	Bank Address : Selects bank to be activated during $\overline{RAS}$ activity Selects bank to be read/written during $\overline{CAS}$ activity
H7, H8, J8, J7, J3, J2, H3, H2, H1, G3, H9, G2	A0 ~ A11	INPUT	Row Address : RA0 ~ RA11, Column Address : CA0 ~ CA7 Auto-precharge flag : A10
F8, F7, F9	$\overline{RAS}$ , $\overline{CAS}$ , $\overline{WE}$	INPUT	Command Inputs : $\overline{RAS}$ , $\overline{CAS}$ and $\overline{WE}$ define the operation Refer function truth table for details
F1, E8	UDQM, LDQM	INPUT	Data Mask : Controls output buffers in read mode and masks input data in write mode
A8, B9, B8, C9, C8, D9, D8, E9, E1, D2, D1, C2, C1, B2, B1, A2	DQ0 ~ DQ15	I/O	Data Input/Output : Multiplexed data input/output pin
A9, E7, J9, A1, E3, J1	VDD/VSS	SUPPLY	Power supply for internal circuits
A7, B3, C7, D3, A3, B7, C3, D7	VDDQ/VSSQ	SUPPLY	Power supply for output buffers
E2, G1	NC	-	No connection



**FUNCTIONAL BLOCK DIAGRAM**  
1Mbit x 4banks x 16 I/O Low Power Synchronous DRAM



## BASIC FUNCTIONAL DESCRIPTION

### Mode Register

BA1	BA0	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	0	0	OP Code	0	0	CAS Latency			BT	Burst Length		

#### OP Code

A9	Write Mode
0	Burst Read and Burst Write
1	Burst Read and Single Write

#### Burst Type

A3	Burst Type
0	Sequential
1	Interleave

#### CAS Latency

A6	A5	A4	CAS Latency
0	0	0	Reserved
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

#### Burst Length

A2	A1	A0	Burst Length	
			A3 = 0	A3 = 1
0	0	0	1	1
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	Reserved	Reserved
1	0	1	Reserved	Reserved
1	1	0	Reserved	Reserved
1	1	1	Full Page	Reserved



## ABSOLUTE MAXIMUM RATING

Parameter	Symbol	Rating	Unit
Ambient Temperature	TA	0 ~ 70	°C
Storage Temperature	TSTG	-55 ~ 125	°C
Voltage on Any Pin relative to VSS	VIN, VOUT	-1.0 ~ 4.6	V
Voltage on VDD relative to VSS	VDD	-1.0 ~ 4.6	V
Voltage on VDDQ relative to VSS	VDDQ	-1.0 ~ 4.6	V
Short Circuit Output Current	IOS	50	mA
Power Dissipation	PD	1	W
Soldering Temperature · Time	TSOLDER	260 · 10	°C · Sec

## DC OPERATING CONDITION (TA= 0 to 70°C )

Parameter	Symbol	Min	Typ	Max	Unit	Note
Power Supply Voltage	VDD, VDDQ	3.0	3.3	3.6	V	1
Input High Voltage	VIH	2.0	3.3	VDDQ+0.3	V	1, 2
Input Low Voltage	VIL	-0.3	-	0.8	V	1, 3

Note : 1. All voltages are referenced to VSS = 0V  
2. VIH(max) is acceptable 5.6V AC pulse width with <=3ns of duration.  
3. VIL(min) is acceptable -2.0V AC pulse width with <=3ns of duration

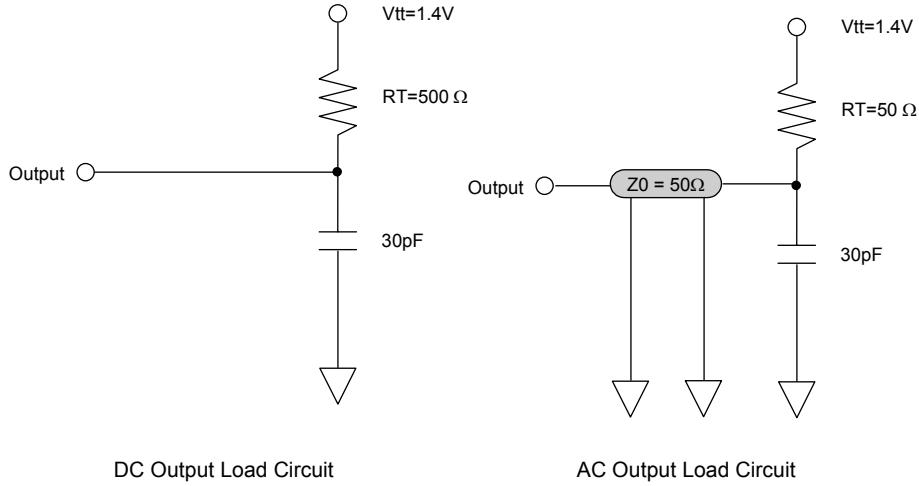
## AC OPERATING TEST CONDITION (TA= 0 to 70 °C, VDD=3.3±0.3V, VSS=0V)

Parameter	Symbol	Value	Unit	Note
AC Input High/Low Level Voltage	VIH / VIL	2.4/0.4	V	
Input Timing Measurement Reference Level Voltage	Vtrip	1.4	V	
Input Rise/Fall Time	tR / tF	1	ns	
Output Timing Measurement Reference Level Voltage	Voutref	1.4	V	
Output Load Capacitance for Access Time Measurement	CL	50	pF	1

## CAPACITANCE (TA= 0 to 70 °C, f=1MHz, VDD=3.3V)

Parameter	Pin	Symbol	Min	Max	Unit
Input capacitance	CLK	CI1	2.5	4	pF
	A0 ~ A11, BA0, BA1, CKE, $\overline{CS}$ , $\overline{RAS}$ , $\overline{CAS}$ , WE, LDQM, UDQM	CI2	2.5	5	pF
Data input / output capacitance	DQ0 ~ DQ15	CI/O	4	6.5	pF

Note 1.



**DC CHARACTERISTICS I** (TA= 0 to 70°C)

Parameter	Symbol	Min	Max	Unit	Note
Input Leakage Current	ILI	-1	1	uA	1
Output Leakage Current	ILO	-1	1	uA	2
Output High Voltage	VOH	2.4	-	V	I <sub>OH</sub> = -2mA
Output Low Voltage	VOL	-	0.4	V	I <sub>OL</sub> = +2mA

Note :

1. VIN = 0 to 3.3V, All other balls are not tested under VIN =0V
2. DOUT is disabled, VOUT=0 to 3.6





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**DC CHARACTERISTICS II** (TA= 0 to 70°C)

Parameter	Symbol	Test Condition	Speed				Unit	Note
			-K	-H	-P	-S		
Operating Current	IDD1	Burst length=1, One bank active tRC ≥ tRC(min), IOL=0mA	85		80		mA	1
Precharge Standby Current in Power Down Mode	IDD2P	CKE ≤ VIL(max), tCK = 15ns	2				mA	
	IDD2PS	CKE ≤ VIL(max), tCK = ∞	2				mA	
Precharge Standby Current in Non Power Down Mode	IDD2N	CKE ≥ VIH(min), $\overline{CS}$ ≥ VIH(min), tCK = 15ns Input signals are changed one time during 2clks. All other pins ≥ VDD-0.2V or ≤ 0.2V	15				mA	
	IDD2NS	CKE ≥ VIH(min), tCK = ∞ Input signals are stable.	12					
Active Standby Current in Power Down Mode	IDD3P	CKE ≤ VIL(max), tCK = 15ns	6				mA	
	IDD3PS	CKE ≤ VIL(max), tCK = ∞	5					
Active Standby Current in Non Power Down Mode	IDD3N	CKE ≥ VIH(min), $\overline{CS}$ ≥ VIH(min), tCK = 15ns Input signals are changed one time during 2clks. All other pins ≥ VDD-0.2V or ≤ 0.2V	30				mA	
	IDD3NS	CKE ≥ VIH(min), tCK = ∞ Input signals are stable.	20					
Burst Mode Operating Cur- rent	IDD4	tCK ≥ tCK(min), IOL=0mA All banks active	CL=3	150	120		mA	1
			CL=2	120				
Auto Refresh Current	IDD5	tRC ≥ tRC(min), All banks active	160				mA	2
Self Refresh Current	IDD6	CKE ≤ 0.2V	Normal	1		mA		
			Low power	400		uA		

**Note :** 1. IDD1 and IDD4 depend on output loading and cycle rates. Specified values are measured with the output open  
 2. Min. of tRRC (Refresh RAS cycle time) is shown at AC CHARACTERISTICS II



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**AC CHARACTERISTICS I** (AC operating conditions unless otherwise noted)

Parameter		Symbol	K		H		P		S		Unit	Note
			Min	Max	Min	Max	Min	Max	Min	Max		
System Clock Cycle Time	CAS Latency=3	tCK3	7.5	1000	7.5	1000	10	1000	10	1000	ns	
	CAS Latency=2	tCK2	7.5		10		10		12		ns	
Clock High Pulse Width		tCHW	2.5	-	2.5	-	3.0	-	3.0	-	ns	1
Clock Low Pulse Width		tCLW	2.5	-	2.5	-	3.0	-	3.0	-	ns	1
Access Time From Clock	CAS Latency=3	tAC3	-	5.4	-	5.4	-	6.0	-	6.0	ns	2
	CAS Latency=2	tAC2	-	5.4	-	6.0	-	6.0	-	8.0	ns	
Data-out Hold Time		tOH	2.0	-	2.0	-	2.0	-	2.0	-	ns	
Data-Input Setup Time		tDS	1.5	-	1.5	-	2.0	-	2.0	-	ns	1
Data-Input Hold Time		tDH	0.8	-	0.8	-	1.0	-	1.0	-	ns	1
Address Setup Time		tAS	1.5	-	1.5	-	2.0	-	2.0	-	ns	1
Address Hold Time		tAH	0.8	-	0.8	-	1.0	-	1.0	-	ns	1
CKE Setup Time		tCKS	1.5	-	1.5	-	2.0	-	2.0	-	ns	1
CKE Hold Time		tCKH	0.8	-	0.8	-	1.0	-	1.0	-	ns	1
Command Setup Time		tCS	1.5	-	1.5	-	2.0	-	2.0	-	ns	1
Command Hold Time		tCH	0.8	-	0.8	-	1.0	-	1.0	-	ns	1
CLK to Data Output in Low-Z Time		tOLZ	1.5	-	1.5	-	1.0	-	2.0	-	ns	
CLK to Data Output in High-Z Time	CAS Latency=3	tOHZ3	-	5.4	-	5.4	-	6.0	-	6.0	ns	
	CAS Latency=2	tOHZ2	-	5.4	-	5.4	-	6.0	-	6.0	ns	

Note :

1. Assume  $t_R / t_F$  (input rise and fall time) is 1ns. If  $t_R \& t_F > 1ns$ , then  $[(t_R+t_F)/2-1]ns$  should be added to the parameter.
2. Access time to be measured with input signals of 1V/ns edge rate, from 0.8V to 0.2V. If  $t_R > 1ns$ , then  $(t_R/2-0.5)ns$  should be added to the parameter.



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**AC CHARACTERISTICS II** (AC operating conditions unless otherwise noted)

Parameter		Symbol	K		H		P		S		Unit	Note
			Min	Max	Min	Max	Min	Max	Min	Max		
RAS Cycle Time	Operation	tRC	65	-	65	-	70	-	70	-	ns	
RAS Cycle Time	Auto Refresh	tRRC	65	-	65	-	70	-	70	-	ns	
RAS to CAS Delay		tRCD	15	-	20	-	20	-	20	-	ns	
RAS Active Time		tRAS	45	120K	45	120K	50	120K	50	120K	ns	
RAS Precharge Time		tRP	15	-	20	-	20	-	20	-	ns	
RAS to RAS Bank Active Delay		tRRD	15	-	15	-	20	-	20	-	ns	
CAS to CAS Delay		tCCD	1	-	1	-	1	-	1	-	CLK	
Write Command to Data-In Delay		tWTL	0	-	0	-	0	-	0	-	CLK	
Data-in to Precharge Command		tDPL	1	-	1	-	1	-	1	-	CLK	
Data-In to Active Command		tDAL	tDPL + tRP									
DQM to Data-Out Hi-Z		tDQZ	2	-	2	-	2	-	2	-	CLK	
DQM to Data-In Mask		tDQM	0	-	0	-	0	-	0	-	CLK	
MRS to New Command		tMRD	1	-	1	-	1	-	1	-	CLK	
Precharge to Data Output High-Z	CAS Latency=3	tPROZ3	3	-	3	-	3	-	3	-	CLK	
	CAS Latency=2	tPROZ2	2	-	2	-	2	-	2	-	CLK	
Power Down Exit Time		tDPE	1	-	1	-	1	-	1	-	CLK	
Self Refresh Exit Time		tSRE	1	-	1	-	1	-	1	-	CLK	1
Refresh Time		tREF	-	64	-	64	-	64	-	64	ms	

Note : 1. A new command can be given tRRC after self refresh exit.



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**COMMAND TRUTH TABLE**

Command	CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	ADDR	A10/AP	BA	Note	
Mode Register Set	H	X	L	L	L	L	X	OP code				
No Operation	H	X	H	X	X	X	X	X				
			L	H	H	H						
Bank Active	H	X	L	L	H	H	X	RA		V		
Read	H	X	L	H	L	H	X	CA	L	V		
Read with Autoprecharge									H			
Write	H	X	L	H	L	L	X	CA	L	V		
Write with Autoprecharge									H			
Precharge All Banks	H	X	L	L	H	L	X	X	H	X		
Precharge selected Bank									L	V		
Burst Stop	H	X	L	H	H	L	X	X				
DQM	H	X					V	X				
Auto Refresh	H	H	L	L	L	H	X	X				
Burst-Read-Single-WRITE	H	X	L	L	L	L	X	A9 ball High (Other balls OP code)			MRS Mode	
Self Refresh <sup>1</sup>	Entry	H	L	L	L	L	H	X	X			
	Exit	L	H	H	X	X	X	X				
L				H	H	H						
Precharge power down	Entry	H	L	H	X	X	X	X	X			
				L	H	H	H					
	Exit	L	H	H	X	X	X	X				
				L	H	H	H					
Clock Suspend	Entry	H	L	H	X	X	X	X	X			
				L	V	V	V					
	Exit	L	H	X				X				

**PACKAGE INFORMATION**

**54 Ball 0.8mm pitch 8mm FBGA**

