IS24C128B

2-WIRE (I^2C)

128K-bit

SERIAL EEPROM

TABLE OF CONTENTS

IS24C128B

128K-bit
2-WIRE SERIAL CMOS EEPROM

PRELIMINARY

FEATURES

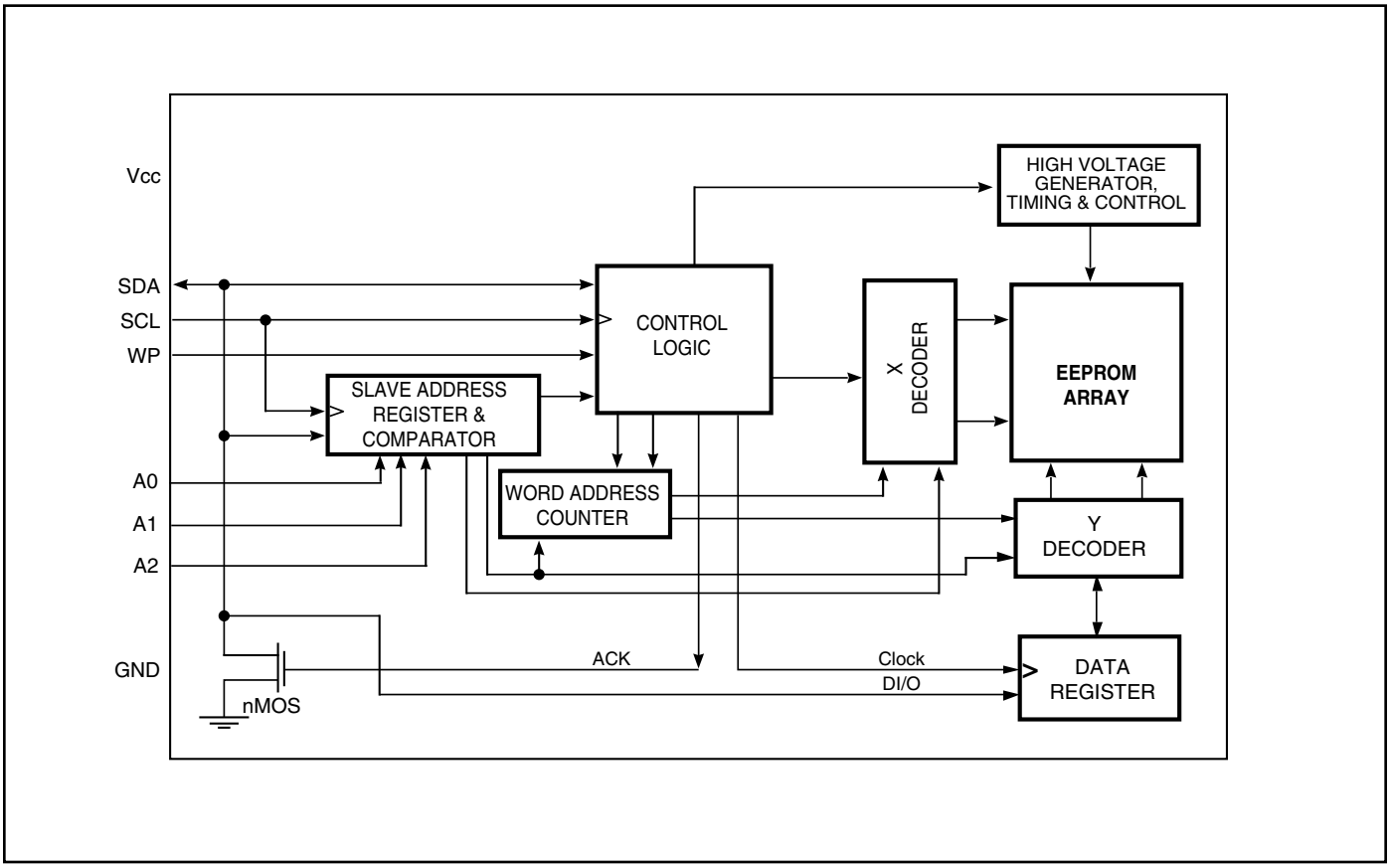
- Two-Wire Serial Interface, I²C™ compatible
  - Bi-directional data transfer protocol
- Wide Voltage Operation
  - Vcc = 1.8V to 5.5V
- 400 KHz (1.8V) and 1 MHz (5.0V) compatibility
- 128K-bit memory
- Low Power CMOS Technology
  - Active Current less than 3 mA (1.8V)
  - Standby Current less than 15 µA (1.8V)
- Hardware Data Protection
  - Write Protect Pin
- Sequential Read Feature
- Filtered Inputs for Noise Suppression
- Self time write cycle with auto clear
  - 5 ms @ 1.8V
- Memory Organization:
  - 16Kx8 (256 pages of 64 bytes)
- 64-Byte Page Write Buffer
- High Reliability
  - Endurance: 1,000,000 Cycles
  - Data Retention: 40 Years
- Industrial temperature range
- Packages: SOIC/SOP (JEDEC), TSSOP and PDIP

DESCRIPTION

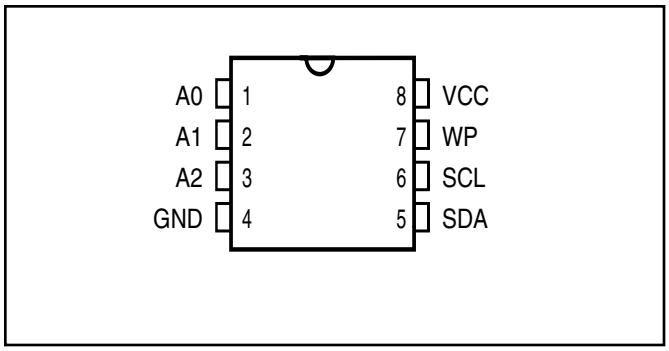
The IS24C128B is an electrically erasable PROM device that uses the standard 2-wire interface for communications. The IS24C128B is 128K-bit (16Kx8). These EEPROM are offered in a wide operating voltage range of 1.8V to 5.5V to be compatible with most application voltages. ISSI designed the IS24C128B to be an efficient 2-wire EEPROM solution. The devices are offered in lead free, RoHS, halogen free or Green. The available package types are 8-pin SOIC (JEDEC), TSSOP and PDIP.

The IS24C128B maintains compatibility with the popular 2-wire bus protocol, so it is easy to design into applications implementing this bus type. The simple bus consists of the Serial Clock wire (SCL) and the Serial Data wire (SDA). Using the bus, a Master device such as a microcontroller is usually connected to one or more Slave devices such as the IS24C128B. The bit stream over the SDA line includes a series of bytes, which identifies a particular Slave device, an instruction, an address within that Slave device, and a series of data, if appropriate. The IS24C128B has a Write Protect pin (WP) to allow blocking of any write instruction transmitted over the bus.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION
8-Pin SOIC, TSSOP, PDIP



PIN DESCRIPTIONS

A0-A2	Address Inputs
SDA	Serial Address/Data I/O
SCL	Serial Clock Input
WP	Write Protect Input
Vcc	Power Supply
GND	Ground

SCL

This input clock pin is used to synchronize the data transfer to and from the device.

SDA

The SDA is a Bi-directional pin used to transfer addresses and data into and out of the device. The SDA pin is an open drain output and can be wire Or'ed with other open drain or open collector outputs. The SDA bus a pullup resistor to Vcc.

A0, A1, A2

The A0, A1, and A2 are the device address inputs that are hardwired or left not connected for hardware compatibility with the IS24C32A/64A. When pins are hardwired, as many as eight 128K devices may be addressed on a single bus system. When the pins are not hardwired, the default values of A0, A1, and A2 are zero.

WP

WP is the Write Protect pin. If the WP pin is tied to Vcc the entire array becomes Write Protected (Read only). When WP is tied to GND or left floating, normal read/write operations are allowed to the device.

DEVICE OPERATION

The IS24C128B features a serial communication and supports a bi-directional 2-wire bus transmission protocol called I²C™.

2-WIRE BUS

The two-wire bus is defined as a Serial Data line (SDA), and a Serial Clock line (SCL). The protocol defines any device that sends data onto the SDA bus as a transmitter, and the receiving devices as receivers. The bus is controlled by Master device which generates the SCL, controls the bus access and generates the Stop and Start conditions. The IS24C128B is the Slave device on the bus.

The Bus Protocol:

– Data transfer may be initiated only when the bus is not busy

– During a data transfer, the SDA line must remain stable whenever the SCL line is high. Any changes in the data line while the SCL line is high will be interpreted as a Start or Stop condition.

The state of the SDA line represents valid data after a Start condition. The SDA line must be stable for the duration of the High period of the clock signal. The data on the SDA line may be changed during the Low period of the clock signal. There is one clock pulse per bit of data. Each data transfer is initiated with a Start condition and terminated with a Stop condition.

Start Condition

The Start condition precedes all commands to the device and is defined as a High to Low transition of SDA when SCL is High. The IS24C128B monitors the SDA and SCL lines and will not respond until the Start condition is met.

Stop Condition

The Stop condition is defined as a Low to High transition of SDA when SCL is High. All operations must end with a Stop condition.

Acknowledge (ACK)

After a successful data transfer, each receiving device is required to generate an ACK. The Acknowledging device pulls down the SDA line.

Reset

The IS24C128B contains a reset function in case the 2-wire bus transmission is accidentally interrupted (eg. a power loss), or needs to be terminated mid-stream. The reset is caused when the Master device creates a Start condition. To do this, it may be necessary for the Master device to monitor the SDA line while cycling the SCL up to nine times. (For each clock signal transition to High, the Master checks for a High level on SDA.)

Standby Mode

Power consumption is reduced in standby mode. The IS24C128B will enter standby mode: a) At Power-up, and remain in it until SCL or SDA toggles; b) Following the Stop signal if no write operation is initiated; or c) Following any internal write operation

DEVICE ADDRESSING

The Master begins a transmission by sending a Start condition. The Master then sends the address of the particular Slave devices it is requesting. The Slave device (Fig. 5) address is 8 bits.

The four most significant bits of the Slave device address are fixed as 1010 for the IS24C128B.

This device has three address bits (A2, A1, and A0), which allows up to eight IS24C128B devices to share the 2-wire bus. Upon receiving the Slave address, the device compares the three address bits with the hardwired A2, A1, and A0 input pins to determine if it is the appropriate Slave.

The last bit of the Slave address specifies whether a Read or Write operation is to be performed. When this bit is set to 1, a Read operation is selected, and when set to 0, a Write operation is selected.

After the Master transmits the Start condition and Slave address byte (Fig. 5), the appropriate 2-wire Slave (eg. IS24C128B) will respond with ACK on the SDA line. The Slave will pull down the SDA on the ninth clock cycle, signaling that it received the eight bits of data. The selected IS24C128B then prepares for a Read or Write operation by monitoring the bus.

WRITE OPERATION

Byte Write

In the Byte Write mode, the Master device sends the Start condition and the Slave address information (with the R/$\overline{W}$ set to Zero) to the Slave device. After the Slave generates an ACK, the Master sends the two byte address that are to be written into the address pointer of the IS24C128B. After receiving another ACK from the Slave, the Master device transmits the data byte to be written into the address memory location. The IS24C128B acknowledges once more and the Master generates the Stop condition, at which time the device begins its internal programming cycle. While this internal cycle is in progress, the device will not respond to any request from the Master device.

Page Write

The IS24C128B is capable of 64-byte Page-Write operation. A Page-Write is initiated in the same manner as a Byte Write, but instead of terminating the internal Write cycle after the first data word is transferred, the Master device can transmit up to 63 more bytes. After the receipt of each data word, the IS24C128B responds immediately with an ACK on SDA line, and the six lower order data word address bits are internally incremented by one, while the higher order bits of the data word address remain constant. If a byte address is incremented from the last byte of a page, it returns to the first byte of that page. If the Master device should transmit more than 64 words prior to issuing the Stop condition, the address counter will “roll over,” and the previously written data will be overwritten. Once all 64 bytes are received and the Stop condition has been sent by the Master, the internal programming cycle begins. At this point, all received data is written to the IS24C128B in a single Write cycle. All inputs are disabled until completion of the internal Write cycle.

Acknowledge (ACK) Polling

The disabling of the inputs can be used to take advantage of the typical Write cycle time. Once the Stop condition is issued to indicate the end of the host's Write operation, the IS24C128B initiates the internal Write cycle. ACK polling can be initiated immediately. This involves issuing the Start condition followed by the Slave address for a Write operation. If the IS24C128B is still busy with the Write operation, no ACK will be returned. If the IS24C128B has completed the Write operation, an ACK will be returned and the host can then proceed with the next Read or Write operation.

READ OPERATION

Read operations are initiated in the same manner as Write operations, except that the (R/$\overline{W}$) bit of the Slave address is set to “1”. There are three Read operation options: current address read, random address read, and sequential read.

Current Address Read

The IS24C128B contains an internal address counter which maintains the address of the last byte accessed, incremented by one. For example, if the previous operation is either a Read or Write operation addressed to the address location n, the internal address counter would increment to address location n+1. When the IS24C128B receives the Slave Device Addressing Byte with a Read operation (R/$\overline{W}$ bit set to “1”), it will respond an ACK and transmit the 8-bit data word stored at address location n+1. The Master should not acknowledge the transfer but should generate a Stop condition so the IS24C128B discontinues transmission. If 'n' is the last byte of the memory, the data from location '0' will be transmitted. (Refer to Figure 8. Current Address Read Diagram.)

Random Address Read

Selective Read operations allow the Master device to select at random any memory location for a Read operation. The Master device first performs a 'dummy' Write operation by sending the Start condition, Slave address and word address of the location it wishes to read. After the IS24C128B acknowledges the word address, the Master device resends the Start condition and the Slave address, this time with the R/$\overline{W}$ bit set to one. The IS24C128B then responds with its ACK and sends the data requested. The Master device does not send an ACK but will generate a Stop condition. (Refer to Figure 9. Random Address Read Diagram.)

Sequential Read

Sequential Reads can be initiated as either a Current Address Read or Random Address Read. After the IS24C128B sends the initial byte sequence, the Master device now responds with an ACK indicating it requires additional data from the IS24C128B. The IS24C128B continues to output data for each ACK received. The Master device terminates the sequential Read operation by pulling SDA High (no ACK) indicating the last data word to be read, followed by a Stop condition.

The data output is sequential, with the data from address n followed by the data from address n+1, ... etc. The address counter increments by one automatically, allowing the entire memory contents to be serially read during sequential Read operation. When the memory address boundary of 16383 (depending on the device) is reached, the address counter “rolls over” to address 0, and the IS24C128B continues to output data for each ACK received. (Refer to Figure 10. Sequential Read Operation Starting with a Random Address Read Diagram.)

Figure 1. Typical System Bus Configuration

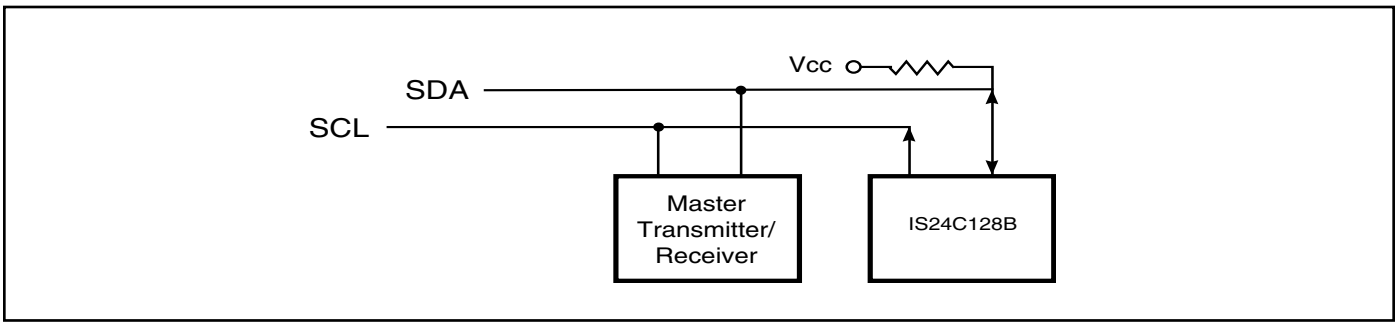


Figure 2. Output Acknowledge

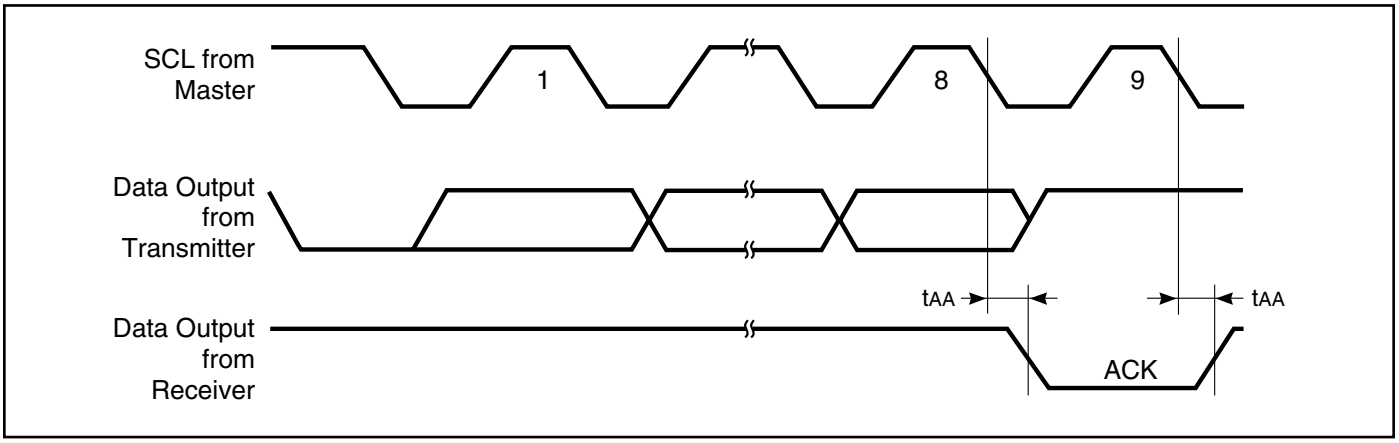


Figure 3. Start and Stop Conditions

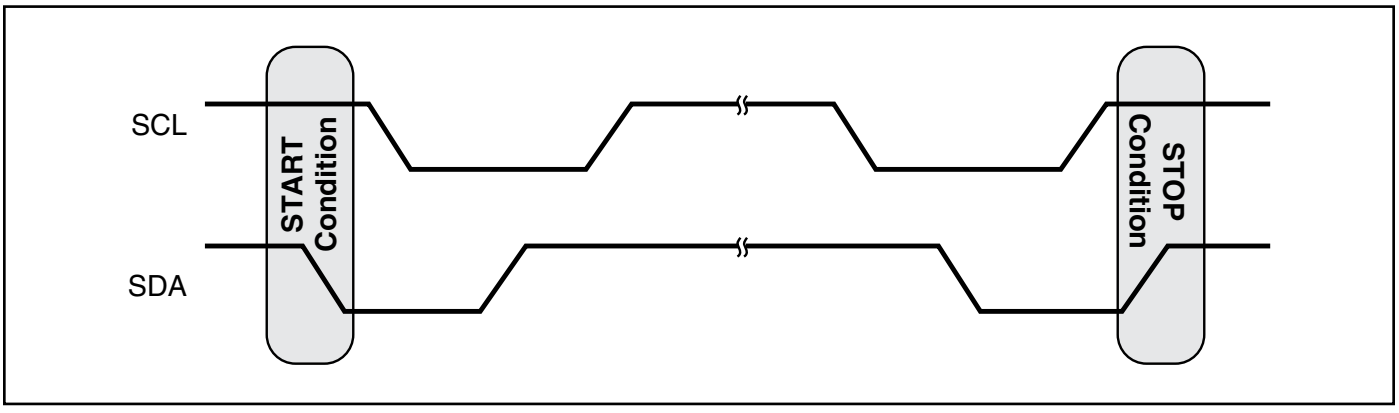


Figure 4. Data Validity Protocol

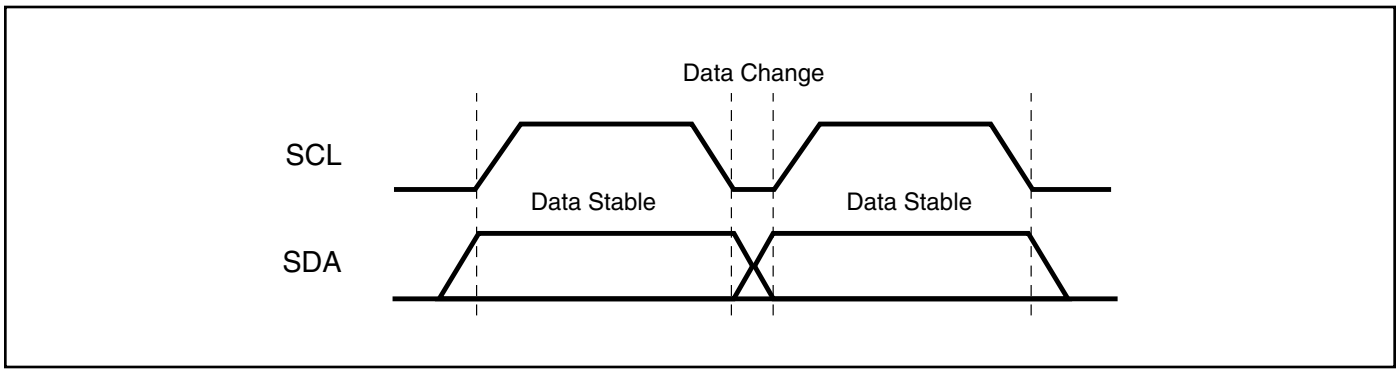


Figure 5. Slave Address

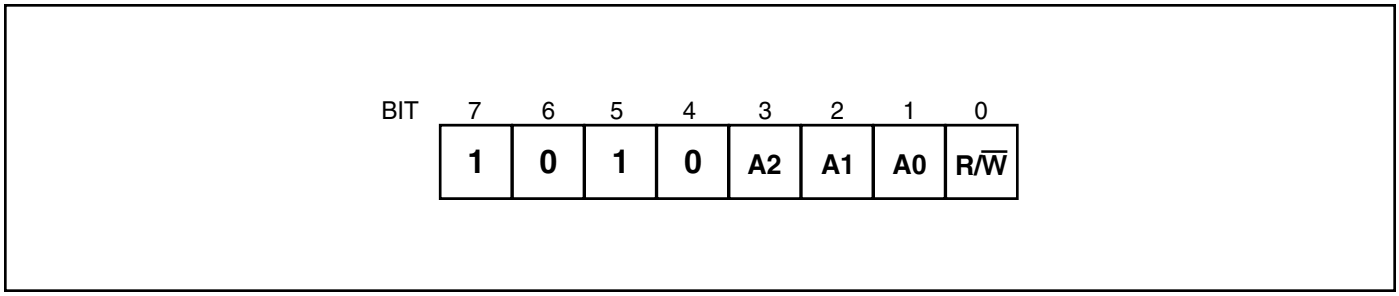


Figure 6. Byte Write

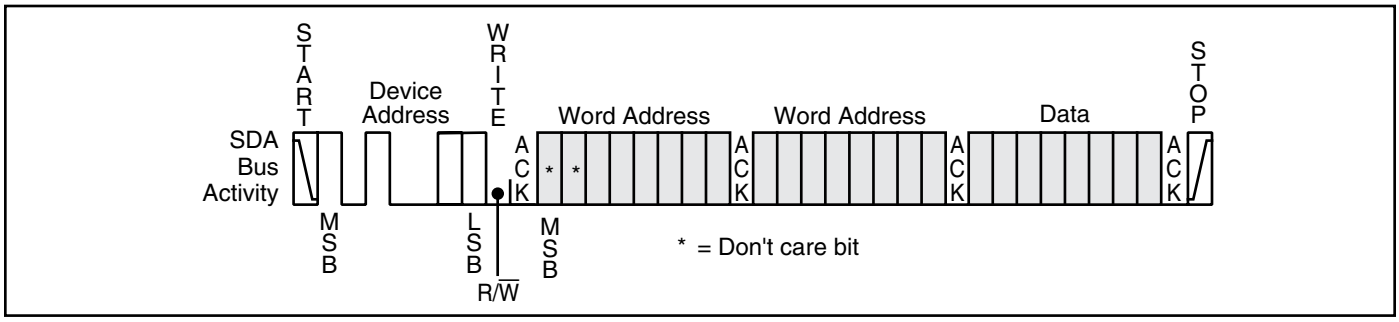


Figure 7. Page Write

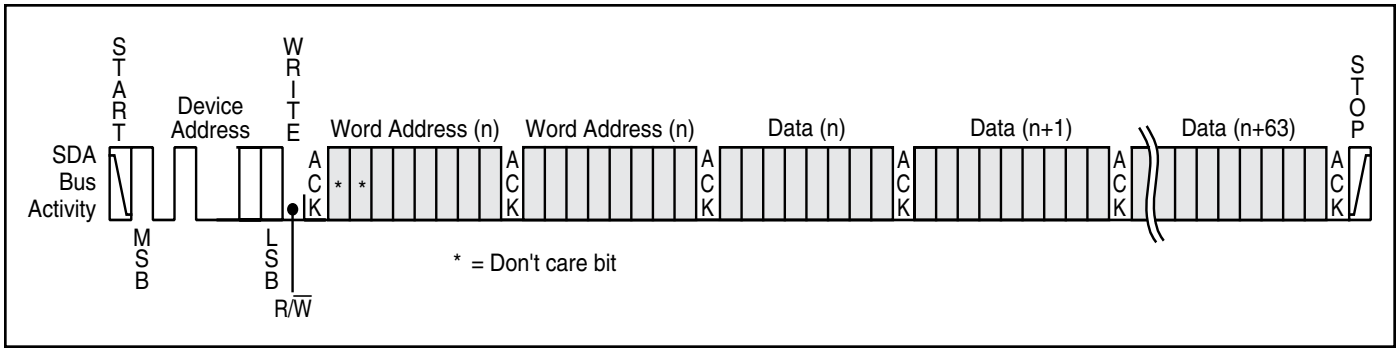


Figure 8. Current Address Read

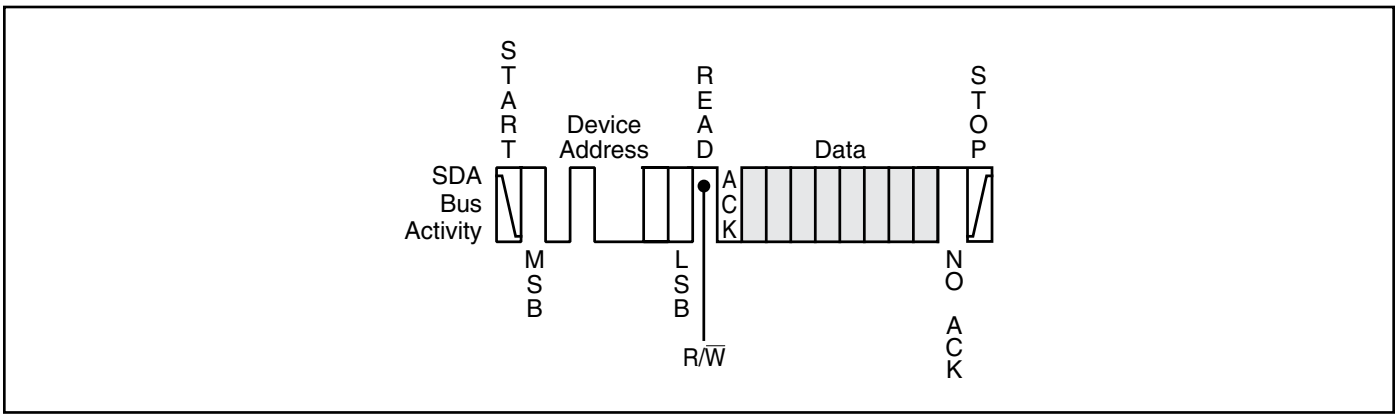


Figure 9. Random Address Read

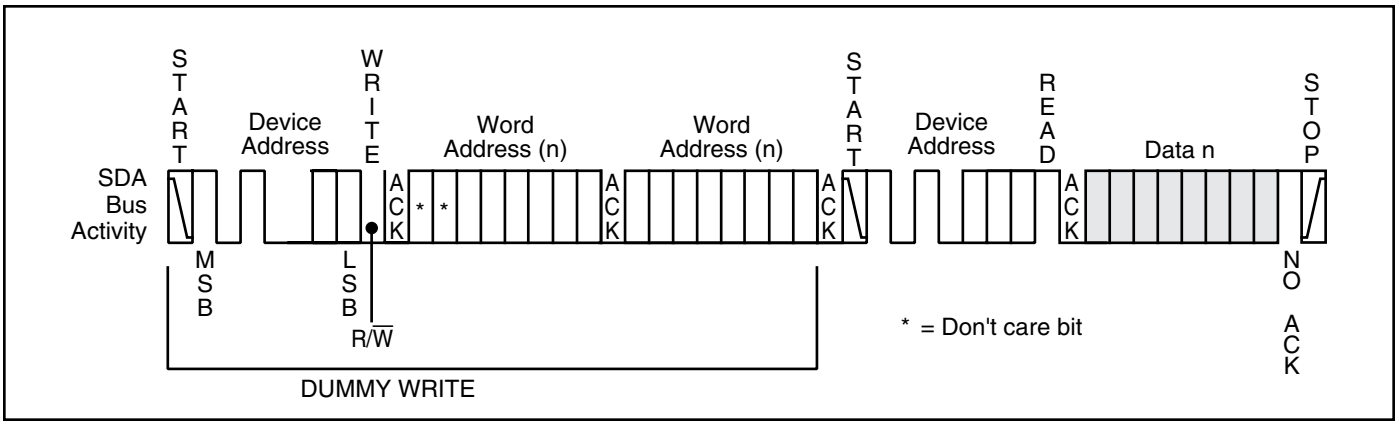


Figure 10. Sequential Read

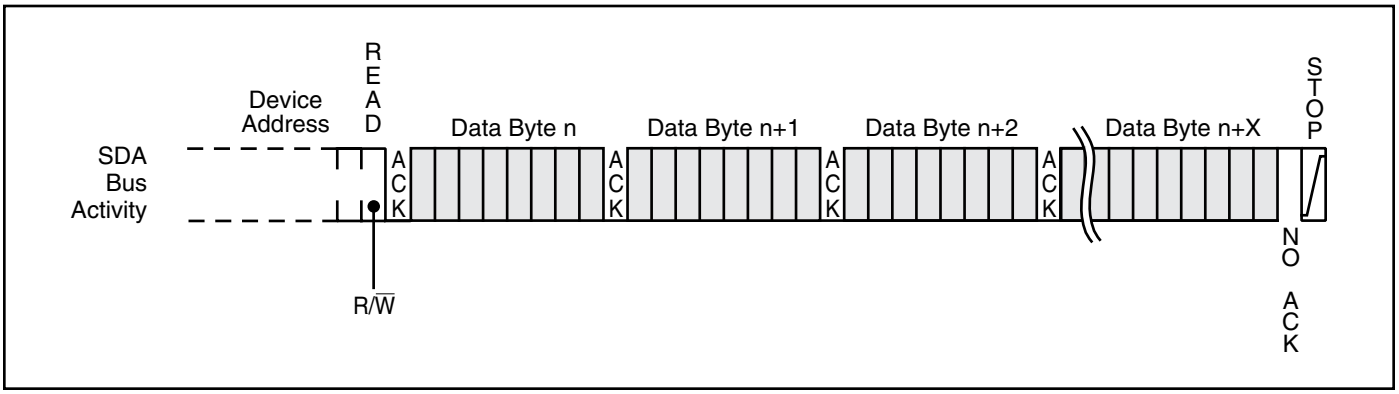
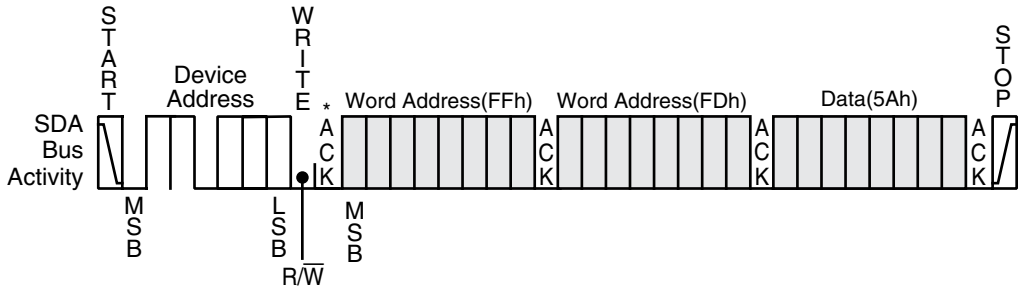
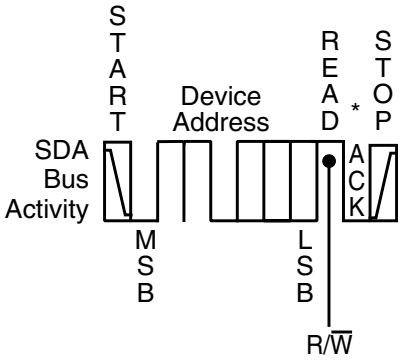


Figure 11 DEEP SLEEP ENTRY/EXIT INITIATION



* The slave does not provide an acknowledgement if the Deep Sleep Mode is enabled, and after stop, it begins to exit.

Figure 12 DEEP SLEEP VERIFICATION



* The slave does not provide an acknowledgement if the Deep Sleep Mode is already enabled. This command does not affect Deep Sleep.

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameter	Value	Unit
V_S	Supply Voltage	–0.5 to +6.5	V
V_P	Voltage on Any Pin	–0.5 to Vcc +0.5	V
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–65 to +150	°C
I_{OUT}	Output Current	5	mA

Notes:
1. Stresses violating the conditions listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only. Functional operation of the device outside these conditions or those indicated in the operational sections of this specification is not implied. Exposure to these conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS

Industrial (T_A = -40°C to +85°C)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
$V_{OL}1$	Output Low Voltage	V_{CC} = 1.8V, I_{OL} = 0.15 mA	—	0.2	V
$V_{OL}2$	Output Low Voltage	V_{CC} = 2.5V, I_{OL} = 2.1 mA	—	0.4	V
V_{IH}	Input High Voltage		V_{CC} x 0.7	V_{CC} + 0.5	V
V_{IL}	Input Low Voltage		–0.3	V_{CC} x 0.3	V
I_{LI}	Input Leakage Current	V_{IN} = V_{CC} max.	—	3	µA
I_{LO}	Output Leakage Current		—	3	µA

Notes: V_{IL} min and V_{IH} max are reference only and are not tested

POWER SUPPLY CHARACTERISTICS

Industrial (T_A = -40°C to +85°C)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
$I_{CC}1$	Operating Current	Read at 400 KHz (Vcc = 1.8V)	—	3.0	mA
$I_{CC}2$	Operating Current	Write at 400 KHz (Vcc = 1.8V)	—	3.0	mA
$I_{SB}1$	Standby Current	Vcc = 1.8V	—	15	µA
$I_{SB}2$	Standby Current	Vcc = 2.5V	—	20	µA
$I_{SB}3$	Standby Current	Vcc = 5.0V	—	25	µA

CAPACITANCE(1,2)

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

Notes:
1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1 MHz, Vcc = 5.0V.

AC ELECTRICAL CHARACTERISTICS

Industrial (T_A = -40°C to +85°C)

		1.8V ≤ Vcc < 2.5V		2.5V ≤ Vcc ≤ 5.5V[1]		
Symbol	**Parameter[2]**	**Min.**	**Max.**	**Min.**	**Max.**	**Unit**
f_{SCL}	SCL Clock Frequency	0	400	0	1000	KHz
T	Noise Suppression Time[1]	—	50	—	50	ns
t_{Low}	Clock Low Period	1.2	—	0.6	—	µs
t_{High}	Clock High Period	0.6	—	0.4	—	µs
t_{BUF}	Bus Free Time Before New Transmission[1]	1.2	—	0.5	—	µs
$t_{SU:STA}$	Start Condition Setup Time	0.6	—	0.25	—	µs
$t_{SU:STO}$	Stop Condition Setup Time	0.6	—	0.25	—	µs
$t_{HD:STA}$	Start Condition Hold Time	0.6	—	0.25	—	µs
$t_{HD:STO}$	Stop Condition Hold Time	0.6	—	0.25	—	µs
$t_{SU:DAT}$	Data In Setup Time	100	—	100	—	ns
$t_{HD:DAT}$	Data In Hold Time	0	—	0	—	ns
$t_{SU:WP}$	WP pin Setup Time	0.6	—	0.6	—	µs
$t_{HD:WP}$	WP pin Hold Time	1.2	—	1.2	—	µs
t_{DH}	Data Out Hold Time (SCL Low to SDA Data Out Change)	50	—	50	—	ns
t_{AA}	Clock to Output (SCL Low to SDA Data Out Valid)	50	900	50	400	ns
t_R	SCL and SDA Rise Time[1]	—	300	—	300	ns
t_F	SCL and SDA Fall Time[1]	—	300	—	100	ns
t_{WR}	Write Cycle Time	—	5	—	5	ms

Notes:
1. This parameter is characterized but not 100% tested.
2. The timing is referenced to half Vcc level.

AC WAVEFORMS

Figure 13. Bus Timing

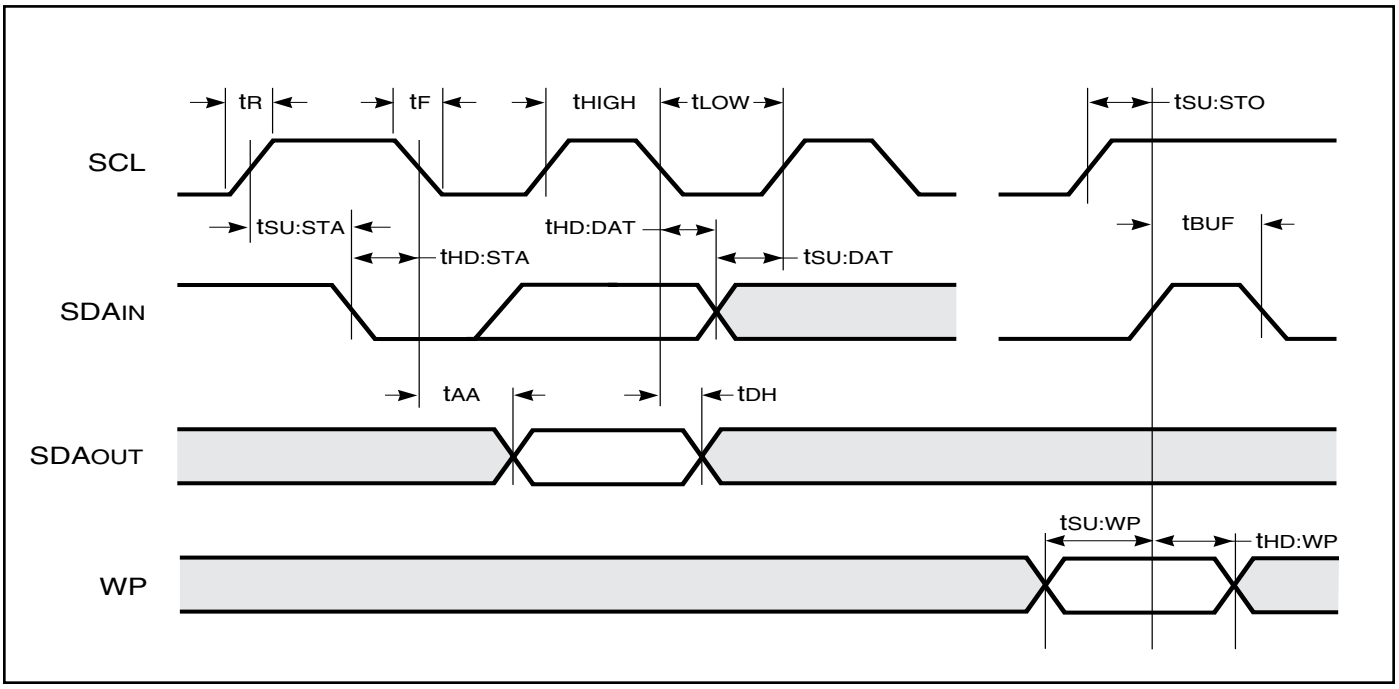
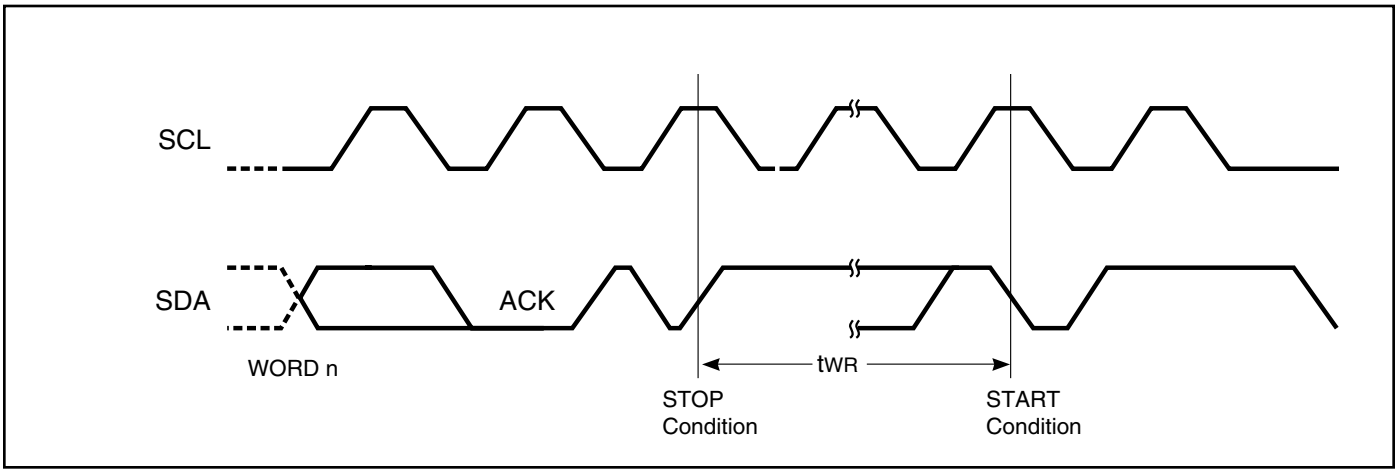


Figure 14. Write Cycle Timing



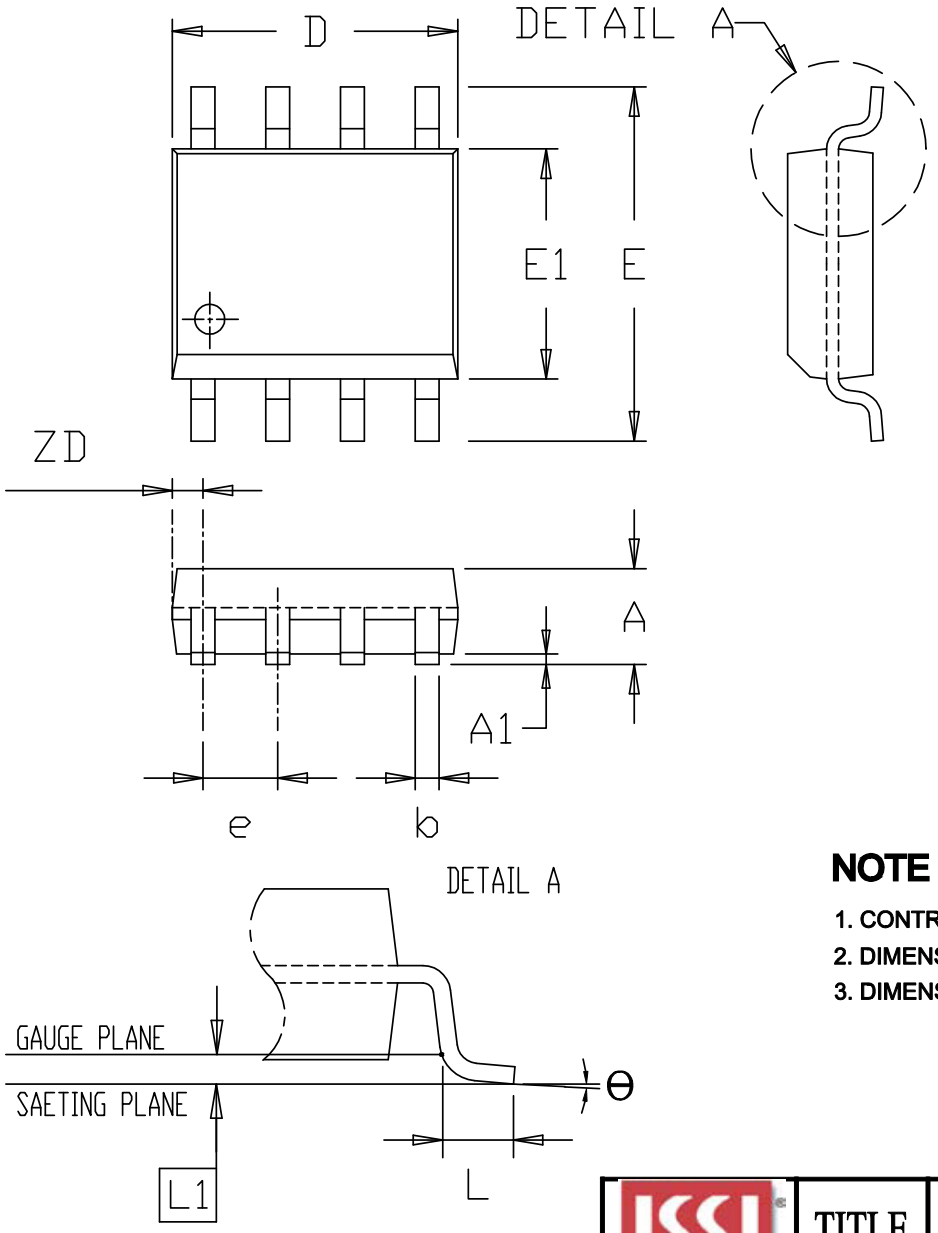
ORDERING INFORMATION:

Industrial Range: -40°C to +85°C, Lead-free*

Voltage Range	Part Number*	Package Type* (8-pin)
2.5V to 5.5V	IS24C128B-3GLI	150-mil SOIC (JEDEC)
	IS24C128B-3ZLI	3 x 4.4 mm TSSOP
1.8V to 5.5V	IS24C128B-2GLI	150-mil SOIC (JEDEC)
	IS24C128B-2ZLI	3 x 4.4 mm TSSOP
	IS24C128B-2PLI	300-mil PDIP

*

1. Contact ISSI Sales Representatives for availability and other information.
2. Most listed part numbers are packed in tube.
3. For tape and reel, add “-TR” at the end of the P/N.
4. Refer to ISSI website for related declaration document on lead free, RoHS, halogen free, or Green, whichever is applicable.
5. ISSI offers Industrial grade for Commercial applications (0°C to +70°C).



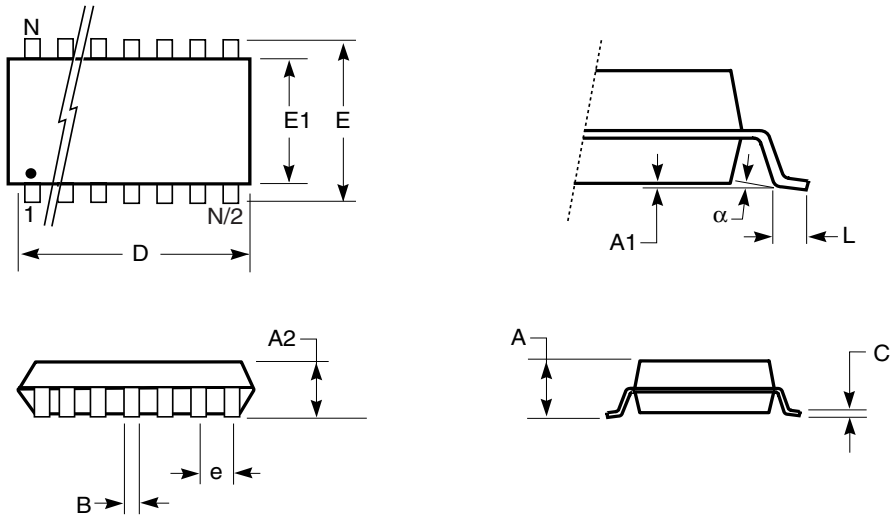
SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.35	—	1.75	0.053	—	0.069
A1	0.10	—	0.25	0.004	—	0.010
b	0.33	—	0.51	0.013	—	0.020
D	4.80	—	5.00	0.189	—	0.197
E	5.80	—	6.20	0.228	—	0.244
E1	3.80	—	4.00	0.150	—	0.157
e	1.27 BSC.			0.050 BSC.		
L	0.38	—	1.27	0.015	—	0.050
L1	0.25 BSC.			0.010 BSC.		
ZD	0.545 REF.			0.021 REF.		
θ	0	—	8°	0	—	8°

NOTE :

1. CONTROLLING DIMENSION : MM
2. DIMENSION D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION.

	TITLE	8L 150mil SOP Package Outline	REV.	B	DATE	07/20/2001

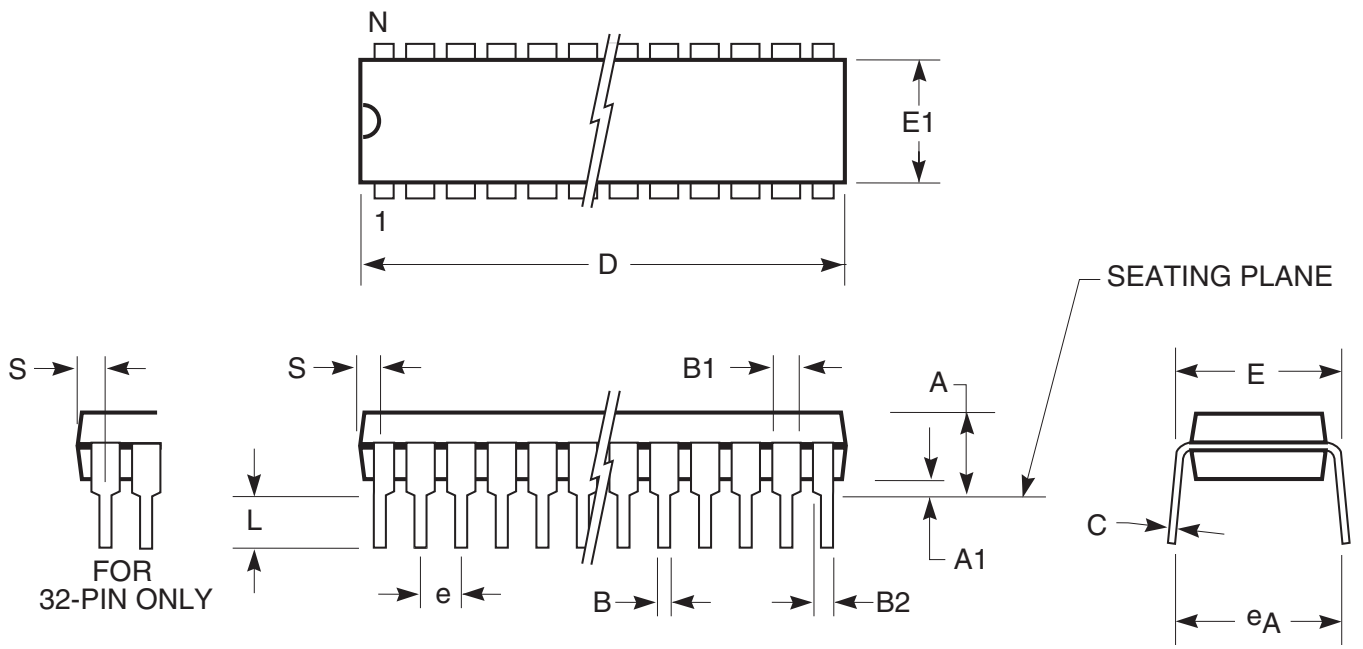
Thin Shrink Small Outline TSSOP
Package Code: Z (8 pin, 14 pin)



TSSOP (Z)				
Ref. Std.	JEDEC MO-153			
No. Leads	8			
	Millimeters		Inches	
Symbol	Min	Max	Min	Max
A	—	1.20	—	0.047
A1	0.05	0.15	0.002	0.006
A2	0.80	1.05	0.032	0.041
B	0.19	0.30	0.007	0.012
C	0.09	0.20	0.004	0.008
D	2.90	3.10	0.114	0.122
E1	4.30	4.50	0.169	0.177
E	6.40 BSC		0.252 BSC	
e	0.65 BSC		0.026 BSC	
L	0.45	0.75	0.018	0.030
α	—	8°	—	8°

TSSOP (Z)				
Ref. Std.	JEDEC MO-153			
No. Leads	14			
	Millimeters		Inches	
Symbol	Min	Max	Min	Max
A	—	1.20	—	0.047
A1	0.05	0.15	0.002	0.006
A2	0.80	1.05	0.031	0.041
B	0.19	0.30	0.007	0.012
C	0.09	0.20	0.0035	0.008
D	4.90	5.10	0.193	0.201
E1	4.30	4.50	0.170	0.177
E	6.40 BSC		0.252 BSC	
e	0.65 BSC		0.026 BSC	
L	0.45	0.75	0.0177	0.0295
α	—	8°	—	8°

300-mil Plastic DIP
Package Code: N,P



	MILLIMETERS		INCHES	
Sym.	**Min.**	**Max.**	**Min.**	**Max.**
N0. Leads		**8**		
A	3.68	4.57	0.145	0.180
A1	0.38	—	0.015	—
B	0.36	0.56	0.014	0.022
B1	1.14	1.52	0.045	0.060
B2	0.81	1.17	0.032	0.046
C	0.20	0.33	0.008	0.013
D	9.12	9.53	0.359	0.375
E	7.62	8.26	0.300	0.325
E1	6.20	6.60	0.244	0.260
e_A	8.13	9.65	0.320	0.380
e	2.54 BSC		0.100 BSC	
L	3.18	—	0.125	—
S	0.64	0.762	0.025	0.030

Notes:
1. Controlling dimension: inches, unless otherwise specified.
2. BSC = Basic lead spacing between centers.
3. Dimensions D and E1 do not include mold flash protrusions and should be measured from the bottom of the package.
4. Formed leads shall be planar with respect to one another within 0.004 inches at the seating plane.