MOTOROLA

Military 54LS251

8-Input Data Selector/ Multiplexer With Enable

ELECTRICALLY TESTED PER:
MIL-M-38510/30905

The 54LS251 is a high-speed 8-input Digital Multiplexer. It provides, in one package, the ability to select one bit of data from up to eight sources. The 'LS251 can be used as a universal function generator to generate any logic function of four variables. Both assertion and negation outputs are provided.

- Schottky Process For High-Speed
- Multifunction Capability
- On-Chip Select Logic Decoding
- Inverting and Non-Inverting 3-State Outputs
- Input Clamp Diodes Limit High-Speed Termination Effects

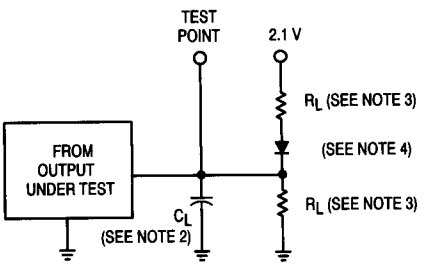
AVAILABLE AS:

1) JAN: JM38510/30905BXA
2) SMD: 7601601
3) 883: 54LS251/BXAJC

X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

THE LETTER "M" APPEARS BEFORE THE / ON LCC.

LOAD CIRCUIT FOR 3-STATE OUTPUT



Pin Names		Loading (Note a)	
		HIGH	LOW
S_0-S_2	Select Inputs	0.5 U.L.	0.25 U.L.
$\overline{EO}$	Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.
I_0-I_7	Multiplexer Inputs	0.5 U.L.	0.25 U.L.
$\overline{Z}$	Multiplexer Output	65 U.L.	15 U.L.
Z	Complementary Multiplexer Output	65 U.L.	15 U.L.

NOTE:
a. One TTL Unit Load (U.L.) = 40 μA HIGH/1.6mA LOW.

PIN ASSIGNMENTS

FUNCT.	DIL 620-09	FLATS 650-05	LCC 756A-02	BURN-IN (COND. A)
I_3	1	1	2	V_{CC}
I_2	2	2	3	V_{CC}
I_1	3	3	4	V_{CC}
I_0	4	4	5	V_{CC}
Z	5	5	7	V_{CC}
$\overline{Z}$	6	6	8	OPEN
$\overline{EO}$	7	7	9	GND
GND	8	8	10	GND
S_2	9	9	12	GND
S_1	10	10	13	GND
S_0	11	11	14	GND
I_7	12	12	15	V_{CC}
I_6	13	13	17	V_{CC}
I_5	14	14	18	V_{CC}
I_4	15	15	19	V_{CC}
V_{CC}	16	16	20	V_{CC}

BURN-IN CONDITIONS:
V_{CC} = 5.0 V MIN/6.0 V MAX

NOTES:
1. Input pulse characteristics: PRR ≤ 1.0 MHz, t_r = 15 ns, $t_f \leq 6.0$ ns.
2. C_L = 50 pF± 10% for t_{PLH}, t_{PHL}, t_{PZL} and t_{PZH} tests, C_L = 15 pF minimum for t_{PHZ} and t_{PLZ} tests. C_L includes scope probe, wiring and stray capacitance.
3. R_L = 2.0 kΩ ± 5.0%.
4. All diodes are 1N3064 or 1N916.
5. The limits specified for C_L = 15 pF, and C_L = 5.0 pF are guaranteed but not tested.

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TRUTH TABLE													
$\overline{EO}$	S_2	S_1	S_0	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	$\overline{Z}$	Z
H	X	X	X	X	X	X	X	X	X	X	X	(Z)	(Z)
L	L	L	L	L	X	X	X	X	X	X	X	H	L
L	L	L	L	H	X	X	X	X	X	X	X	L	H
L	L	L	H	X	L	X	X	X	X	X	X	H	L
L	L	L	H	X	H	X	X	X	X	X	X	L	H
L	L	H	L	X	X	L	X	X	X	X	X	H	L
L	L	H	L	X	X	H	X	X	X	X	X	L	H
L	L	H	H	X	X	X	L	X	X	X	X	H	L
L	L	H	H	X	X	X	H	X	X	X	X	L	H
L	H	L	L	X	X	X	X	L	X	X	X	H	L
L	H	L	L	X	X	X	X	H	X	X	X	L	H
L	H	L	H	X	X	X	X	X	L	X	X	H	L
L	H	L	H	X	X	X	X	X	H	X	X	L	H
L	H	H	L	X	X	X	X	X	X	L	X	H	L
L	H	H	L	X	X	X	X	X	X	H	X	L	H
L	H	H	H	X	X	X	X	X	X	X	L	H	L
L	H	H	H	X	X	X	X	X	X	X	H	L	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
(Z) = High Impedance (Off)

FUNCTIONAL DESCRIPTION

The 'LS251 is a logic implementation of a single pole, 8-position switch with the switch position controlled by the state of the three Select inputs, S_0, S_1, S_2. Both assertion and negation outputs are provided. The Output Enable input (EO) is active LOW. When it is not activated, the logic function provided at the output is:

$$Z = \overline{EO} \bullet (I_0 \bullet \overline{S}_0 \bullet \overline{S}_1 \bullet \overline{S}_2 + I_1 \bullet S_0 \bullet \overline{S}_1 \bullet \overline{S}_2 + I_2 \bullet \overline{S}_0 \bullet S_1 \bullet \overline{S}_2 + I_3 \bullet S_0 \bullet S_1 \bullet \overline{S}_2 + I_4 \bullet \overline{S}_0 \bullet \overline{S}_1 \bullet S_2 + I_5 \bullet S_0 \bullet \overline{S}_1 \bullet S_2 + I_6 \bullet \overline{S}_0 \bullet S_1 \bullet S_2 + I_7 \bullet S_0 \bullet S_1 \bullet S_2)$$

When the Output Enable is HIGH, both outputs are in the high impedance (high Z) state. This feature allows the multiplexer expansion by tying the outputs of up to 128 devices together. When the outputs of the 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. The Output Enable signals should be designed to ensure there is no overlap in the active LOW portion of the enable Voltage.

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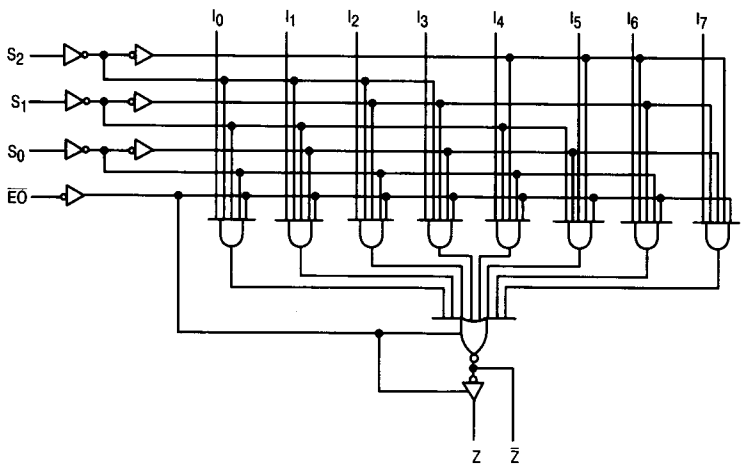
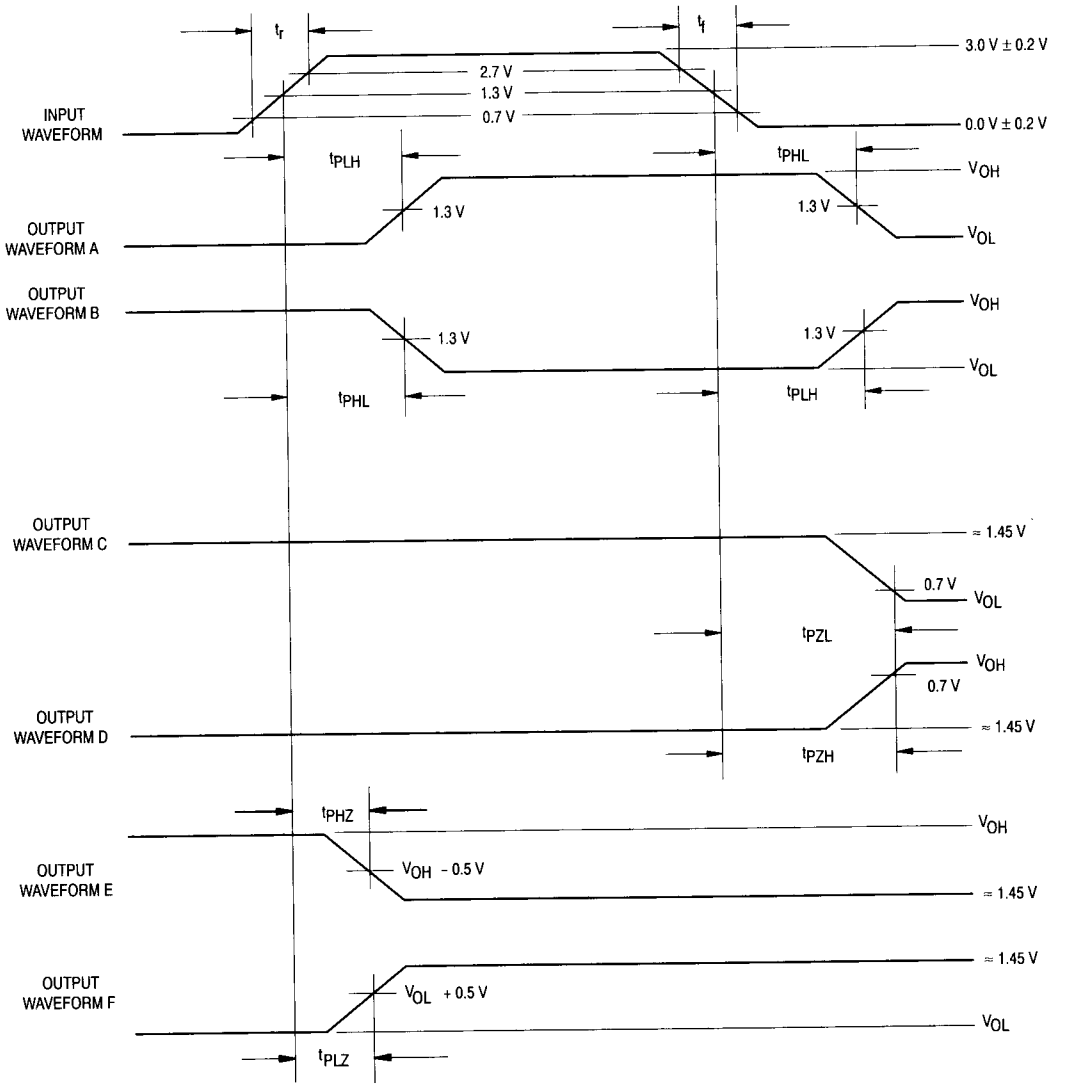
LOGIC DIAGRAM



WAVEFORMS


t_r
t_f
3.0 V ± 0.2 V
2.7 V
1.3 V
0.7 V
INPUT WAVEFORM
0.0 V ± 0.2 V
t_{PLH}
t_{PHL}
V_{OH}
1.3 V
1.3 V
OUTPUT WAVEFORM A
V_{OL}
OUTPUT WAVEFORM B
V_{OH}
1.3 V
1.3 V
V_{OL}
t_{PHL}
t_{PLH}
OUTPUT WAVEFORM C
≈ 1.45 V
0.7 V
V_{OL}
t_{PZL}
V_{OH}
0.7 V
OUTPUT WAVEFORM D
≈ 1.45 V
t_{PZH}
t_{PHZ}
V_{OH}
V_{OH} - 0.5 V
OUTPUT WAVEFORM E
≈ 1.45 V
≈ 1.45 V
OUTPUT WAVEFORM F
V_{OL} + 0.5 V
V_{OL}
t_{PLZ}

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Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Static Parameters:	+ 25°C		+ 125°C		- 55°C			
		Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V_{OH}	Logical "1" Output Voltage	2.4		2.4		2.4		V	V_{CC} = 4.5 V, I_{OH} = – 1.0 mA, V_{IH} = 2.0 V, V_{IL} = 0.7 V, S = 0.7 V or 2.0 V, $\overline{EO}$ = 0.7 V.
V_{OL}	Logical "0" Output Voltage		0.4		0.4		0.4	V	V_{CC} = 4.5 V, I_{OL} = 4.0 mA, V_{IL} = 0.7 V, S = 2.0 V or 0.7 V, $\overline{EO}$ = 0.7 V, V_{IH} = 2.0 V.
V_{IC}	Input Clamping Voltage		– 1.5					V	V_{CC} = 4.5 V, I_{IN} = – 18 mA, other inputs are open.
I_{IH}	Logical "1" Input Current		20		20		20	µA	V_{CC} = 5.5 V, V_{IH} = 2.7 V, other inputs are GND, S = 2.7 V, 5.5 V or GND.
I_{IHH}	Logical "1" Input Current		100		100		100	µA	V_{CC} = 5.5 V, V_{IHH} = 5.5 V, other inputs are GND, S = 5.5 V or GND.
$I_{IL(I)}$	Logical "0" Input Current	– 0.005	– 0.72	– 0.005	– 0.72	– 0.005	– 0.72	mA	V_{CC} = 5.5 V, $\overline{EO}$ = GND, V_{IN}= 0.4 V, S = 5.5 V or GND, other inputs = 5.5 V.
$I_{IL(\overline{EO})}$	Logical "0" Input Current	– 0.002	– 0.15	– 0.002	– 0.15	– 0.002	– 0.15	mA	V_{CC} = 5.5 V, V_{IN} = 5.5 V (all inputs), $\overline{EO}$ = 0.4 V.
$I_{IL(S)}$	Logical "0" Input Current	– 0.1	– 0.34	– 0.1	– 0.34	– 0.1	– 0.34	mA	V_{CC} = 5.5 V, V_{IN} = 0.4 V, other inputs = 5.5 V, $\overline{EO}$ = GND.
I_{OS}	Output Short Circuit Current	– 30	– 130	– 30	– 130	– 30	– 130	mA	V_{CC} = 5.5 V, V_{IN} = 5.5 V, other inputs are open, V_{OUT} = GND, $\overline{EO}$ = GND, S = 5.5 V or GND.
I_{OZH}	Output Off Current High		20		20		20	µA	V_{CC} = 5.5 V, V_{IN} = 5.5 V, V_{OUT} = 2.7 V, $\overline{EO}$ = 2.0 V, S = 0.7 V or 2.0 V.
I_{OZL}	Output Off Current Low		– 20		– 20		– 20	µA	V_{CC} = 5.5 V, V_{IN} = 5.5 V, V_{OUT} = 0.4 V, $\overline{EO}$ = 2.0 V, S = 2.0 V or 0.7 V.
I_{CCH}	Power Supply Current		10		10		10	mA	V_{CC} = 5.5 V, V_{IN} = 5.5 V (all inputs).
I_{CCL}	Power Supply Current		12		12		12	mA	V_{CC} = 5.5 V, V_{IN} = 5.5 V (all inputs), $\overline{EO}$ = GND.
V_{IH}	Logical "1" Input Voltage	2.0		2.0		2.0		V	V_{CC} = 4.5 V.
V_{IL}	Logical "0" Input Voltage		0.7		0.7		0.7	V	V_{CC} = 4.5 V.
	Functional Tests	Subgroup 7		Subgroup 8A		Subgroup 8B			per Truth Table with V_{CC} = 5.0 V, V_{INL} = 0.4 V, and V_{INH} = 2.4 V.

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Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Switching Parameters:	+ 25°C		+ 125°C		- 55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t_{PHL1} t_{PHL1}	Propagation Delay /Data-Output Data to Z Output	3.0 —	33 28	3.0 —	50 45	3.0 —	50 45	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF, R_L = 667 Ω.
t_{PLH1} t_{PLH1}	Propagation Delay /Data-Output Data to Z Output	3.0 —	33 28	3.0 —	50 45	3.0 —	50 45	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF, R_L = 667 Ω.
t_{PHL2} t_{PHL2}	Propagation Delay /Data-Output Data to $\overline{Z}$ Output	3.0 —	20 15	3.0 —	30 25	3.0 —	30 25	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF, R_L = 667 Ω.
t_{PLH2} t_{PLH2}	Propagation Delay /Data-Output Data to $\overline{Z}$ Output	3.0 —	20 15	3.0 —	30 25	3.0 —	30 25	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF, R_L = 667 Ω.
t_{PHL5} t_{PHL5}	Propagation Delay /Data-Output Select to Z Output	3.0 —	50 45	3.0 —	75 70	3.0 —	75 70	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF, R_L = 667 Ω.
t_{PLH5} t_{PLH5}	Propagation Delay /Data-Output Select to Z Output	3.0 —	50 45	3.0 —	75 70	3.0 —	75 70	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF, R_L = 667 Ω.
t_{PHL6} t_{PHL6}	Propagation Delay /Data-Output Select to $\overline{Z}$ Output	3.0 —	38 33	3.0 —	57 52	3.0 —	57 52	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF, R_L = 667 Ω.
t_{PLH6} t_{PLH6}	Propagation Delay /Data-Output Select to $\overline{Z}$ Output	3.0 —	38 33	3.0 —	57 52	3.0 —	57 52	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF, R_L = 667 Ω.
t_{PZH1} t_{PZH1}	Propagation Delay /Data-Output Output High-Low	3.0 —	50 45	3.0 —	75 70	3.0 —	75 70	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF, R_L = 667 Ω.
t_{PZL1} t_{PZL1}	Propagation Delay /Data-Output Output Low-High	3.0 —	45 40	3.0 —	68 63	3.0 —	68 63	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF, R_L = 667 Ω.
t_{PZH2} t_{PZH2}	Propagation Delay /Data-Output Output High-Low	3.0 —	32 45	3.0 —	48 43	3.0 —	48 43	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF, R_L = 667 Ω.
t_{PZL2} t_{PZL2}	Propagation Delay /Data-Output Output Low-High	3.0 —	45 40	3.0 —	68 63	3.0 —	68 63	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF, R_L = 667 Ω.
t_{PHZ1} t_{PHZ1}	Propagation Delay /Data-Output Output High-Low	3.0 —	50 45	3.0 —	75 70	3.0 —	75 70	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF, R_L = 667 Ω.
t_{PLZ1} t_{PLZ1}	Propagation Delay /Data-Output Output Low-High	3.0 —	35 25	3.0 —	45 40	3.0 —	45 40	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF, R_L = 667 Ω.
t_{PHZ2} t_{PHZ2}	Propagation Delay /Data-Output Output High-Low	3.0 —	60 55	3.0 —	90 85	3.0 —	90 85	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 5.0 pF, R_L = 667 Ω.
t_{PLZ2} t_{PLZ2}	Propagation Delay /Data-Output Output Low-High	3.0 —	35 25	3.0 —	45 40	3.0 —	45 40	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 5.0 pF, R_L = 667 Ω.

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