SRM20100L70/85/10

CMOS 1M-BIT STATIC RAM

- **Low Supply Current**
- **Access Time 70ns/85ns/100ns**
- **131,072 Words × 8-Bit Asynchronous**

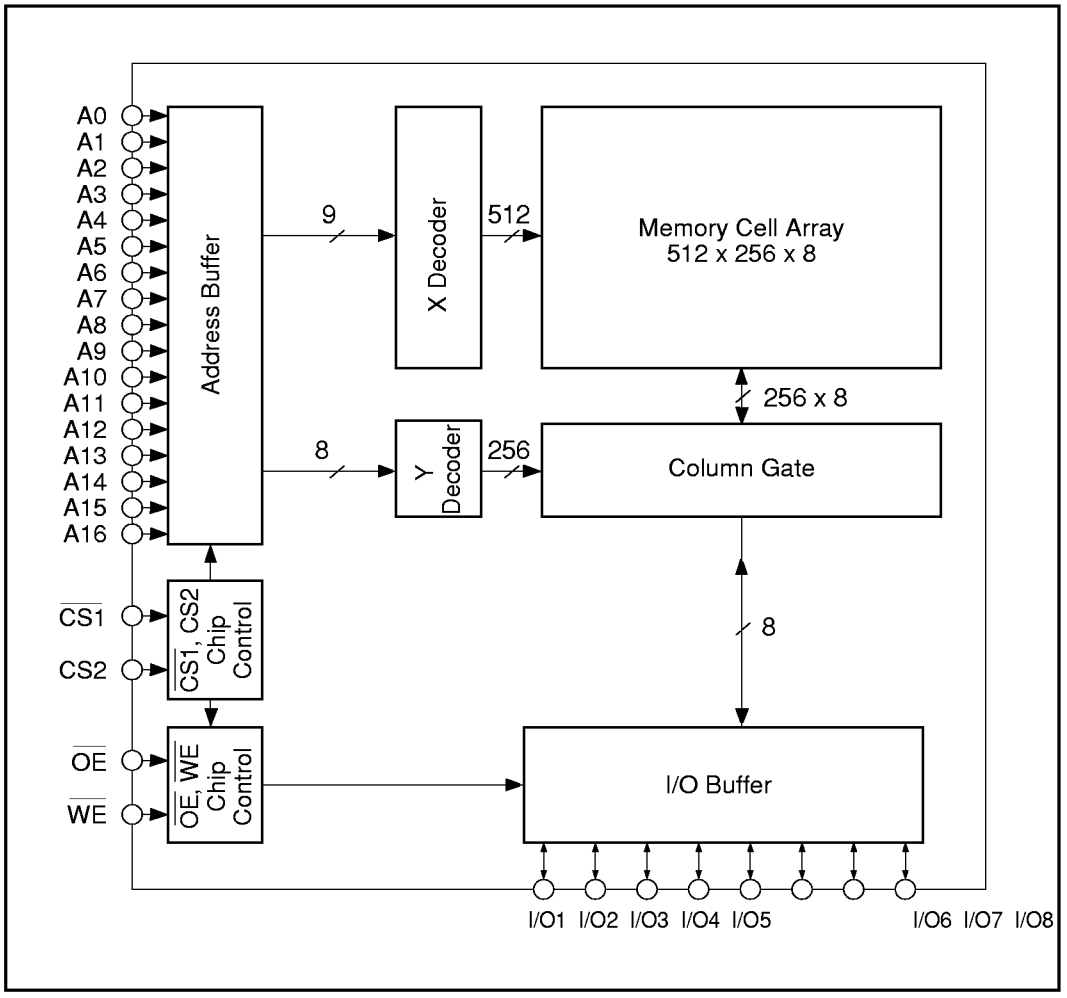
■ DESCRIPTION

The SRM20100L70/85/10 is a 131,072 words x 8-bit asynchronous, static, random access memory on a monolithic CMOS chip. Its very low standby power requirement makes it ideal for applications requiring non-volatile storage with back-up batteries. The asynchronous and static nature of the memory requires no external clock or refreshing circuit. Both the input and output ports are TTL compatible and the 3-state output allows easy expansion of memory capacity.

■ FEATURES

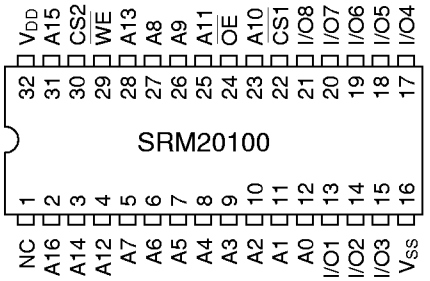
- Access time. . . . . SRM20100L70 . . . . . 70ns (Max)
  SRM20100L85 . . . . . 85ns (Max)
  SRM20100L10 . . . . . 100ns (Max)
- Low supply current . . . . . Standby. . . . . 2μA (Typ)
  Operation . . . . . 15mA/MHz (Typ)
- Completely static. . . . . No clock required
- Single power supply . . . . . 5V ± 10%
- TTL compatible inputs and outputs
- 3-state output with wired-OR capacity
- Non-volatile storage with battery back-up batteries
- Package . . . . . SRM20100LC70/85/10 . . . . . DIP-32pin (plastic)
  SRM20100LM70/85/10 . . . . . SOP6-32pin (plastic)
  SRM20100LTM70/85/10 . . . . . TSOP(I)-32pin (plastic)
  SRM20100LRM70/85/10. . . . . RTSOP(I)-32pin (plastic)

■ BLOCK DIAGRAM

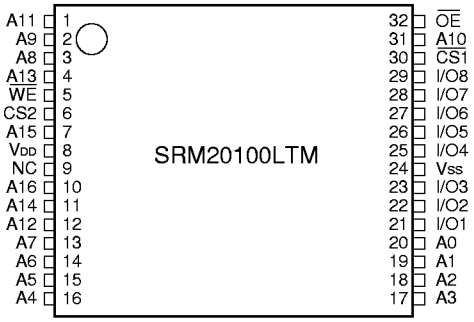


■ PIN CONFIGURATION

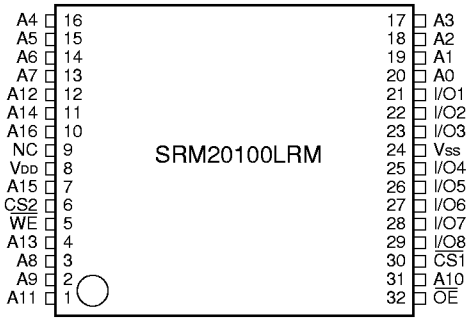
(DIP)



(TSOP)



(RTSOP)



■ PIN DESCRIPTION

A0 to A16	Address Input
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
$\overline{CS1}$	Chip Select 1
CS2	Chip Select 2
I/O1 to 8	Data Input/Output
V_{DD}	Power Supply (+5V)
V_{SS}	Power Supply (0V)
NC	No Connection

■ ABSOLUTE MAXIMUM RATINGS

V_{SS} = 0V

Parameter	Symbol	Rating	Unit
Supply voltage	V_{DD}	–0.5 to 7.0	V
Input voltage*	V_I	–0.5 to 7.0	V
Input/output voltage*	$V_{I/O}$	–0.5 to V_{DD} + 0.3	V
Power dissipation	P_D	1.0	W
Operating temperature	T_{OPR}	0 to 70	°C
Storage temperature	T_{STG}	–65 to 150	°C
Soldering temperature and time	T_{SOL}	260°C, 10s (Lead only)	—

* V_I, $V_{I/O}$ (Min.) = –3.0V(pulse width is 50ns)

■ DC RECOMMENDED OPERATING CONDITIONS

V_{SS} = 0V, T_a = 0 to 70°C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}	—	4.5	5.0	5.5	V
	V_{SS}	—	0	0	0	V
Input voltage	V_{IH}	—	2.2	3.5	V_{DD} + 0.3	V
	V_{IL}	—	–0.3*	—	0.8	V

* If pulse width is less than 50ns, it is –3.0V

■ ELECTRICAL CHARACTERISTICS

● DC Electrical Characteristics

V_{DD} = 5V±10%, V_{SS} = 0V, T_a = 0 to 70°C

Parameter	Symbol	Conditions	SRM20100L70			SRM20100L85			SRM20100L10			Unit
			Min	Typ*	Max	Min	Typ*	Max	Min	Typ*	Max	
Input leakage	I_{LI}	V_I = 0 to V_{DD}	–1	—	1	–1	—	1	–1	—	1	µA
Standby supply current	I_{DDS}	$\overline{CS1}$ = V_{IH} or CS2 = V_{IL}	—	1.0	3	—	1.0	3	—	1.0	3	mA
	I_{DDS1}	$\overline{CS1}$ = CS2 ≥ V_{DD} – 0.2V or CS2 ≤ 0.2V	—	2	100	—	2	100	—	2	100	µA
Average operating current	I_{DDA}	V_I = V_{IL}, V_{IH} $I_{I/O}$ = 0mA, t_{CYC} = Min	—	45	70	—	45	70	—	45	70	mA
Operating supply current	I_{DDO}	V_I = V_{IL}, V_{IH} I_{LO} = 0mA	—	15	35	—	15	35	—	15	35	mA
Output leakage	I_{LO}	$\overline{CS1}$ = V_{IH} or CS2 = V_{IL} or $\overline{WE}$ = V_{IL} or $\overline{OE}$ = V_{IH}, $V_{I/O}$ = 0 to V_{DD}	–1	—	1	–1	—	1	–1	—	1	µA
High level output voltage	V_{OH}	I_{OH} = –1.0mA	2.4	—	—	2.4	—	—	2.4	—	—	V
Low level output voltage	V_{OL}	I_{OL} = 2.1mA	—	—	0.4	—	—	0.4	—	—	0.4	V

* Typical values are measured at T_a = 25°C and V_{DD} = 5.0V

● Terminal Capacitance

(f = 1MHz, T_a = 25°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Address capacitance	C_{ADD}	V_{ADD} = 0V	—	—	9	pF
Input capacitance	C_I	V_I = 0V	—	—	10	pF
I/O capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	—	—	10	pF

● AC Electrical Characteristics

○ Read Cycle

V_{DD} = 5V ± 10%, V_{SS} = 0V, Ta = 0 to 70°C

Parameter	Symbol	Condi-tions	SRM20100L70		SRM20100L85		SRM20100L10		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t_{RC}	*1	70	—	85	—	100	—	ns
Address access time	t_{ACC}		—	70	—	85	—	100	ns
Chip select1 access time	t_{ACS1}		—	70	—	85	—	100	ns
Chip select2 access time	t_{ACS2}		—	70	—	85	—	100	ns
Output enable access time	t_{OE}		—	40	—	45	—	50	ns
Chip select1 output set time	t_{CLZ1}	*2	10	—	10	—	10	—	ns
Chip select1 output floating	t_{CHZ1}		—	30	—	30	—	35	ns
Chip select2 output set time	t_{CLZ2}		10	—	10	—	10	—	ns
Chip select2 output floating	t_{CHZ2}		—	30	—	30	—	35	ns
Output enable output set time	t_{OLZ}		5	—	5	—	5	—	ns
Output enable output floating	t_{OHZ}		—	30	—	30	—	35	ns
Output hold time	t_{OH}	*1	10	—	10	—	10	—	ns

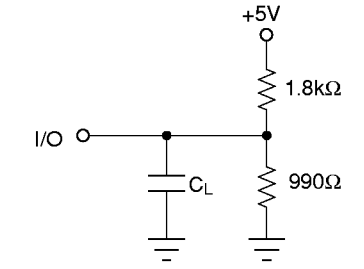
○ **Write Cycle**

V_{DD} = 5V ± 10%, V_{SS} = 0V, T_a = 0 to 70°C

Parameter	Symbol	Conditions	SRM20100L70		SRM20100L85		SRM20100L10		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t_{WC}	*1	70	—	85	—	100	—	ns
Chip Select time1	t_{CW1}		60	—	70	—	80	—	ns
Chip Select time2	t_{CW2}		60	—	70	—	80	—	ns
Address enable time	t_{AW}		60	—	70	—	80	—	ns
Address setup time	t_{AS}		0	—	0	—	0	—	ns
Write pulse width	t_{WP}		55	—	65	—	75	—	ns
Address hold time	t_{WR}		0	—	0	—	0	—	ns
Input data setup time	t_{DW}		30	—	35	—	40	—	ns
Input data hold time	t_{DH}		0	—	0	—	0	—	ns
$\overline{WE}$ output floating	t_{WHZ}	*2	—	30	—	30	—	35	ns
$\overline{WE}$ output setup time	t_{OW}		5	—	5	—	5	—	ns

***1. Test Conditions**

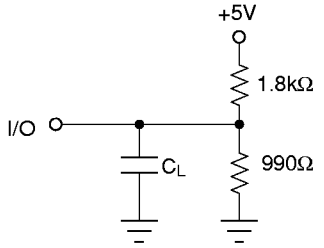
1. Input pulse level: 0.6V to 2.4V
2. tr = tf = 5ns
3. Input and output timing reference levels : 1.5V
4. Output load C_L = 100pF



C_L=100pF (includes Jig Capacitance)

***2. Test Conditions**

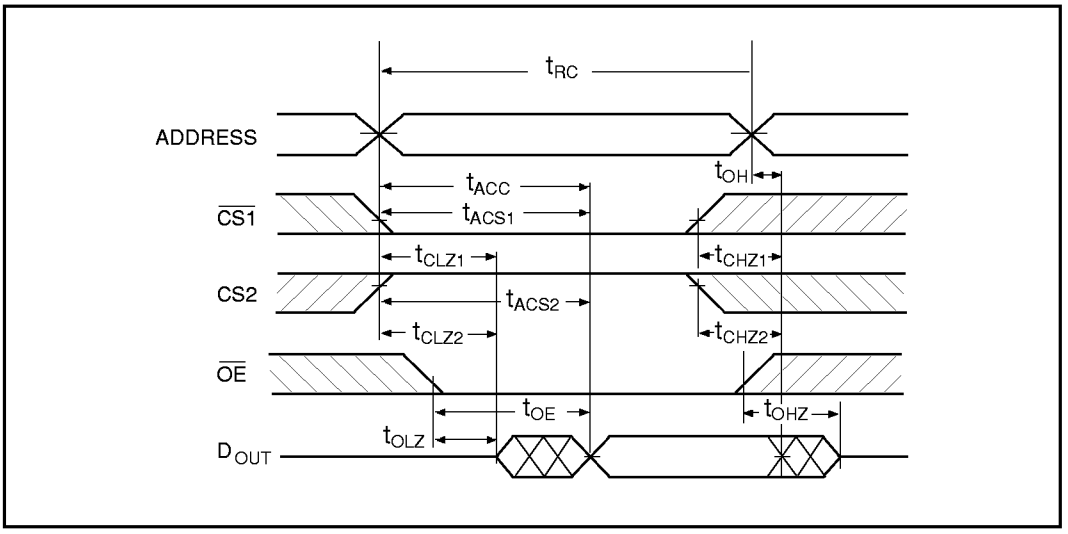
1. Input pulse level: 0.6V to 2.4V
2. tr = tf = 5ns
3. Input timing reference levels : 1.5V
4. Output timing reference levels: ± 200mV (the level displaced from stable output voltage level)
5. Output load C_L = 5pF



C_L=5pF (includes Jig Capacitance)

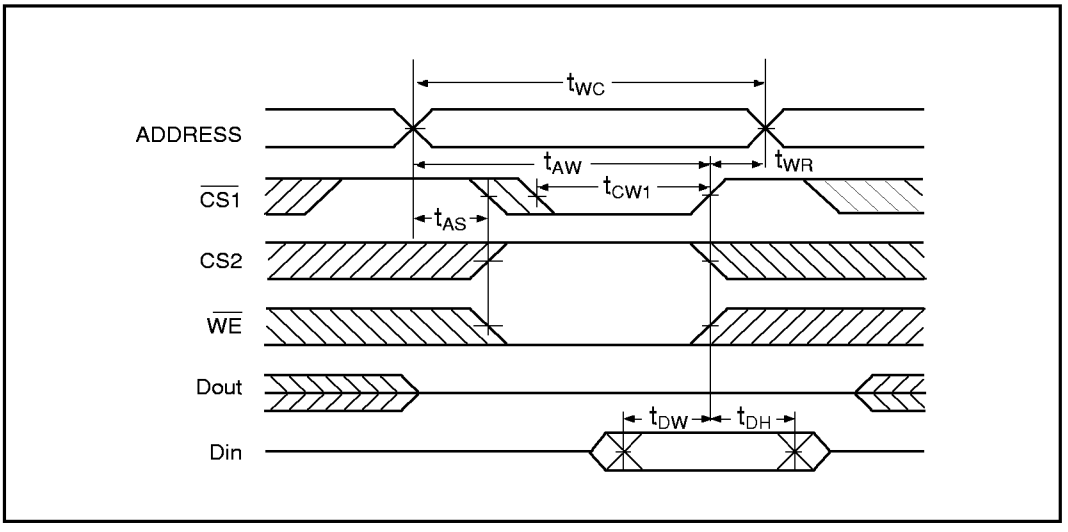
● **Timing Charts**

○ **Read Cycle*1**



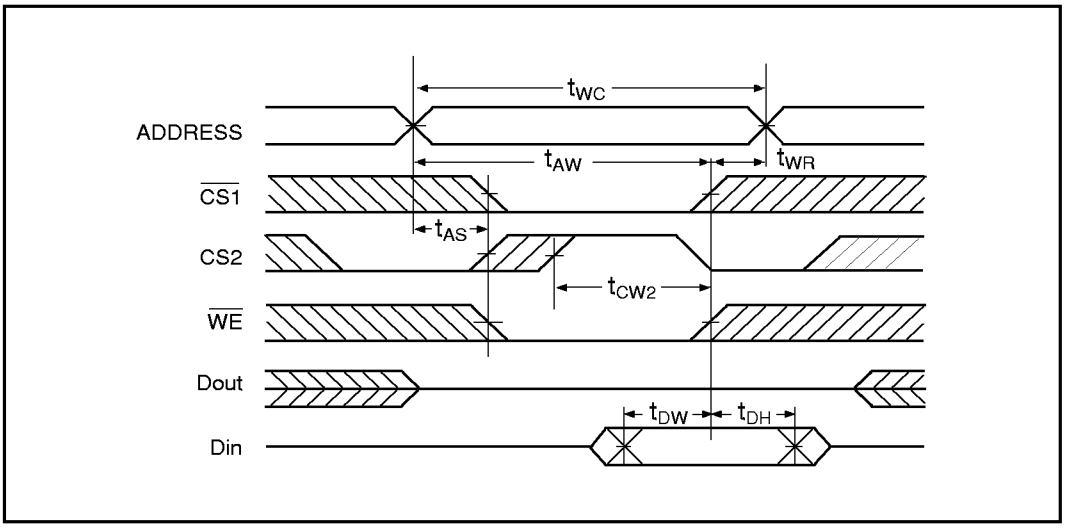
Note: *1. During read cycle time, $\overline{WE}$ should be "H" level.

○ **Write Cycle (1) ($\overline{CS1}$ Control)*2**



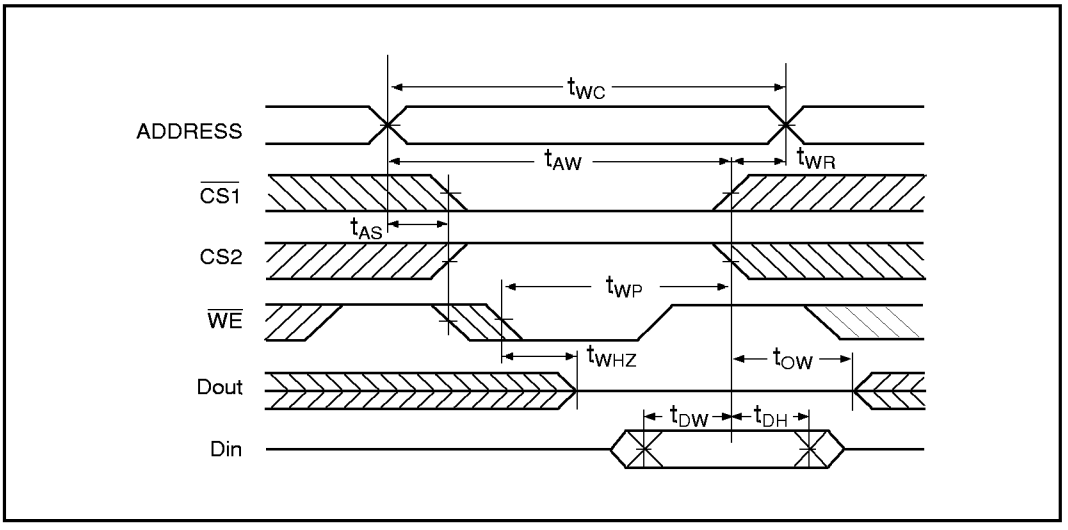
Note: *2. During write cycle time that is controlled by $\overline{CS1}$ or CS2, the output buffer is in high impedance state, whether $\overline{OE}$ level is "H" or "L".

○ **Write Cycle (2) (CS2 Control)*2**



Note: *2. During write cycle time that is controlled by $\overline{CS1}$ or CS2, the output buffer is in high impedance state, whether $\overline{OE}$ level is "H" or "L".

○ **Write Cycle (3) ($\overline{WE}$ Control)*3, *4**



Note: *3. During the write cycle that is controlled by $\overline{WE}$, the output buffer is in high impedance state if $\overline{OE}$ is "H" level.
*4. When I/O terminals are in output mode, be careful not to send conflicting (opposite) signals to the I/O terminals.

■ DATA RETENTION CHARACTERISTIC WITH LOW VOLTAGE POWER SUPPLY

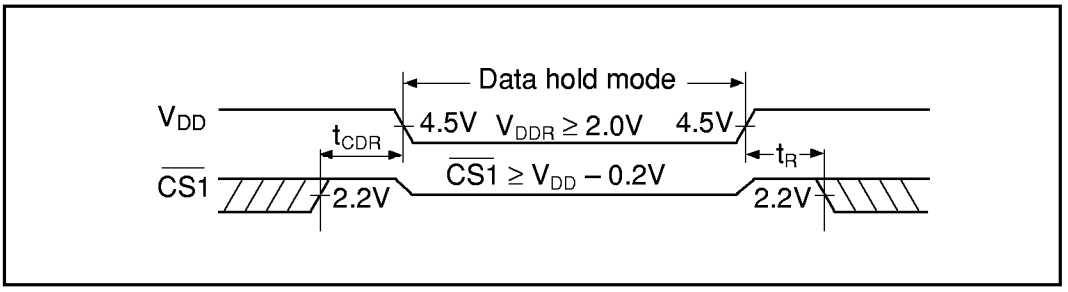
(T_a = 0 to 70°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data retention supply voltage	V_{DDR}		2.0	—	5.5	V
Data retention current	I_{DDR}	V_{DD} = 3V $\overline{CS1}$ = CS2 ≥ V_{DD} – 0.2V or CS2 < 0.2V	—	1*	50	µA
Chip select data hold time	t_{CDR}		0	—	—	ns
Operation recovery time	t_R		t_{RC}**	—	—	ns

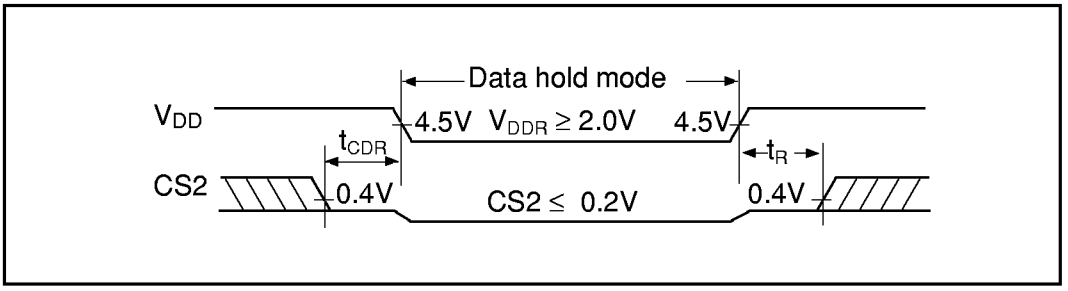
* T_a = 25°C

** t_{RC} = Read cycle time

● Data Retention Timing ($\overline{CS1}$ Control)



● Data Retention Timing (CS2 Control)



■ FUNCTIONS

● Truth Table

$\overline{CS1}$	CS2	$\overline{OE}$	$\overline{WE}$	Data I/O	Mode	I_{DD}
H	X	—	—	Hi-Z	Unselected	I_{DDS}, I_{DDS1}
—	L	—	—	Hi-Z	Unselected	I_{DDS}, I_{DDS1}
L	H	X	L	Input data	Write	I_{DD0}
L	H	L	H	Output data	Read	I_{DD0}
L	H	H	H	Hi-Z	Output disable	I_{DD0}

X: "H" or "L"
—: "H", "L" or "Hi-Z"

● Reading Data

Data can be read by setting the addresses as follows:

$\overline{CS1}$ — low CS2 — high $\overline{OE}$ — low $\overline{WE}$ — high

Since data I/O terminals are in a high-impedance state when $\overline{OE}$ is high, the data bus line can be used for other operations, reducing data access time.

● Writing Data

The four methods of writing data into memory are as follows:

1. Set CS2 high, $\overline{WE}$ low, set addresses and send a low pulse to $\overline{CS1}$.
2. Set $\overline{CS1}$ low, $\overline{WE}$ low, set addresses and send a high pulse to CS2.
3. Set $\overline{CS1}$ low, CS2 high, set addresses and send a low pulse to $\overline{WE}$.
4. Set addresses, send a low pulse to $\overline{CS1}$ and $\overline{WE}$, and send a high pulse to CS2.

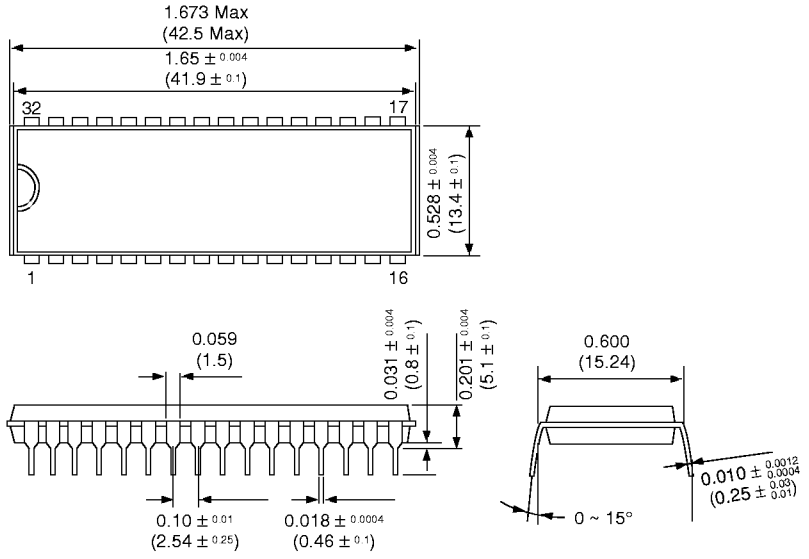
No matter which data writing configuration is used, data at the data I/O terminals are latched to the SRM20100L70/85/10 at the end of the period that $\overline{CS1}$ and $\overline{WE}$ are low, and CS2 is high. Since Data I/O terminals are always in a high-impedance state when $\overline{CS1}$ and $\overline{OE}$ are high, and when CS2 is low, data bus contention is avoided.

● Standby Mode

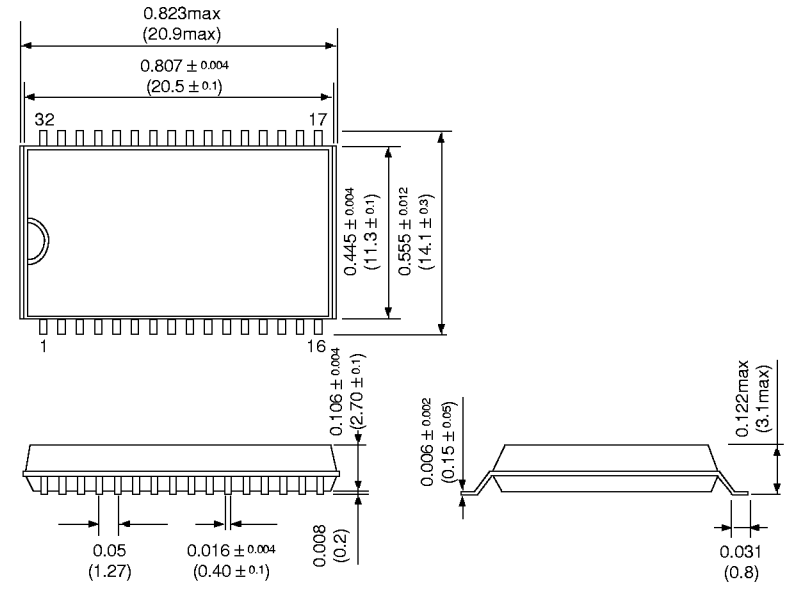
When $\overline{CS1}$ is high, or CS2 is low, the SRM20100L70/85/10 is in standby mode. During this state, data I/O terminals are Hi-Z, and all address inputs, data, and $\overline{WE}$ can be either high or low. When $\overline{CS1}$ and CS2 are greater than V_{DD}–0.2V or when CS2 is less than 0.2V, current flow in the SRM20100L70/85/10 is negligible, except in high resistance areas.

■ PACKAGE DIMENSIONS

Plastic 32-pin DIP **Unit: inch (mm)**

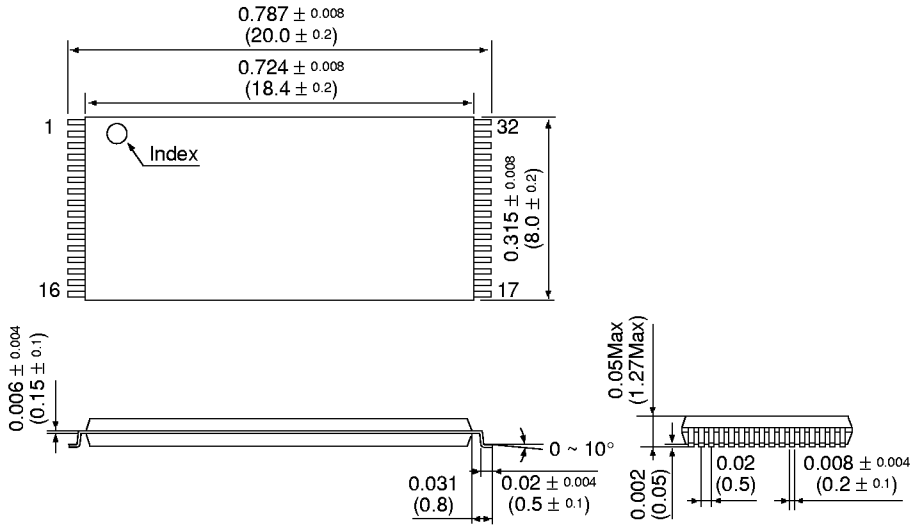


Plastic SOP6-32 pin*1 **Unit: inch (mm)**



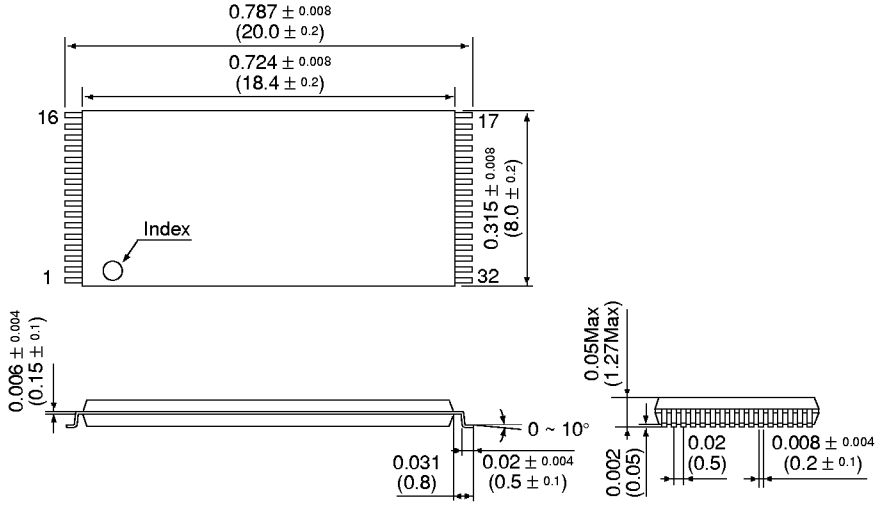
*1 SRM20100LM70/85/10 has the same characteristics as SRM20100LC70/85/10.

Plastic 32-pin TSOP(I)*1 **Unit: inch (mm)**



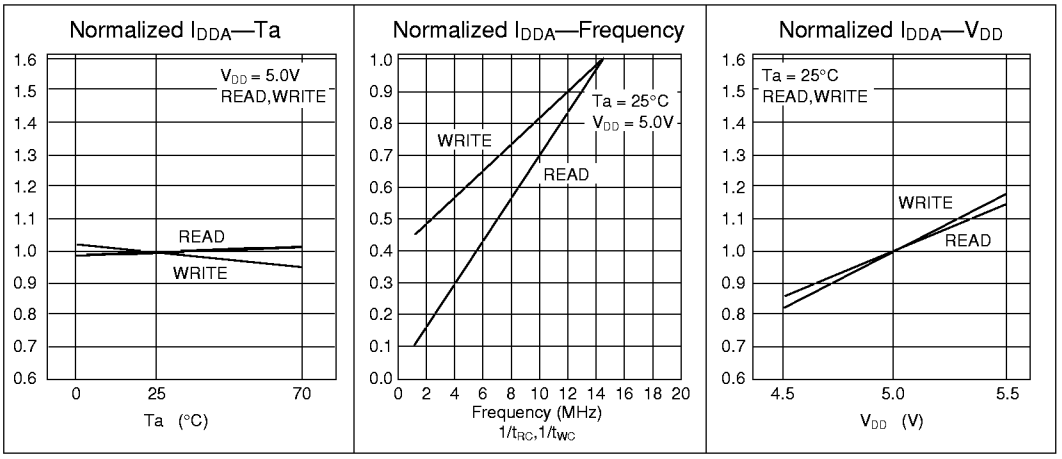
*1 SRM20100LTM70/85/10 has the same characteristics as SRM20100L70/85/10.

Plastic 32-pin RTSOP(I)*2 **Unit: inch (mm)**



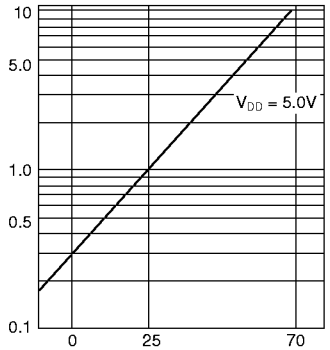
*2 SRM20100LRM70/85/10 has the same characteristics as SRM20100L70/85/10.

■ CHARACTERISTIC CURVES

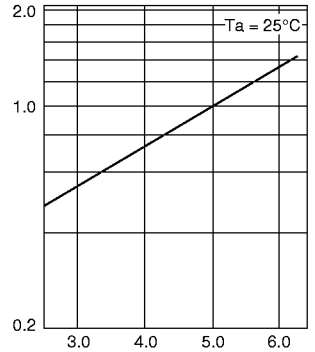


■ CHARACTERISTIC CURVES (Continued)

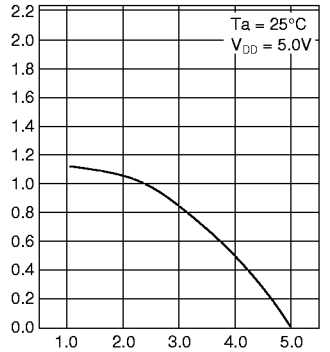
Normalized I_{DDS1}—Ta



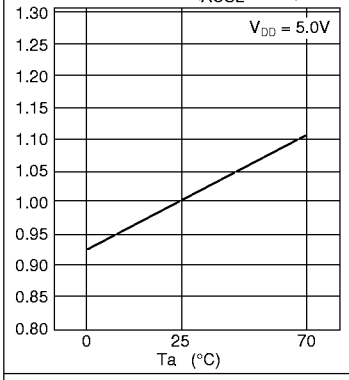
Normalized I_{DDS1}—V_{DD}



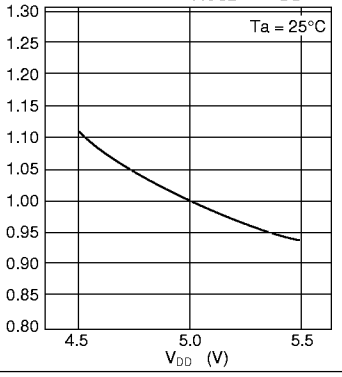
Normalized I_{OH}—V_{OH}



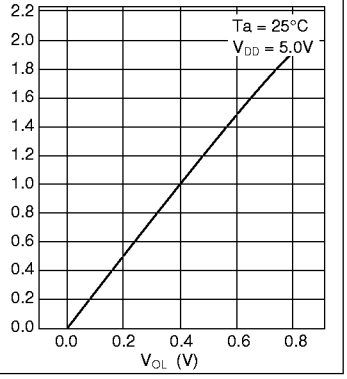
Normalized t_{ACC} / t_{ACS1} / t_{ACS2}—Ta



Normalized t_{ACC} / t_{ACS1} / t_{ACS2}—V_{DD}



Normalized I_{OL}—V_{OL}



Normalized t_{ACC} / t_{ACS1} / t_{ACS2}—C_L