STK11C68AM

CMOS/SNOS nvSRAM
Military
High Performance
8K x 8 Non-Volatile Static RAM

PRELIMINARY

FEATURES

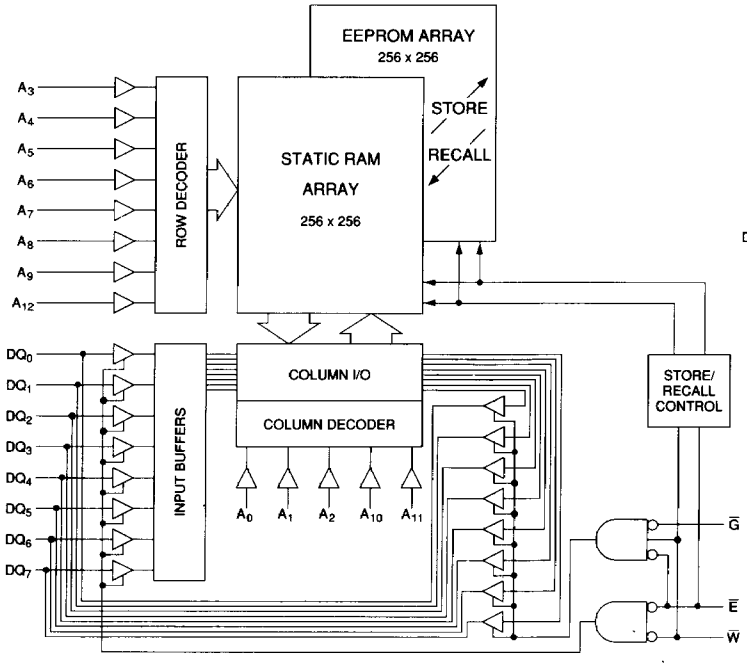
- **Non-Volatile Data Integrity**
- **45, 55 and 70ns Address Access Times**
- **45, 55 and 70ns Chip Enable Access Times**
- **Unlimited Read and Write to SRAM**
- **Unlimited Recall cycles from EEPROM**
- **10^5 Store cycles to EEPROM**
- **Software initiated Store to EEPROM**
- **Software initiated Recall from EEPROM**
- **Automatic Recall on Power Up**
- **Automatic Store Timing**
- **Single 5V ±10% Operation**
- **Military Temperature Range –55°C to 125°C**
- **10 year data retention in EEPROM**
- **JEDEC SRAM pinout in a 600 mil 28 pin DIP**
- **JEDEC SRAM pinout in a 32 pin LCC**
- **Available in an industry standard 300 mil DIP**

DESCRIPTION

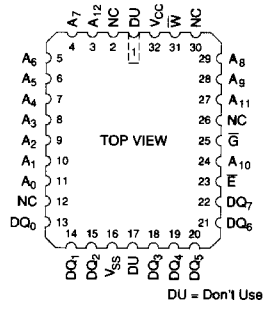
The Simtek STK11C68AM is a fast static RAM (35, 45 and 55ns), with a non-volatile electrically-erasable PROM (EEPROM) cell incorporated in each static memory cell. The SRAM can be read and written an unlimited number of times, while independent non-volatile data resides in EEPROM. Data transfers from the SRAM to the EEPROM (STORE) or from the EEPROM to the SRAM (RECALL) are initiated through software sequences. A RECALL also takes place upon power-up. It combines the high performance and ease of use of a fast SRAM with the data integrity of non-volatility.

The STK11C68AM features the JEDEC standard pinout for 8K x 8 SRAMs in a 28-pin 600 mil dual in line package, a 32 pin LCC or a 28-pin 300 mil DIP. will be screened to MIL-STD method 5004 and 5005. Simtek is currently establishing a military standard compliant program.

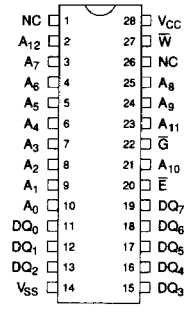
LOGIC BLOCK DIAGRAM



PIN CONFIGURATIONS



DU = Don't Use



PIN NAMES

$A_0 - A_{12}$	Address Inputs
$\overline{W}$	Write Enable
$DQ_0 - DQ_7$	Data In/Out
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground

Simtek Corporation
1465 Kelly Johnson Blvd.
Colorado Springs, Colorado 80920 USA
(719) 531-9444 FAX (719) 531-9481

ABSOLUTE MAXIMUM RATINGS[a]

Voltage on typical input relative to V_{SS}.....–0.6V to 7.0V
Voltage on DQ_{0-7} and $\overline{W}$.....–0.5V to (V_{CC}+0.5V)
Temperature under bias.....–55°C to 125°C
Storage temperature.....–65°C to 150°C
Power dissipation.....1W
DC output current.....15mA
(One output at a time, one second duration)

Note a: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
V_{IH}	Input Logic "1" Voltage	2.0		V_{CC}+.5	V	All Inputs
V_{IL}	Input Logic "0" Voltage	V_{SS}–.5		0.8	V	All Inputs
T_A	Ambient Operating Temperature	-55		125	°C	

DC ELECTRICAL CHARACTERISTICS[b,c]

(-55°C≤T_A≤125°C) (V_{CC}=5.0V ±10%)

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC}	Average V_{CC} Power Supply Current		90 85 80	mA mA mA	t_{AVAV}=45ns t_{AVAV}=55ns t_{AVAV}=70ns
I_{SB_1}	V_{CC} Power Supply Current (Standby, Cycling TTL Input Levels)		19 19 19	mA mA mA	t_{AVAV}=45ns t_{AVAV}=55ns t_{AVAV}=70ns $\overline{E}$≥V_{IH} all other inputs cycling
I_{SB_2}	V_{CC} Power Supply Current (Standby, Stable CMOS Input Levels)		2	mA	$\overline{E}$≥(V_{CC}–0.2V) All other inputs at V_{IN}≤ 0.2V or ≥(V_{CC}–0.2V)
I_{ILK}	Input Leakage Current (Any Input)		±1	µA	V_{CC}=max V_{IN}=V_{SS} to V_{CC}
I_{OLK}	Off State Output Leakage Current		±5	µA	V_{CC}=max V_{IN}=V_{SS} to V_{CC}
V_{OH}	Output Logic "1" Voltage	2.4		V	I_{OUT}=–4mA
V_{OL}	Output Logic "0" Voltage		0.4	V	I_{OUT}=8mA

Note b: I_{CC} is dependent on output loading and cycle rate. The specified values are obtained with outputs unloaded.
Note c: Bringing $\overline{E}$≥V_{IH} will not produce standby currents levels until any non-volatile cycle in progress has timed out. See MODE SELECTION table.

AC TEST CONDITIONS

Input Pulse Levels	V_{SS} to 3V
Input Rise and Fall Times	≤ 5ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Figure 1

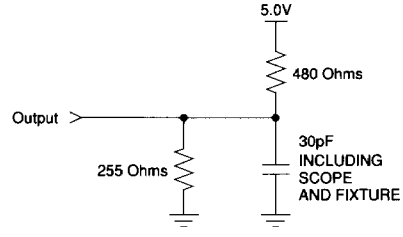


Figure 1: AC Output Loading

CAPACITANCE (T_A=25°C, f=1.0MHz)[d]

SYMBOL	PARAMETER	MAX	UNITS	CONDITIONS
C_{IN}	Input Capacitance	5	pF	ΔV=0 to 3V
C_{OUT}	Output Capacitance	7	pF	ΔV=0 to 3V

Note d: This parameter is characterized and not 100% tested.

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1465 Kelly Johnson Blvd.
Colorado Springs, Colorado 80920 USA
(719) 531-9444 FAX (719) 531-9481

SRAM MEMORY OPERATION

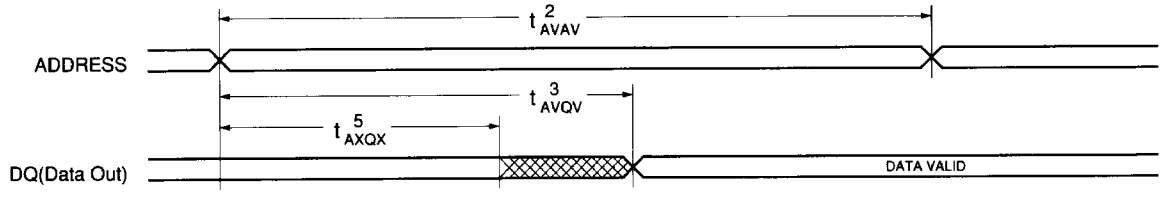
READ CYCLES 1 & 2[e]

(-55°C≤T_A≤125°C) (V_{CC}=5.0V ±10%)

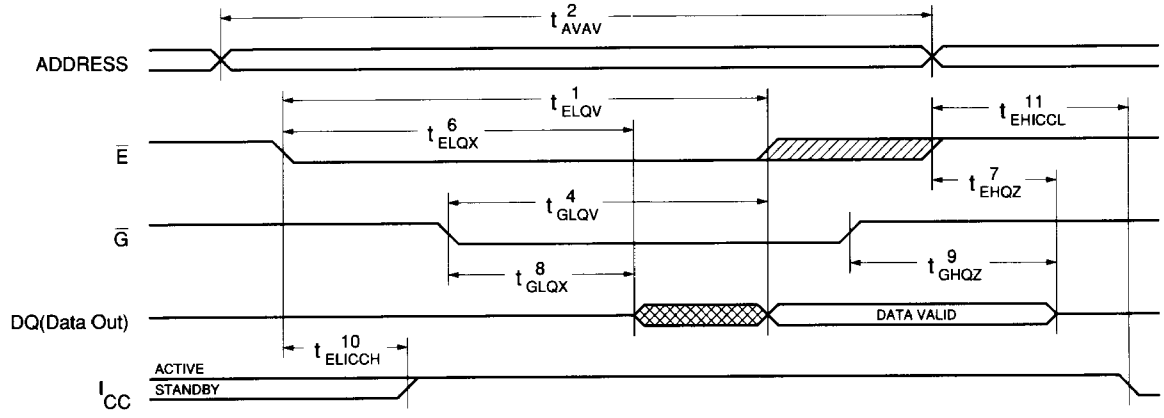
NO.	SYMBOL		PARAMETER	STK11C68AM-45		STK11C68AM-55		STK11C68AM-70		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX		
1	t_{ELQV}	t_{ACS}	Chip Enable Access Time		45		55		70	ns	
2	t_{AVAV}	t_{RC}	Read Cycle Time	45		55		70		ns	f
3	t_{AVQV}	t_{AA}	Address Access Time		45		55		70	ns	g
4	t_{GLQV}	t_{OE}	Output Enable to Data Valid		20		25		30	ns	
5	t_{AXQX}	t_{OH}	Output Hold After Address Change	5		5		5		ns	
6	t_{ELQX}	t_{LZ}	Chip Enable to Output Active	5		5		5		ns	
7	t_{EHQZ}	t_{OHZ}	Chip Disable to Output Inactive		20		25		30	ns	h
8	t_{GLQX}	t_{OLZ}	Output Enable to Output Active	0		0		0		ns	
9	t_{GHQZ}	t_{HZ}	Output Disable to Output Inactive		20		25		30	ns	h
10	t_{ELICCH}	t_{PA}	Chip Enable to Power Active	0		0		0		ns	i
11	t_{EHICCL}	t_{PS}	Chip Enable to Power Standby		25		25		25	ns	b,i

Note b: Bringing $\overline{E}$≥V_{IH} will not produce standby currents until any non-volatile cycle in progress has timed out. See MODE SELECTION table.
Note e: $\overline{E}$, $\overline{G}$ and $\overline{W}$ must make the transition between V_{IH} (min) to V_{IL} (max), or V_{IL} (max) to V_{IH} (min) in a monotonic fashion.
Note f: For READ CYCLE 1 and 2, $\overline{W}$ is high for entire cycle.
Note g: Device is continuously selected with $\overline{E}$ low, and $\overline{G}$ low.
Note h: Measured ±200mV from steady state output voltage. Load capacitance is 5pF.
Note i: Parameter guaranteed but not tested.

READ CYCLE 1[f,g]



READ CYCLE 2[f]



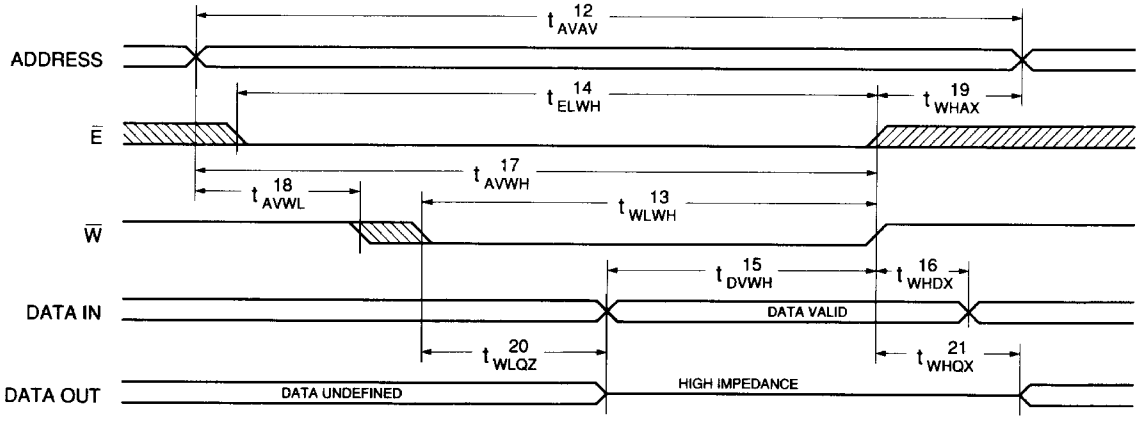
Simtek Corporation
1465 Kelly Johnson Blvd.
Colorado Springs, Colorado 80920 USA
(719) 531-9444 FAX (719) 531-9481

WRITE CYCLE 1: $\overline{W}$ CONTROLLED[e,j]

(-55°C≤T_A≤125°C) (V_{CC}=5.0V ±10%)

NO.	SYMBOL		PARAMETER	STK11C68AM-45		STK11C68AM-55		STK11C68AM-70		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX		
12	t_{AVAV}	t_{WC}	Write Cycle Time	45		55		70		ns	
13	t_{WLWH}	t_{WP}	Write Pulse Width	40		50		65		ns	
14	t_{ELWH}	t_{CW}	Chip Enable to End of Write	40		50		65		ns	
15	t_{DVWH}	t_{DW}	Data Set-up to End of Write	15		20		25		ns	
16	t_{WHDX}	t_{DH}	Data Hold After End of Write	0		0		0		ns	
17	t_{AVWH}	t_{AW}	Address Set-up to End of Write	40		50		65		ns	
18	t_{AVWL}	t_{AS}	Address Set-up to Start of Write	0		0		0		ns	
19	t_{WHAX}	t_{WR}	Address Hold After End of Write	0		0		0		ns	
20	t_{WLQZ}	t_{WZ}	Write Enable to Ouput Disable		25		30		40	ns	h
21	t_{WHQX}	t_{OW}	Output Active After End of Write	5		5		5		ns	k

WRITE CYCLE 1: $\overline{W}$ CONTROLLED[e,j]



WRITE CYCLE 2: $\overline{E}$ CONTROLLED[e,j]

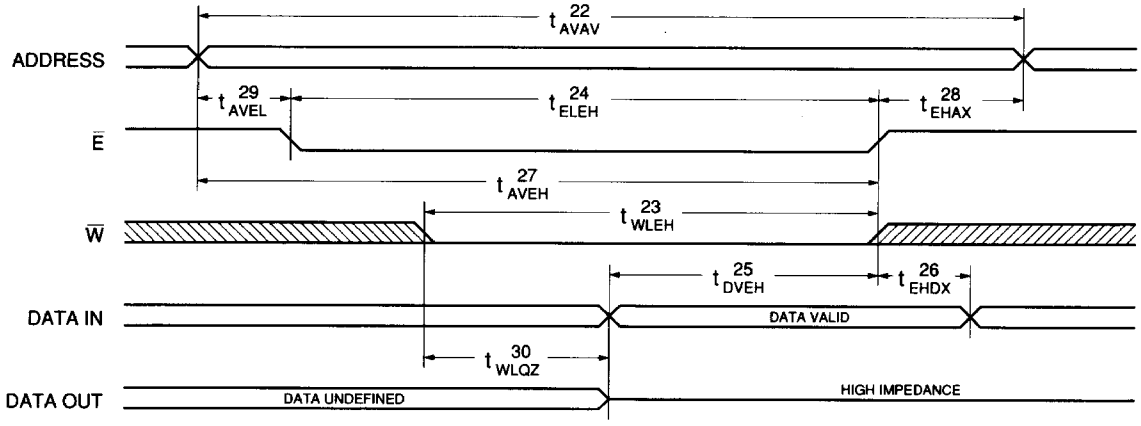
(-55°C≤T_A≤125°C) (V_{CC}=5.0V ±10%)

NO.	SYMBOL		PARAMETER	STK11C68AM-45		STK11C68AM-55		STK11C68AM-70		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX		
22	t_{AVAV}	t_{WC}	Write Cycle Time	45		55		70		ns	
23	t_{WLEH}	t_{WP}	Write Pulse Width	40		50		65		ns	
24	t_{ELEH}	t_{CW}	Chip Enable to End of Write	40		50		65		ns	
25	t_{DVEH}	t_{DW}	Data Set-up to End of Write	20		25		35		ns	
26	t_{EHDX}	t_{DH}	Data Hold After End of Write	0		0		0		ns	
27	t_{AVEH}	t_{AW}	Address Set-up to End of Write	40		50		65		ns	
28	t_{EHAX}	t_{AS}	Address Hold After End of Write	0		0		0		ns	
29	t_{AVEL}	t_{WR}	Address Set-up To Start of Write	0		0		0		ns	
30	t_{WLQZ}	t_{WZ}	Write Enable to Ouput Disable		25		30		40	ns	h

Note e: $\overline{E}$, $\overline{G}$ and $\overline{W}$ must make the transition between V_{IH} (max) to V_{IL} (max), or V_{IL} (max) to V_{IH} (min) in a monotonic fashion.
Note h: Measured ±200mV from steady state output voltage. Load capacitance is 5pF.
Note j: $\overline{E}$ or $\overline{W}$ must be ≥V_{IH} during address transitions.
Note k: If $\overline{W}$ is low when $\overline{E}$ goes low, the outputs remain in the high impedance state.

Simtek Corporation
1465 Kelly Johnson Blvd.
Colorado Springs, Colorado 80920 USA
(719) 531-9444 FAX (719) 531-9481

WRITE CYCLE 2: $\overline{E}$ CONTROLLED[h,j]



NON-VOLATILE MEMORY OPERATION

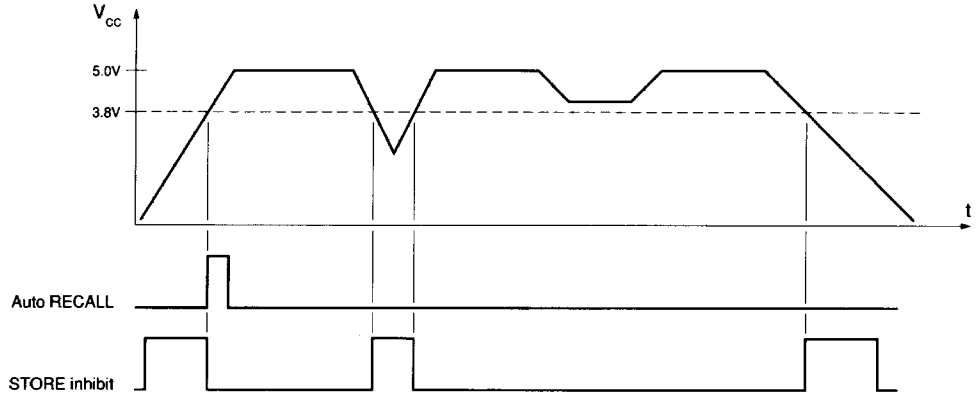
MODE SELECTION

$\overline{E}$	$\overline{W}$	A_{12}-A_0 (hex)	MODE	I/O	POWER	NOTES
H	X	X	Not Selected	Output High Z	Standby	
L	H	X	Read RAM	Output Data	Active	n
L	L	X	Write RAM	Input Data	Active	
L	H	0000	Read RAM	Output Data	Active	m, n
		1555	Read RAM	Output Data		m, n
		0AAA	Read RAM	Output Data		m, n
		1FFF	Read RAM	Output Data		m, n
		10F0	Read RAM	Output Data		m, n
		0F0F	Non-volatile Store	Output High Z		m
L	H	0000	Read RAM	Output Data	Active	m, n
		1555	Read RAM	Output Data		m, n
		0AAA	Read RAM	Output Data		m, n
		1FFF	Read RAM	Output Data		m, n
		10F0	Read RAM	Output Data		m, n
		0F0E	Non-volatile Recall	Output High Z		m

Note m: The six consecutive addresses must be in order listed – (0000, 1555, 0AAA, 1FFF, 10F0, 0F0F) for a STORE cycle or (0000, 1555, 0AAA, 1FFF, 10F0, 0F0E) for a RECALL cycle. $\overline{W}$ must be high during all six consecutive cycles. See STORE CYCLE and RECALL CYCLE tables and diagrams for further details.

Note n: I/O state assumes that $\overline{G} \leq V_{IL}$.

AUTOMATIC RECALL AND STORE INHIBIT:



Simtek Corporation
1465 Kelly Johnson Blvd.
Colorado Springs, Colorado 80920 USA
(719) 531-9444 FAX (719) 531-9481

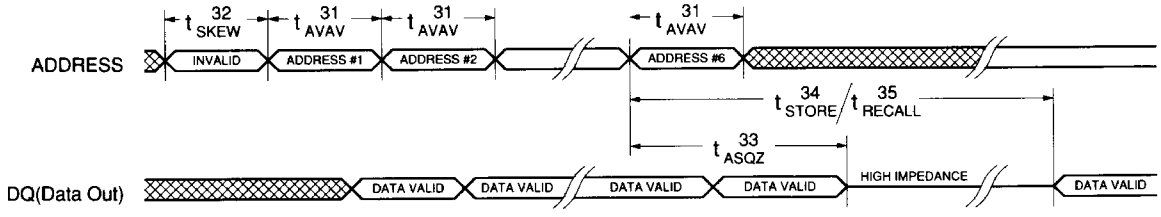
STORE/RECALL CYCLES 1 & 2[p,u]

(-55°C≤T_A≤125°C) (V_{CC}=5.0V ±10%)

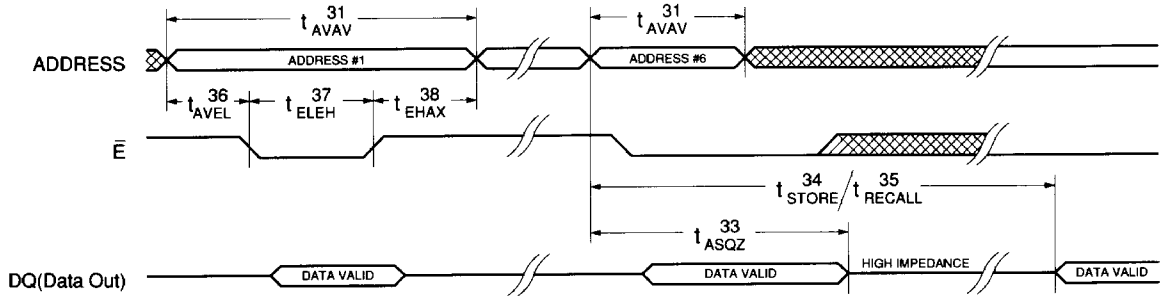
NO.	SYMBOL		PARAMETER	STK11C68AM-45		STK11C68AM-55		STK11C68AM-70		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX		
31	t_{AVAV}	t_{ACS}	Read Cycle Time	45		55		70		ns	
32		t_{SKEW}	Skew Between Sequentially Adjacent Address Pins		5		5		5	ns	o
33		t_{ASQZ}	Address Sequence to Output Inactive		75		75		75	ns	q
34		t_{STORE}	Store Cycle Time		11		11		11	ms	r
35		t_{RECALL}	Recall Cycle Time		40		40		40	µs	r
36	t_{AVEL}	t_{AE}	Address Set-up to Chip Enable	0		0		0		ns	s
37	t_{ELEH}	t_{EP}	Chip Enable Pulse Width	45		55		70		ns	s
38	t_{EHAX}	t_{EA}	Chip Disable to Address Change	0		0		0		ns	s

Note o: Skew spec may be avoided by using $\overline{E}$ (STORE/RECALL CYCLE 2).
Note p: $\overline{W} \geq V_{IH}$ during entire address sequence to initiate a non-volatile cycle. Required address sequences are shown in MODE SELECTION table.
Note q: Once the software STORE or RECALL cycle is initiated, it completes automatically, ignoring all inputs.
Note r: Measured with $\overline{W}$ high and $\overline{G}$ and $\overline{E}$ low. Note that STORE cycles are aborted by V_{CC} < 3.8V (STORE Inhibit).
Note s: $\overline{E}$ must make the transition between V_{IH} (max) to V_{IL} (max), or V_{IL} (max) to V_{IH} (min) in a monotonic fashion.
Note t: Chip is continuously selected with $\overline{E}$ low.
Note u: Addresses #1 through #6 are found in the MODE SELECTION table. Address #6 determines whether the STK11C68AM performs a STORE or RECALL. A RECALL cycle is performed automatically at power up when V_{CC} exceeds 3.8V.

STORE/RECALL CYCLE 1[p,t]



STORE/RECALL CYCLE 2[p]



Simtek Corporation
1465 Kelly Johnson Blvd.
Colorado Springs, Colorado 80920 USA
(719) 531-9444 FAX (719) 531-9481

DEVICE OPERATION

The STK11C68AM has two separate modes of operation: SRAM mode and non-volatile mode. In SRAM mode the memory operates as an ordinary static RAM. In non-volatile operation, data is transferred from SRAM to EEPROM or from EEPROM to SRAM. In this mode SRAM functions are disabled.

SRAM READ

The STK11C68AM performs a read cycle whenever $\overline{E}$ and $\overline{G}$ are LOW and $\overline{W}$ is HIGH. The address specified by the 13 addresses, $A_{0\text{-}12}$ specify which of the 8192 data bytes will be accessed. If the read cycle is initiated by an address transition, the outputs will be valid at t_{AVQV} (READ CYCLE 1). If the cycle is initiated by a clock signal the outputs will be valid at t_{ELQV} or at t_{GLQV}, whichever is later (READ CYCLE 2). As long as the clocks remain in the READ state the outputs will repeatedly respond to address changes within t_{AVQV} access time without the need for additional clocking cycles. The outputs remain valid until another address change or until $\overline{E}$ or $\overline{G}$ is brought HIGH or $\overline{W}$ is brought LOW.

SRAM WRITE

A write cycle is performed whenever $\overline{E}$ and $\overline{W}$ are LOW. The address inputs must be stable prior to entering the WRITE cycle and must remain stable until either $\overline{E}$ or $\overline{W}$ go HIGH at the end of the cycle. The data on the eight inputs, $DQ_{0\text{-}7}$, will be written into the memory location specified by the address inputs. The DQ data may be changed during the write cycle. Valid data must, however, be present t_{DVWH} before the end of a $\overline{W}$ controlled WRITE or t_{DVEH} before the end of an $\overline{E}$ controlled WRITE for the memory cells to be fully written.

It is recommended that $\overline{G}$ be kept HIGH during the entire WRITE cycle to avoid data bus contention on the common I/O's. If $\overline{G}$ is left LOW however, internal circuitry will turn off the output buffers t_{WHQZ} after $\overline{W}$ goes LOW. Until that time, data bus contention is possible.

NON-VOLATILE STORE

The STK11C68AM STORE cycle is initiated by executing sequential READ cycles from six specific address locations. By relying on READ cycles only, the STK11C68AM implements non-volatile operation while remaining pin-for-pin compatible with standard 8K×8 SRAM's. During the STORE cycle, an erase of the previous non-volatile data is first performed, followed by a program of the non-volatile elements. The program operation copies the SRAM data into non-volatile storage. Once a STORE cycle is initiated, further input and output are disabled until the cycle is completed.

Because a sequence of addresses is used for STORE initiation, it is critical that no invalid address states intervene in the sequence or the sequence will be aborted. The maximum skew between address inputs $A_{0\text{-}12}$ for each address state is t_{SKEW} (STORE CYCLE 1). If t_{SKEW} is exceeded it is possible that the transitional data state will be interpreted as a valid address and the sequence will be aborted. If $\overline{E}$ controlled READ cycles are used for the sequence (STORE CYCLE 2), address skew is no longer a concern.

To enable the STORE cycle the following READ sequence must be performed:

1.	Read address	0000 (hex)	Valid READ
2.	Read address	1555 (hex)	Valid READ
3.	Read address	0AAA (hex)	Valid READ
4.	Read address	1FFF (hex)	Valid READ
5.	Read address	10F0 (hex)	Valid READ
6.	Read address	0F0F (hex)	Initiate STORE Cycle

Once the sixth address in the sequence has been entered, the STORE cycle will commence and the chip will be disabled. It is important that READ cycles and not WRITE cycles be used in the sequence, although it is not necessary that $\overline{G}$ be LOW for the sequence to be valid. After the t_{ASQV} cycle time has been fulfilled, the SRAM will again be activated for READ and WRITE operation.

HARDWARE PROTECT

The STK11C68AM offers hardware protection against inadvertent STORE cycles through V_{CC} Sense. A STORE cycle will not be initiated, and one in progress will discontinue, if V_{CC} goes below 3.8V.

NON-VOLATILE RECALL

A RECALL of the EEPROM data into the SRAM is initiated with a sequence of READ operations in a manner similar to the STORE initiation. To initiate the RECALL cycle the following sequence of READ operations must be performed:

1.	Read address	0000 (hex)	Valid READ
2.	Read address	1555 (hex)	Valid READ
3.	Read address	0AAA (hex)	Valid READ
4.	Read address	1FFF (hex)	Valid READ
5.	Read address	10F0 (hex)	Valid READ
6.	Read address	0F0E (hex)	Initiate RECALL Cycle

Internally, RECALL is a two step procedure. First, the SRAM data is cleared and second, the non-volatile information is transferred into the SRAM cells. The RECALL operation in no way alters the data in the EEPROM cells. The non-volatile data can be recalled an unlimited number of times.

On power-up, once V_{CC} exceeds the V_{CC} sense voltage of 3.8V, a RECALL cycle is automatically initiated. For this reason, SRAM operation cannot commence until t_{RECALL} after V_{CC} is high.

Simtek Corporation
1465 Kelly Johnson Blvd.
Colorado Springs, Colorado 80920 USA
(719) 531-9444 FAX (719) 531-9481

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1465 Kelly Johnson Blvd.
Colorado Springs, Colorado 80920 USA
(719) 531-9444 FAX (719) 531-9481

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