MOTOROLA

Military 54LS126A

Quad Bus Buffer Gate
Non-Inverting Control Input

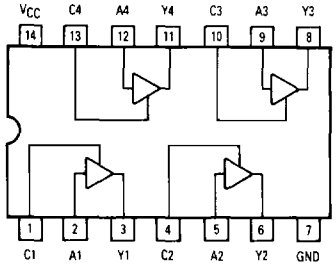
ELECTRICALLY TESTED PER:
MIL-M-38510/32302

AVAILABLE AS:

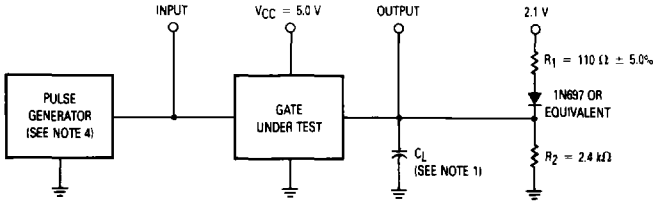
1) JAN: JM38510/32302BXA
2) SMD: *
3) 883C: 54LS126A/BXAJC

X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: C
CERFLAT: D
LCC: 2
***Call Factory for latest update**

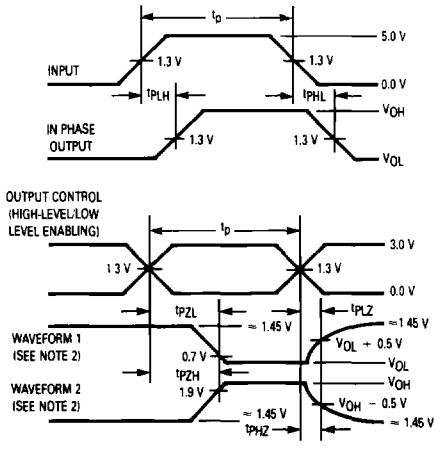
LOGIC DIAGRAM



AC TEST CIRCUIT



WAVEFORMS



PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION A)
C1	1	1	2	V_{CC}
A1	2	2	3	V_{CC}
Y1	3	3	4	V_{CC}
C2	4	4	6	V_{CC}
A2	5	5	8	V_{CC}
Y2	6	6	9	V_{CC}
GND	7	7	10	GND
Y3	8	8	12	V_{CC}
A3	9	9	13	V_{CC}
C3	10	10	14	V_{CC}
Y4	11	11	16	V_{CC}
A4	12	12	18	V_{CC}
C4	13	13	19	V_{CC}
V_{CC}	14	14	20	V_{CC}

BURN-IN CONDITIONS:
V_{CC} = 5.0 V MIN/6.0 V MAX

TRUTH TABLE

Inputs		Output
E	D	
H	L	L
H	H	H
L	X	(Z)

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = HIGH Impedance (off)

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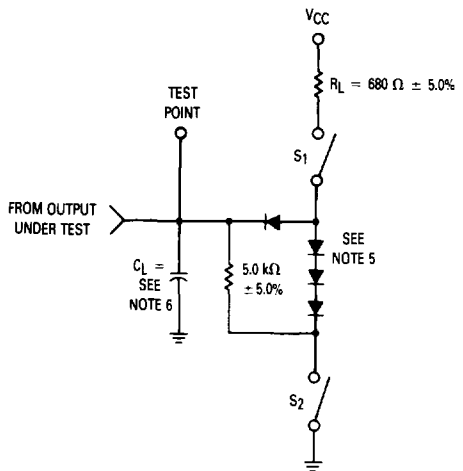
AC TEST CIRCUIT

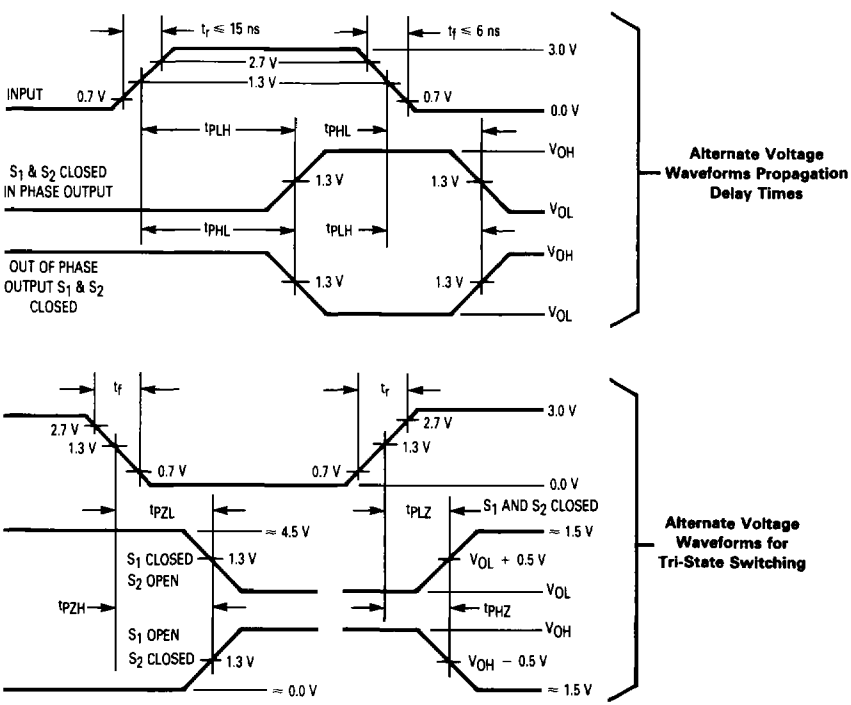
ALTERNATE LOAD CIRCUIT



Test Type	S1	S2
t_{PZH}	open	closed
t_{PZL}	closed	open
t_{PLZ}	closed	closed
t_{PHZ}	closed	closed

NOTES:
1. C_L = 50 pF ± 10% minimum for all tests. C_L includes scope probe and jig capacitance.
2. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
3. In the example, the phase relationships between inputs and outputs have been chosen arbitrarily.
4. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1.0 MHz, t_p = 500 ns, $Z_{OUT} \approx 50\ \Omega$, V_{gen} = 3.0 V and $t_r \leq 15$ ns, $t_f \leq 6.0$ ns between 0.7 V and 2.7 V.
5. Diodes are 1N3064 or equivalent (unless otherwise specified).
6. C_L = 15 pF minimum for t_{PHZ} and t_{PLZ} (for alternate load circuit).

WAVEFORMS



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Symbol	Parameter	Limits						Units	Test Condition (Unless Otherwise Specified)
		+25°C		+125°C		−55°C			
	Static Parameters:	Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V_{OH}	Logical "1" Output Voltage	2.4		2.4		2.4		V	V_{CC} = 4.5 V, I_{OH} = −1.0 mA, V_{IH} = 2.0 V (both inputs).
V_{OL}	Logical "0" Output Voltage		0.4		0.4		0.4	V	V_{CC} = 4.5 V, I_{OL} = 12 mA, V_{IL} = 0.7 V, V_{IH} = 2.0 V.
V_{IC}	Input Clamping Voltage		−1.5					V	V_{CC} = 4.5 V, I_{IN} = −18 mA, other input = 4.5 V.
I_{IH}	Logical "1" Input Current		20		20		20	μA	V_{CC} = 5.5 V, V_{IH} = 2.7 V, other input is open (or) V_{IH} = 5.5 V, other input = 2.7 V.
I_{IHH}	Logical "1" Input Current		100		100		100	μA	V_{CC} = 5.5 V, V_{IHH} = 5.5 V, other input is open (or) V_{IHH} = 5.5 V, (both inputs).
I_{IL1}	Logical "0" Input Current	−0.16	−0.4	−0.16	−0.4	−0.16	−0.4	mA	V_{CC} = 5.5 V, V_{IN} = 0.4 V, other input is open.
I_{IL2}	Logical "0" Input Current	−0.16	−0.4	−0.16	−0.4	−0.16	−0.4	mA	V_{CC} = 5.5 V, V_{IN} = 5.5 V, other input = 0.4 V.
I_{OS}	*Output Short* Circuit Current	−40	−225	−40	−225	−40	−225	mA	V_{CC} = 5.5 V, V_{IN} = 4.5 V *(both inputs)*, V_{OUT} = GND.
I_{IOZH}	Output Off Current High		20		20		20	μA	V_{CC} = 5.5 V, V_{IN} = 0.7 V (both inputs), V_{OUT} = 2.4 V.
I_{IOZL}	Output Off Current Low		−20		−20		−20	μA	V_{CC} = 5.5 V, V_{IN} = 2.0 V, other input = 0.7 V, V_{OUT} = 0.4 V.
I_{CC}	Power Supply Current Off		22		22		22	mA	V_{CC} = 5.5 V, V_{IN} = GND (all inputs).
V_{IH}	Logical "1" Input Voltage	2.0		2.0		2.0		V	V_{CC} = 4.5 V.
V_{IL}	*Logical "0"* Input Voltage		0.7		0.7		0.7	V	V_{CC} = 4.5 V.
		Subgroup 7		Subgroup 8A		Subgroup 8B			
	Functional Tests								per Truth Table with V_{CC} = 5.0 V, V_{INL} = 0.4 V, and V_{INH} = 2.4 V.

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Symbol	Parameter	Limits						Units	Test Condition (Unless Otherwise Specified)
	Switching Parameters	+25°C		+125°C		−55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t_{PHL1} t_{PHL1}	Propagation Delay /Data-Output Output High-Low	2.0	18 18	2.0	24 19	2.0	24 19	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_1 = 110 Ω, R_2 = 2.4 kΩ. V_{CC} = 5.0 V, C_L = 45 pF, R_L = 667 Ω.
t_{PLH1} t_{PLH1}	Propagation Delay /Data-Output Output Low-High	2.0	15 15	2.0	20 15	2.0	20 15	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_1 = 110 Ω, R_2 = 2.4 kΩ. V_{CC} = 5.0 V, C_L = 45 pF, R_L = 667 Ω
t_{PLZ1} t_{PLZ1}	Propagation Delay /Data-Output Output Low-High	2.0	30 25	2.0	39 34	2.0	39 34	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_1 = 110 Ω, R_2 = 2.4 kΩ. V_{CC} = 5.0 V, C_L = 45 pF, R_L = 667 Ω
t_{PHZ1} t_{PHZ1}	Propagation Delay /Data-Output Output High-Low	2.0	42 25	2.0	48 43	2.0	48 43	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_1 = 110 Ω, R_2 = 2.4 kΩ. V_{CC} = 5.0 V, C_L = 45 pF, R_L = 667 Ω
t_{PZL1} t_{PZL1}	Propagation Delay /Data-Output Output Low-High	2.0	35 35	2.0	46 41	2.0	46 41	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_1 = 110 Ω, R_2 = 2.4 kΩ. V_{CC} = 5.0 V, C_L = 45 pF, R_L = 667 Ω
t_{PZH1} t_{PZH1}	Propagation Delay /Data-Output Output High-Low	2.0	25 25	2.0	33 28	2.0	33 28	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_1 = 110 Ω, R_2 = 2.4 kΩ. V_{CC} = 5.0 V, C_L = 45 pF, R_L = 667 Ω