Integrated Device Technology, Inc.

FAST CMOS OCTAL TRANSCEIVER/ REGISTER

PRELIMINARY
IDT 54/74FCT651/A
IDT 54/74FCT652/A

T-52-31

FEATURES:

- IDT54/74FCT651 and IDT54/74FCT652 are equivalent to FAST™ speeds
- **IDT54/74FCT651A and IDT54/74FCT652A 30% faster than FAST™ speeds**
- Bidirectional bus transceiver and registers
- Independent registers for A and B buses
- Real-time data transfer or stored data transfer
- Choice of true and inverting data transfer
- 3-state outputs
- I_{OL} = 64mA (commercial) and 48mA (military)
- CMOS power levels (5μW typ. static)
- TTL input and output level compatible
- CMOS output level compatible
- Available in 24-pin 300 mil DIP, SOIC, 28-pin LCC and PLCC
- Product available in Radiation Tolerant and Enhanced versions
- Military product compliant to MIL-STD-883, Class B

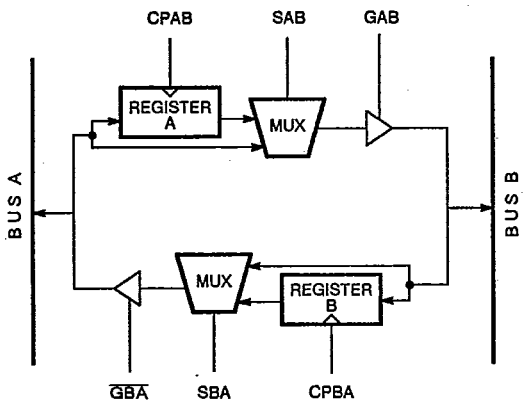
DESCRIPTION:

The IDT54/74FCT651/A and IDT54/74FCT652/A, built in CEMOS™, consist of bus transceiver circuits, D-type flip-flops and control circuitry arranged for multiplex transmission of data directly from the data bus or from the internal storage registers. GAB and $\overline{GBA}$ are provided to control the transceiver functions. SAB and SBA control pins are provided to select either real-time or stored data transfer. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. A low input level selects real-time data and a high selects stored data.

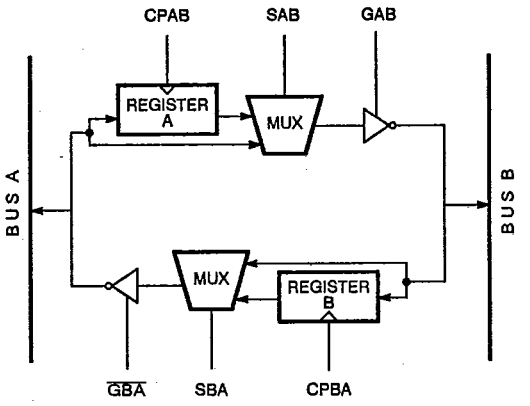
Data on the A or B data bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock pins (CPAB or CPBA), regardless of the select or enable control pins. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling GAB and $\overline{GBA}$. In this configuration, each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines will remain at its last state.

FUNCTIONAL BLOCK DIAGRAM

IDT54/74FCT652/A (Non-Inverting)



IDT54/74FCT651/A (Inverting)



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FAST is a trademark of Fairchild Semiconductor Co.

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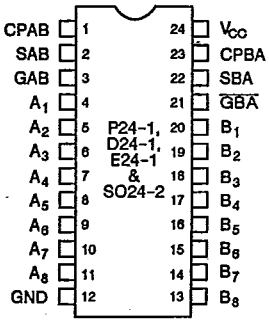
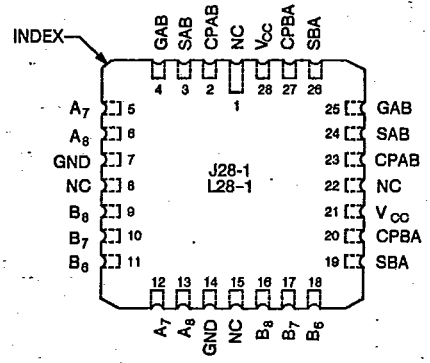
PIN CONFIGURATIONS

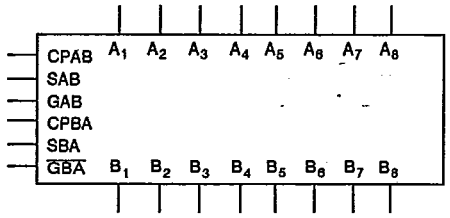


DIP/CERPACK/SOIC
TOP VIEW



LCC/PLCC
TOP VIEW

LOGIC SYMBOL



PIN DESCRIPTION

PIN NAMES	DESCRIPTION
A_1-A_8	Data Register Inputs Data Register A Outputs
B_1-B_8	Data Register B Inputs Data Register B Outputs
CPAB, CPBA	Clock Pulse Inputs
SAB, SBA	Transmit/Receive Inputs
GAB, $\overline{GBA}$	Output Enable Inputs

FUNCTION TABLE

INPUTS						DATA I/O		OPERATION OR FUNCTION	
GAB	$\overline{GBA}$	CPAB	CPBA	SAB	SBA	A_1 THRU A_8	B_1 THRU B_8	FCT651/A	FCT652/A
L	H	H or L	H or L	X	X	Input	Input	Isolation	Isolation
L	H	↑	↑	X	X			Store A and B Data	Store A and B Data
X	H	↑	H or L	X	X	Input	Unspecified[1]	Store A, Hold B	Store A, Hold B
H	H	↑	↑	X[2]	X	Input	Output	Store A in both registers	Store A in both registers
L	X	H or L	↑	X	X	Unspecified[1]	Input	Hold A, Store B	Hold A, Store B
L	L	↑	↑	X	X[2]	Output	Input	Store B in both registers	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-Time $\overline{B}$ Data to A Bus	Real-Time B Data to A Bus
L	L	X	H or L	X	H			Stored $\overline{B}$ Data to A Bus	Stored B Data to A Bus
H	H	X	X	L	X	Input	Output	Real-Time $\overline{A}$ Data to B Bus	Real-Time A Data to B Bus
H	H	H or L	X	H	X			Stored $\overline{A}$ Data to B Bus	Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored $\overline{A}$ Data to B Bus and Stored $\overline{B}$ Data to A Bus	Stored A Data to B Bus and Stored B Data to A Bus

NOTES:

1. The data output functions may be enabled or disabled by various signals at the GAB or $\overline{GBA}$ inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.
2. Select control = L: clocks can occur simultaneously.
   Select control = H: clocks must be staggered in order to load both registers.

H = HIGH, L = LOW, X = Don't Care, ↑ LOW-to-HIGH Transition

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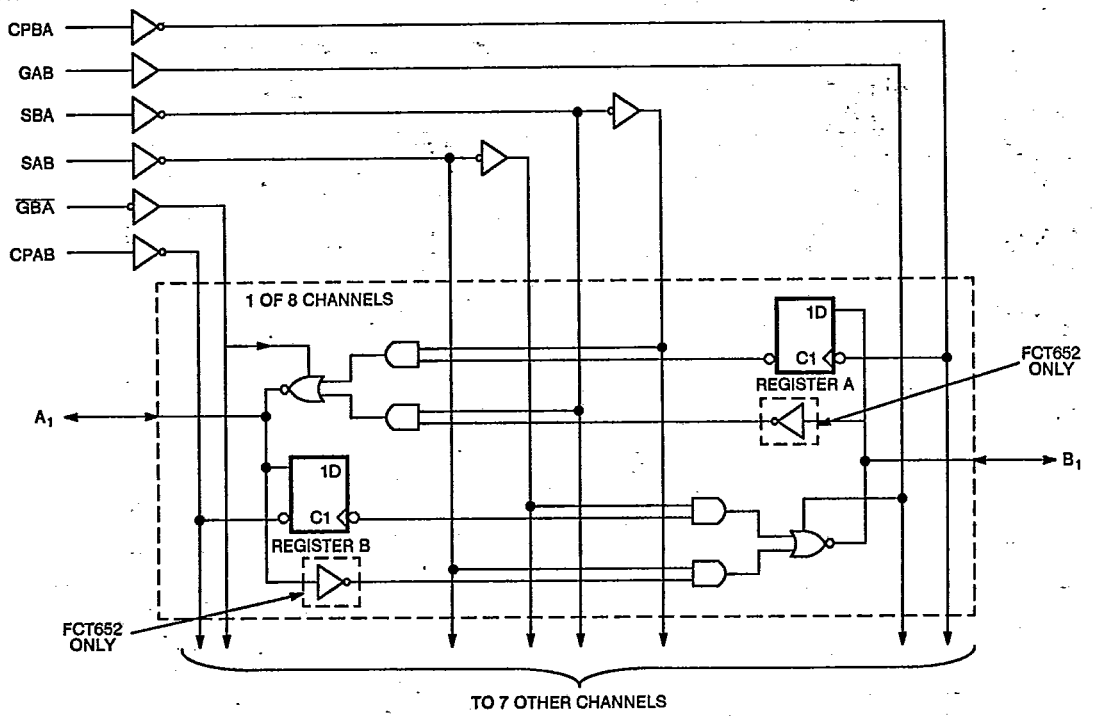
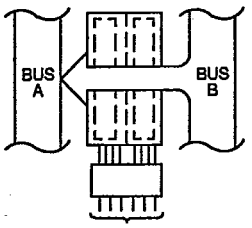
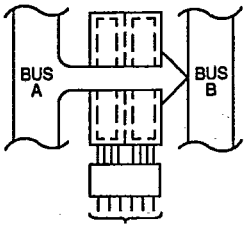
DETAILED BLOCK DIAGRAM





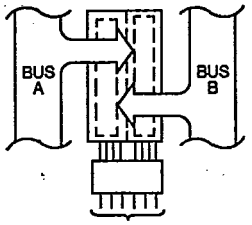
GAB	GBA	CPAB	CPBA	SAB	SBA
L	L	X	X	X	L

REAL-TIME TRANSFER
BUS B TO BUS A



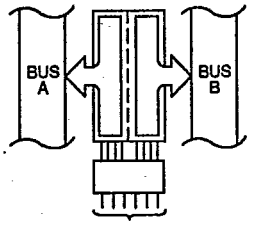
GAB	GBA	CPAB	CPBA	SAB	SBA
H	H	X	X	L	X

REAL-TIME TRANSFER
BUS A TO BUS B



GAB	GBA	CPAB	CPBA	SAB	SBA
X	H	↑	X	X	X
L	X	X	↑	X	X
L	H	↑	↑	X	X

STORAGE FROM
A AND/OR B



GAB	GBA	CPAB	CPBA	SAB	SBA
H	L	H or L	H or L	H	H

TRANSFER
STORED DATA
TO A AND/OR B

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ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM} (2)	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
V_{TERM} (3)	Terminal Voltage with Respect to GND	-0.5 to V_{CC}	-0.5 to V_{CC}	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Input and V_{CC} terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:

1. This parameter is guaranteed by characterization data and not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V
Commercial: T_A = 0°C to +70°C; V_{CC} = 5.0V±5%
Military: T_A = -55°C to +125°C; V_{CC} = 5.0V±10%

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		–	–	0.8	V
I_{IH}	Input HIGH Current (Except I/O pins)	V_{CC} = Max.	V_I = V_{CC}	–	–	5	µA
			V_I = 2.7V	–	–	5(4)	
I_{IL}	Input LOW Current (Except I/O pins)		V_I = 0.5V	–	–	-5(4)	
			V_I = GND	–	–	-5	
I_{IH}	Input HIGH Current (I/O pins only)	V_{CC} = Max.	V_I = V_{CC}	–	–	15	µA
			V_I = 2.7V	–	–	15(4)	
I_{IL}	Input LOW Current (I/O pins only)		V_I = 0.5V	–	–	-15(4)	
			V_I = GND	–	–	-15	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = -18mA		–	-0.7	-1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.(3), V_O = GND		-60	-120	–	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32 µA		V_{HC}	V_{CC}	–	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	–	
			I_{OH} = -12mA MIL.	2.4	4.3	–	
			I_{OH} = -15mA COM'L.	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		–	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	–	GND	V_{LC}	
			I_{OL} = 48mA MIL.	–	0.3	0.55	
			I_{OL} = 64mA COM'L.	–	0.3	0.55	
V_H	Input Hysteresis on Clock Only	–		–	200	–	mV

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.
5. These are maximum I_{OL} values per output, for 8 outputs turned on simultaneously. Total maximum I_{OL} (all outputs) is 512mA for commercial and 384mA for military. Derate I_{OL} for number of outputs turned on simultaneously.

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POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} – 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ $f_{CP} = f_i = 0$		–	0.001	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		–	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open GAB = GND $\overline{GBA}$ = GND SAB = CPAB = GND SBA = V_{CC} One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	–	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle GAB = GND $\overline{GBA}$ = GND SAB = CPAB = GND SBA = V_{CC} One Bit Toggling at f_i = 5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	1.5	4.0	mA
			V_{IN} = 3.4V or V_{IN} = GND	–	2.0	6.0	
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle GAB = GND $\overline{GBA}$ = GND SAB = CPAB = GND SBA = V_{CC} Eight Bits Toggling at f_i = 2.5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	3.75	7.8[5]	
			V_{IN} = 3.4V or V_{IN} = GND	–	6.0	16.8[5]	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

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SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION[1]	IDT54/74FCT651/652					IDT54/74FCT651A/652A					UNIT
			TYP.[3]	COM'L.		MIL.		TYP.[3]	COM'L.		MIL.		
				MIN.[2]	MAX.	MIN.[2]	MAX.		MIN.[2]	MAX.	MIN.[2]	MAX.	
t_{PLH} t_{PHL}	Propagation Delay Bus to Bus	C_L = 50pF R_L = 500Ω	8.0	2.0	9.0	2.0	10.0	–	–	–	–	–	ns
t_{PLH} t_{PHL}	Propagation Delay Clock to Bus		8.0	2.0	9.0	2.0	11.0	–	–	–	–	–	ns
t_{PLH} t_{PHL}	Propagation Delay SBA or SAB to A or B		10.0	2.0	11.0	2.0	12.0	–	–	–	–	–	ns
t_{PZH} t_{PZL}	Output Enable Time Enable to Bus		9.0	2.0	10.0	2.0	12.0	–	–	–	–	–	ns
t_{PHZ} t_{PLZ}	Output Disable Time Enable to Bus		9.0	2.0	10.0	2.0	12.0	–	–	–	–	–	ns
t_{SU}	Set-up Time HIGH or LOW Bus to Clock		3.0	4.0	–	4.5	–	–	–	–	–	–	ns
t_H	Hold Time HIGH or LOW Bus to Clock		1.0	2.0	–	2.0	–	–	–	–	–	–	ns
t_W	Pulse Width, HIGH or LOW		4.0	6.0	–	6.0	–	–	–	–	–	–	ns

NOTES:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.

ORDERING INFORMATION

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IDTXXFCT XXX Device Type X Package X Process/Temperature

Blank	Commercial
B	Compliant to MIL-STD-883, Class B
P	Plastic DIP
D	CERDIP
E	CERPACK
J	Plastic Leadless Chip Carrier
L	Leadless Chip Carrier
SO	Small Outline IC
651	Inverting Octal Transceiver/Register
652	Non-Inverting Octal Transceiver/Register
651A	Inverting Fast Octal Transceiver/Register
652A	Non-Inverting Fast Octal Transceiver/Register
54	-55°C to +125°C
74	0°C to +70°C