SN54AS29823, SN54AS29824, SN74AS29823, SN74AS29824
9-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

D2910, MAY 1986

- **Designed to be Interchangeable with AMD AM29823 and AM29824**
- **Ideal for Data Synchronization of Wider Data Paths**
- **Provides Extra Data Width Necessary for Wider Address/Data Paths or Buses with Parity**
- **Outputs Have Undershoot Protection Circuitry**
- **Power-Up High-Impedance State**
- **Buffered Control Inputs to Reduce DC Loading Effects**
- **Package Options Include Plastic "Small Outline" Packages, Both Plastic and Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

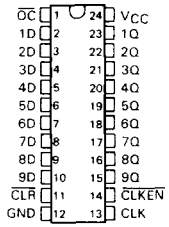
description

These 9-bit flip-flops feature three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. They are particularly suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers, parity bus interfacing and working registers.

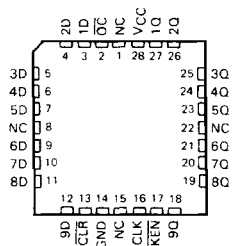
With the clock enable ($\overline{CLKEN}$) low, the nine D-type edge-triggered flip-flops enter data on the low-to-high transitions of the clock. Taking $\overline{CLKEN}$ high will disable the clock buffer, thus latching the outputs. The 'AS29823 has noninverting D inputs and the 'AS29824 has inverting $\overline{D}$ inputs. Taking the $\overline{CLR}$ input low causes the nine Q outputs to go low independently of the clock.

The buffered output-control input ($\overline{OC}$) can be used to place the nine outputs in either a normal logic state (high or low levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components. The output control does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

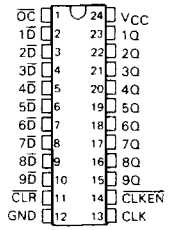
SN54AS29823 . . . JT PACKAGE
SN74AS29823 . . . DW or NT PACKAGE
(TOP VIEW)



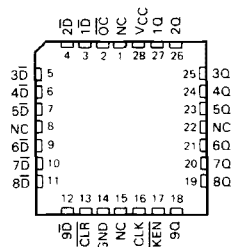
SN54AS29823 . . . FK PACKAGE
SN74AS29823 . . . FN PACKAGE
(TOP VIEW)



SN54AS29824 . . . JT PACKAGE
SN74AS29824 . . . DW or NT PACKAGE
(TOP VIEW)



SN54AS29824 . . . FK PACKAGE
SN74AS29824 . . . FN PACKAGE
(TOP VIEW)



NC No internal connection

The SN54AS29823 and SN54AS29824 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74AS29823 and SN74AS29824 are characterized for operation from 0°C to 70°C.

FUNCTION TABLES

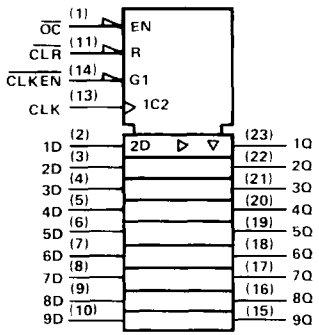
'AS29823

INPUTS					OUTPUT
$\overline{OC}$	$\overline{CLR}$	$\overline{CLKEN}$	CLK	D	Q
L	L	X	X	X	L
L	H	L	↑	H	H
L	H	L	↑	L	L
L	H	H	X	X	Q_O
H	X	X	X	X	Z

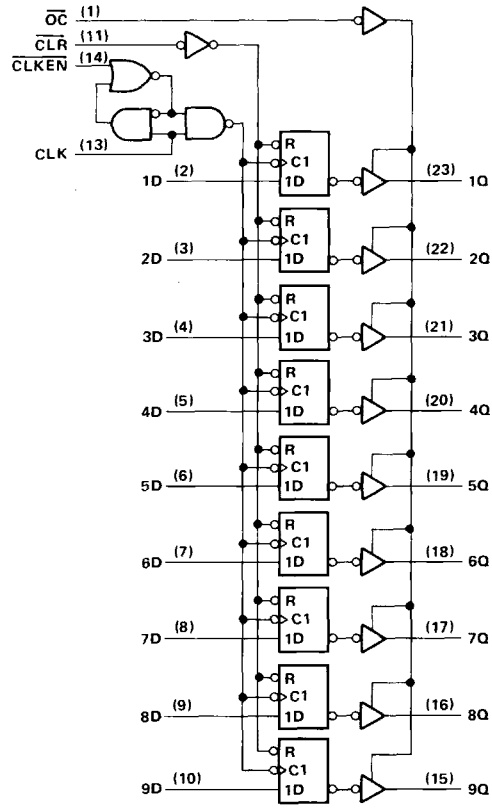
'AS29824

INPUTS					OUTPUT
$\overline{OC}$	$\overline{CLR}$	$\overline{CLKEN}$	CLK	$\overline{D}$	Q
L	L	X	X	X	L
L	H	L	↑	H	L
L	H	L	↑	L	H
L	H	H	X	X	Q_O
H	X	X	X	X	Z

'AS29823 logic symbol†



'AS29823 logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

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FUNCTION TABLES

'AS29823

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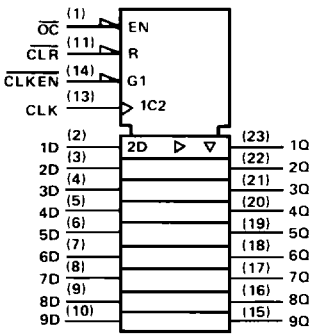
$\overline{OC}$	$\overline{CLR}$	$\overline{CLKEN}$	CLK	D	Q
L	L	X	X	X	L
L	H	L	↑	H	H
L	H	L	↑	L	L
L	H	H	X	X	Q_0
H	X	X	X	X	Z

'AS29824

INPUTS					OUTPUT
$\overline{OC}$	$\overline{CLR}$	$\overline{CLKEN}$	CLK	$\overline{D}$	Q
L	L	X	X	X	L
L	H	L	↑	H	L
L	H	L	↑	L	H
L	H	H	X	X	Q_0
H	X	X	X	X	Z

'AS29823 logic symbol†



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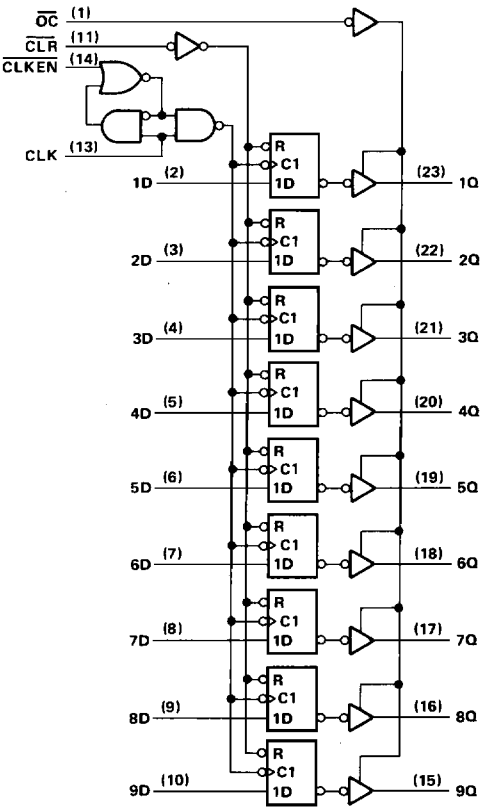

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for DW, JT, and NT packages.