MCP1811A/11B/12A/12B

Ultra-Low Quiescent Current LDO Regulator for Long-Life Battery-Powered Applications

Features

- Ultra-Low Quiescent Current: 250 nA (typical)
- Ultra-Low Shutdown Supply Current:
  - 10 nA typical for MCP1811A/12A
  - 5 nA typical for MCP1811B/12B
- Output Current Capability:
  - 150 mA for MCP1811X **(Note 1)**
  - 300 mA for MCP1812X
- Input Voltage Range: 1.8V to 5.5V
- Standard Output Voltages (V_R): 1V, 1.2V, 1.8V, 2.0V, 2.5V, 2.8V, 3.0V, 3.3V and 4.0V; for any other voltage options (between 1V to 4V), please contact your local sales office
- Stable with Ceramic Output Capacitor: 1.0 µF (MCP1811X) and 2.2 µF (MCP1812X)
- Overcurrent Protection
- Output Discharge (Shutdown mode, $\overline{SHDN}$ = GND) MCP1811A/12A
- Available for the Following Packages:
  - 3-Lead SOT-23
  - 3-Lead SC70
  - 4-Lead 1 x 1 mm UDFN
  - 5-Lead SOT-23
  - 5-Lead SC70

Applications

- Energy Harvesting
- Long-Life, Battery-Powered Applications
- Smart Cards
- Ultra-Low Consumption “Green” Products
- Wearable Electronics (smart watches, bracelets, headsets)
- Medical Devices (hearing aids)

Description

The MCP1811X/12X devices are 150 mA (MCP1811X) and 300 mA (MCP1812X) Low-Dropout (LDO) linear regulators that provide high-current and low-output voltages while maintaining an ultra-low 250 nA of quiescent current during device operation. In addition, the MCP1811B/12B can be shut down for 5 nA (typical) supply current draw.

The MCP1811X/12X family comes in nine standard fixed output voltage versions: 1V, 1.2V, 1.8V, 2.0V, 2.5V, 2.8V, 3.0V, 3.3V and 4.0V.

The 150/300 mA output current capability, combined with the low output voltage capability, make the MCP1811X/12X device family a good choice for new ultra-long life LDO applications that have high-current demands, but require ultra-low power consumption during Sleep periods.

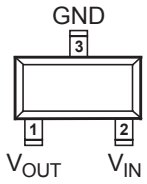
The MCP1811X/12X devices are stable with ceramic output capacitors that inherently provide lower output noise, and reduce the size and cost of the entire regulator solution. Only 1 µF (2.2 µF for MCP1812X) of output capacitance is needed to assure the stability of the system with a low noise output.

The MCP1811X/12X family can be paired with other ultra-low current devices, such as Microchip’s eXtreme Low-Power (XLP) technology devices, for a complete ultra-low power solution.

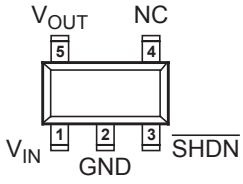
Note 1: The MCP1811X and MCP1812X designations refer to MCP1811A/11B and MCP1812A/12B, respectively.

Package Types

3-Lead SOT-23/SC70

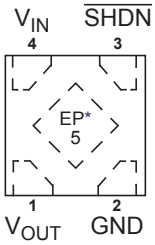


5-Lead SOT-23/SC70



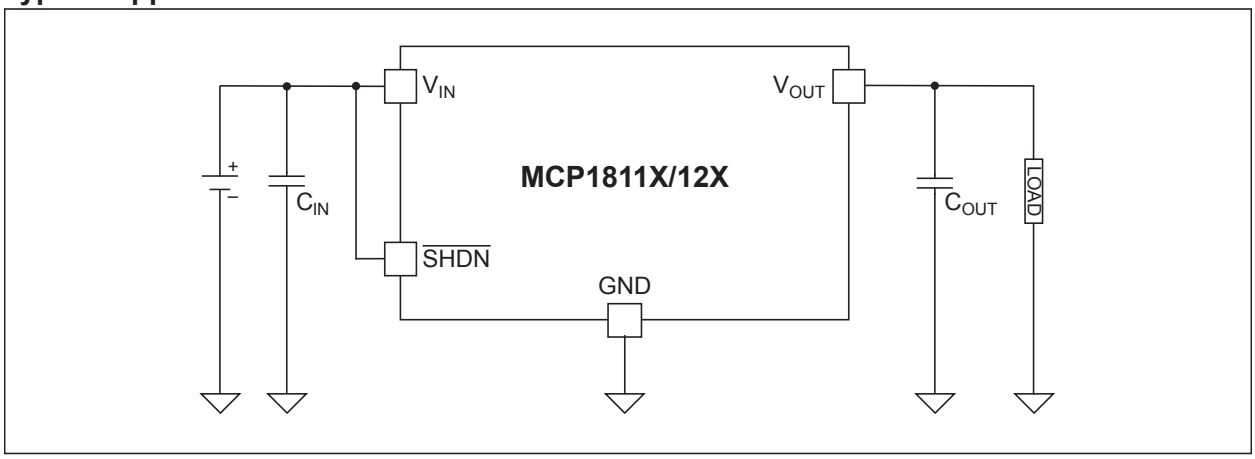
Top View

4-Lead 1x1 mm UDFN



* Includes Exposed Thermal Pad (see Table 3-1).

Typical Application



Functional Block Diagram

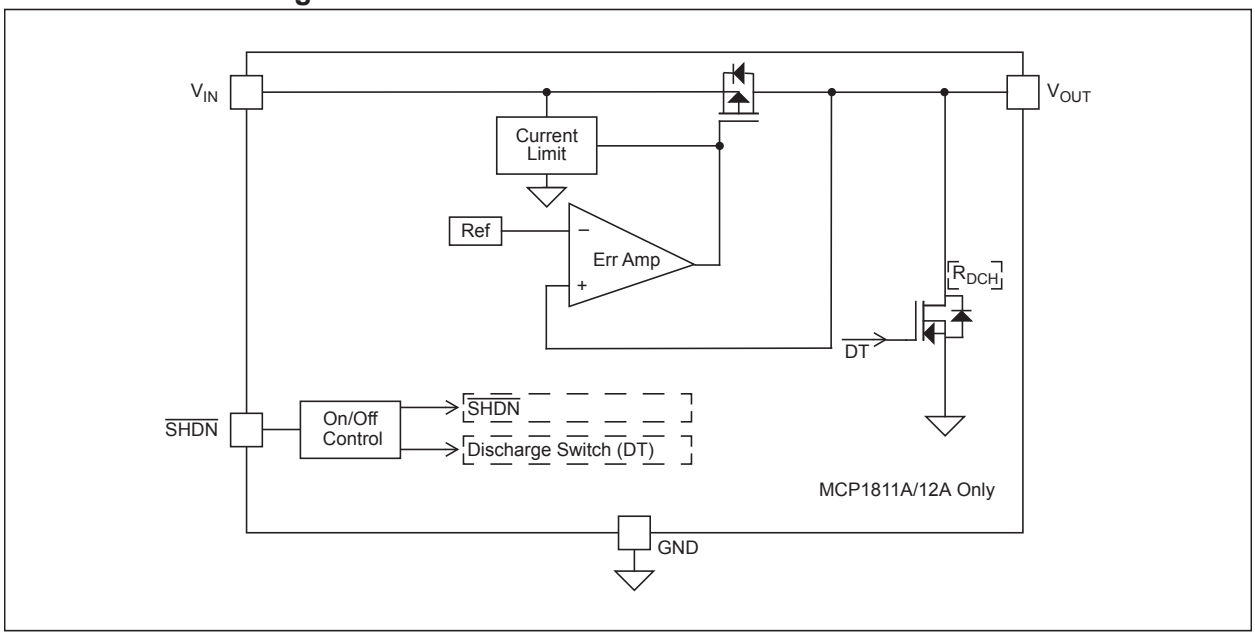


TABLE 1: MCP1811X/12X FAMILY MEMBERS

Device	Description
MCP1811A	Ultra-Low Quiescent Current LDO Regulator with Output Discharge and 150 mA Output Current
MCP1811B	Ultra-Low Quiescent Current LDO Regulator with No Output Discharge and 150 mA Output Current
MCP1812A	Ultra-Low Quiescent Current LDO Regulator with Output Discharge and 300 mA Output Current
MCP1812B	Ultra-Low Quiescent Current LDO Regulator with No Output Discharge and 300 mA Output Current

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

Input Voltage, V_{IN} ..... +6.0V
Maximum Voltage on Any Pin ..... GND – 0.3V to V_{IN} + 0.3V
Output Short-Circuit Duration ..... Unlimited **(Note 1)**
Storage Temperature ..... -55°C to +150°C
Maximum Junction Temperature, T_J ..... +125°C
Operating Junction Temperature, T_J ..... -40°C to +85°C
ESD Protection on All Pins (HBM) ..... ≥ 4 kV

† Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

AC/DC CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, $V_{IN} = V_R + 1V$ **(Note 2)**, $I_{OUT} = 1$ mA, $C_{IN} = C_{OUT} = 1$ µF (MCP1811X) or 2.2 µF (MCP1812X) ceramic (X7R), $T_A = +25°C$, $\overline{SHDN} > 1.4V$.
Boldface type applies for junction temperatures T_J of -40°C to +85°C **(Note 4)**.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Input Operating Voltage	V_{IN}	**1.8**	—	**5.5**	V	I_{OUT} ≤ 50 mA (MCP1811X, MCP1812X)
		2.0	—	**5.5**	V	I_{OUT} ≤ 150 mA (MCP1811X, MCP1812X)
		2.4	—	**5.5**	V	I_{OUT} ≤ 300 mA (MCP1812X)
Output Voltage Range	V_{OUT}	**V_R – 4%**	V_R	**V_R + 4%**		(MCP1811X, MCP1812X) **(Note 2)**
Input Quiescent Current	I_Q	—	250	**500**	nA	I_{OUT} = 0 (MCP1811X, MCP1812X)
Input Quiescent Current for $\overline{SHDN}$ Mode	$I_{\overline{SHDN}}$	—	10	**250**	nA	$\overline{SHDN}$ = GND (MCP1811A/12A)
		—	5	**125**	nA	$\overline{SHDN}$ = GND (MCP1811B/12B)
Ground Current	I_{GND}	—	90	**110**	µA	I_{OUT} = 0 to 150 mA (MCP1811X)
		—	180	**220**		I_{OUT} = 0 to 300 mA (MCP1812X)
Maximum Continuous Output Current	I_{OUT}	**150**	—	—	mA	MCP1811X
		300	—	—		MCP1812X
Current Limit	I_{LIMIT}	—	250	**420**	mA	MCP1811X
		—	500	**840**		MCP1812X

1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the operating junction temperature to exceed the maximum +85°C rating. Sustained junction temperatures above +85°C can impact device reliability.

2: V_R is a nominal regulator output voltage. The minimum V_{IN} must meet two conditions: $V_{IN} \geq V_{IN(MIN)}$ and $V_{IN} \geq V_R + V_{DROPOUT(MAX)}$.

3: Load regulation is measured at a constant junction temperature using low duty cycle pulse testing. Load regulation is tested over a load range from 1 mA to the maximum specified output current.

4: The junction temperature is approximated by soaking the device under test at an ambient temperature equal to the desired Junction temperature. The test time is small enough such that the rise in the junction temperature over the ambient temperature is not significant.

5: Dropout voltage is defined as the input-to-output voltage differential at which the output voltage drops 2% below its nominal value that was measured with an input voltage of $V_{IN} = V_R + 1V$.

AC/DC CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise indicated, $V_{IN} = V_R + 1V$ **(Note 2)**, $I_{OUT} = 1$ mA, $C_{IN} = C_{OUT} = 1$ µF (MCP1811X) or 2.2 µF (MCP1812X) ceramic (X7R), $T_A = +25°C$, $\overline{SHDN} > 1.4V$.
Boldface type applies for junction temperatures T_J of -40°C to +85°C **(Note 4)**.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Foldback Current		—	50	—	mA	$R_{LOAD} = 1\Omega$ (MCP1811X)
		—	100	—		$R_{LOAD} = 1\Omega$ (MCP1812X)
Start-up Voltage Overshoot	V_{OVER}	—	5	**10**	$\%V_{OUT}$	V_{IN} = 0V to 5.5V
Line Regulation	ΔV_{OUT}	—	±20	—	mV	1.8V < V_{IN} < 5.5V (MCP1811X), 2.4V < V_{IN} < 5.5V (MCP1812X)
Load Regulation	ΔV_{OUT}	—	±25	—	mV	I_{OUT} = 1 mA to 150 mA (MCP1811X) **(Note 3)**
		—	±50	—		I_{OUT} = 1mA to 300 mA (MCP1812X) **(Note 3)**
Dropout Voltage	$V_{DROPOUT}$	—	400	**600**	mV	I_{OUT} = 150 mA (MCP1811X), I_{OUT} = 300 mA (MCP1812X) **(Note 5)**
Shutdown Input						
Logic High Input	$V_{SHDN-HIGH}$	**70**	—	—	$\%V_{IN}$	
Logic Low Input	$V_{SHDN-LOW}$	—	—	**20**	$\%V_{IN}$	
Shutdown Input Leakage Current	$\overline{SHDN}_{ILK}$	—	0.100	**0.500**	nA	$\overline{SHDN}$ = GND
		—	1.0	**20.0**	nA	$\overline{SHDN}$ = 5.5V
Discharge Transistor R_{DCH}		—	100	—	Ω	MCP1811A/12A
AC Performance						
Start-up Delay from $\overline{SHDN}$	T_{DELAY}	—	400	—	µs	$\overline{SHDN}$ = GND to V_{IN}, V_{OUT} = GND to $10\%V_R$, $V_{IN} = V_R + 1V$ to 5.5V
Start-up Rise Time	T_{RISE}	200	—	1000	µs	$\overline{SHDN}$ = GND to V_{IN}, $V_{OUT} = 10\%V_R$ to 95% V_R, $V_{IN} = V_R + 1V$ to 5.5V
Power Supply Ripple Rejection Ratio	PSRR	—	-50	—	dB	C_{IN} = 0 µF, $V_{IN} = V_R + 1V + V_{INAC}/2$ or $V_{IN} = V_{IN\_Min} + 1V + V_{INAC}/2$, I_{OUT} = 10 mA and Full Load, $V_{INAC} = 0.2V_{pk-pk}$, f = 1 kHz

1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the operating junction temperature to exceed the maximum +85°C rating. Sustained junction temperatures above +85°C can impact device reliability.

2: V_R is a nominal regulator output voltage. The minimum V_{IN} must meet two conditions: $V_{IN} \geq V_{IN(MIN)}$ and $V_{IN} \geq V_R + V_{DROPOUT(MAX)}$.

3: Load regulation is measured at a constant junction temperature using low duty cycle pulse testing. Load regulation is tested over a load range from 1 mA to the maximum specified output current.

4: The junction temperature is approximated by soaking the device under test at an ambient temperature equal to the desired Junction temperature. The test time is small enough such that the rise in the junction temperature over the ambient temperature is not significant.

5: Dropout voltage is defined as the input-to-output voltage differential at which the output voltage drops 2% below its nominal value that was measured with an input voltage of $V_{IN} = V_R + 1V$.

TEMPERATURE SPECIFICATIONS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Operating Junction Temperature Range	T_J	-40	—	+85	°C	Steady state
Maximum Junction Temperature	T_J	—	—	+125	°C	Transient
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 4-Lead 1x1 mm UDFN	θ_{JA}	—	91.05	—	°C/W	JEDEC standard 4-layer FR4 board with 1 oz. copper and thermal vias
	$\theta_{JC(Top)}$	—	285.89	—	°C/W	
Thermal Resistance, 3-Lead SOT-23	θ_{JA}	—	211.33	—	°C/W	JEDEC standard 4-layer FR4 board with 1 oz. copper
	$\theta_{JC(Top)}$	—	138.72	—	°C/W	
Thermal Resistance, 5-Lead SOT-23	θ_{JA}	—	184.82	—	°C/W	
	$\theta_{JC(Top)}$	—	151.05	—	°C/W	
Thermal Resistance, 3-Lead SC70	θ_{JA}	—	300.6	—	°C/W	
	$\theta_{JC(Top)}$	—	130.03	—	°C/W	
Thermal Resistance, 5-Lead SC70	θ_{JA}	—	237.83	—	°C/W	
	$\theta_{JC(Top)}$	—	144.91	—	°C/W	

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, C_{IN} = C_{OUT} = 1 µF (MCP1811X) or 2.2 µF (MCP1812X) ceramic type (X7R), I_{OUT} = 1 mA, T_A = +25°C, V_{IN} = V_R + 1V, $\overline{SHDN}$ = 1 MΩ pull-up to V_{IN}.

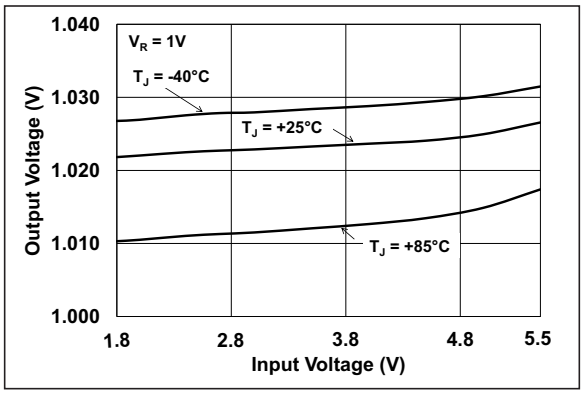


FIGURE 2-1: *Output Voltage vs. Input Voltage (MCP1811X, V_R = 1.0V).*

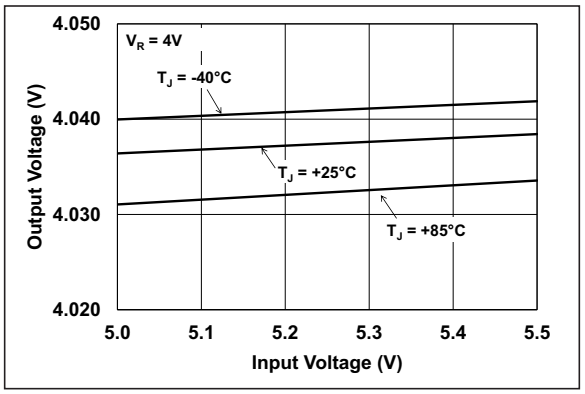


FIGURE 2-4: *Output Voltage vs. Input Voltage (MCP1811X, V_R = 4.0V).*

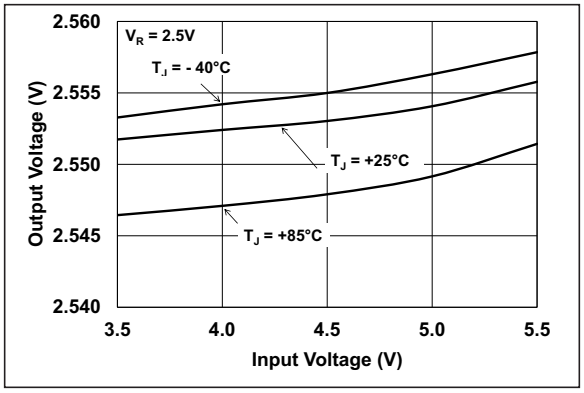


FIGURE 2-2: *Output Voltage vs. Input Voltage (MCP1812X, V_R = 2.5V).*

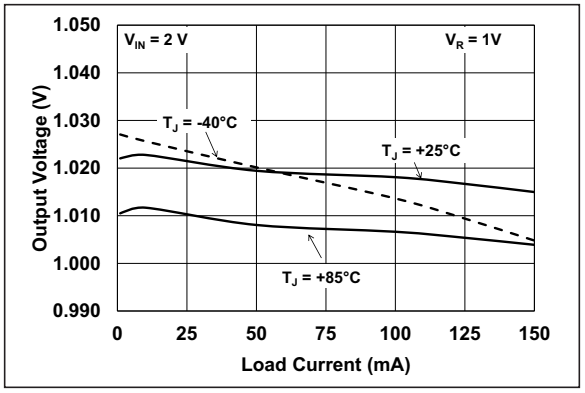


FIGURE 2-5: *Output Voltage vs. Load Current (MCP1811X, V_R = 1.0V).*

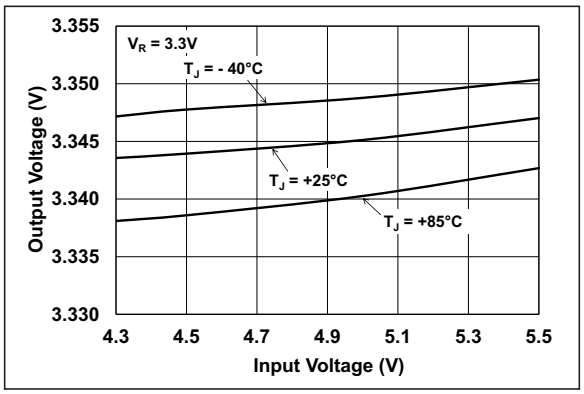


FIGURE 2-3: *Output Voltage vs. Input Voltage (MCP1812X, V_R = 3.3V).*

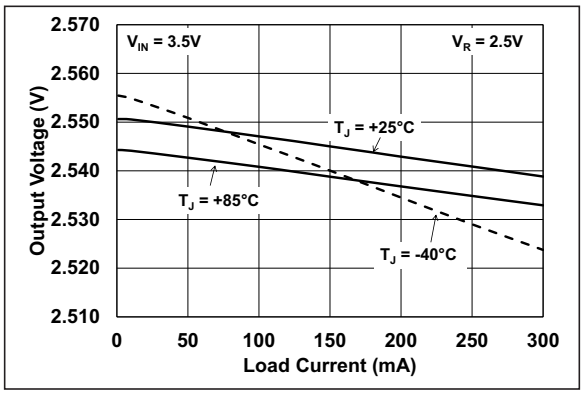


FIGURE 2-6: *Output Voltage vs. Load Current (MCP1812X, V_R = 2.5V).*

Note: Unless otherwise indicated, C_{IN} = C_{OUT} = 1 µF (MCP1811X) or 2.2 µF (MCP1812X) ceramic type (X7R), I_{OUT} = 1 mA, T_A = +25°C, V_{IN} = V_R + 1V, $\overline{SHDN}$ = 1 MΩ pull-up to V_{IN}.

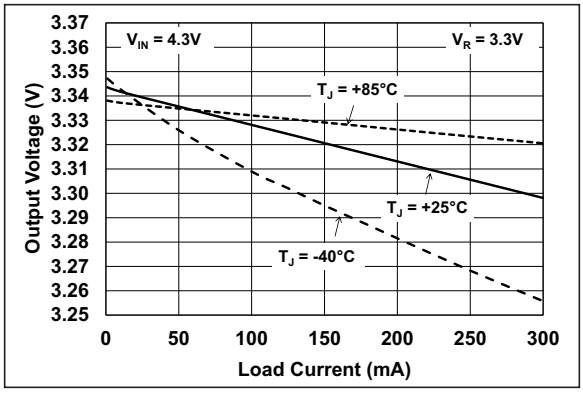


FIGURE 2-7: *Output Voltage vs. Load Current (MCP1812X, V_R = 3.3V).*

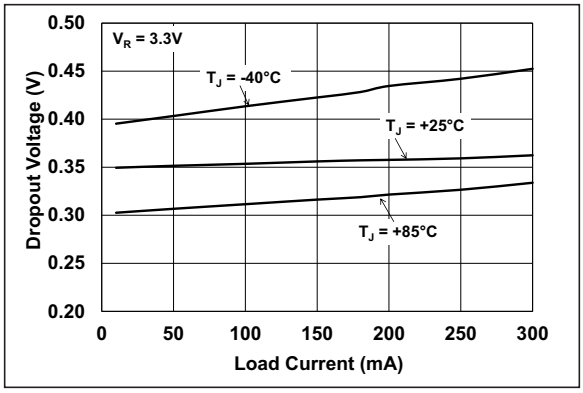


FIGURE 2-10: *Dropout Voltage vs. Load Current (MCP1812X, V_R = 3.3V).*

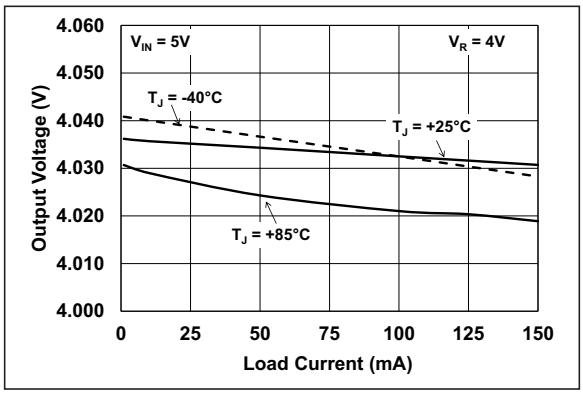


FIGURE 2-8: *Output Voltage vs. Load Current (MCP1811X, V_R = 4.0V).*

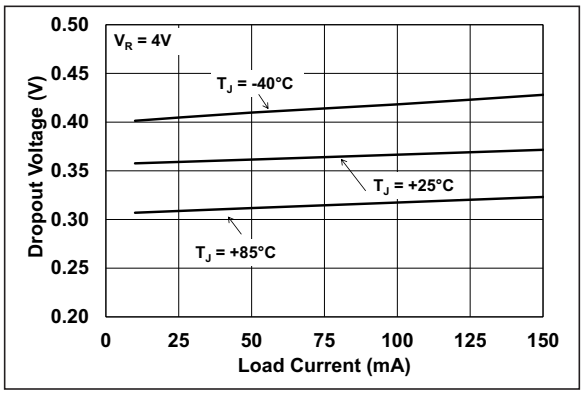


FIGURE 2-11: *Dropout Voltage vs. Load Current (MCP1811X, V_R = 4.0V).*

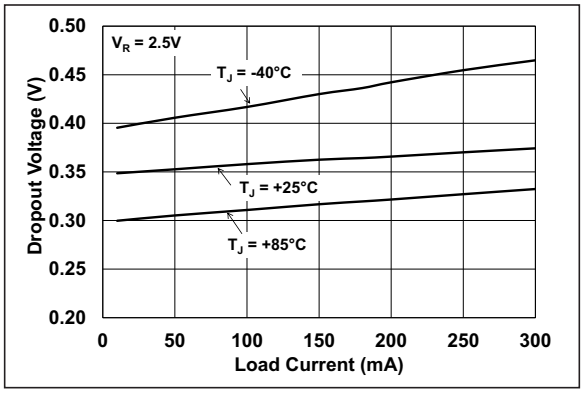


FIGURE 2-9: *Dropout Voltage vs. Load Current (MCP1812X, V_R = 2.5V)*

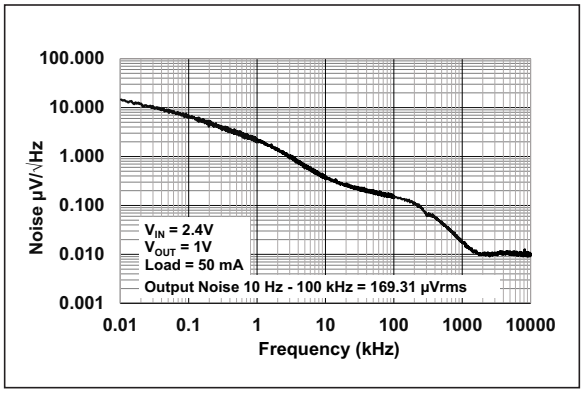


FIGURE 2-12: *Noise vs. Frequency (MCP1812X, V_R = 1.0V).*

Note: Unless otherwise indicated, C_{IN} = C_{OUT} = 1 µF (MCP1811X) or 2.2 µF (MCP1812X) ceramic type (X7R), I_{OUT} = 1 mA, T_A = +25°C, V_{IN} = V_R + 1V, $\overline{SHDN}$ = 1 MΩ pull-up to V_{IN}.

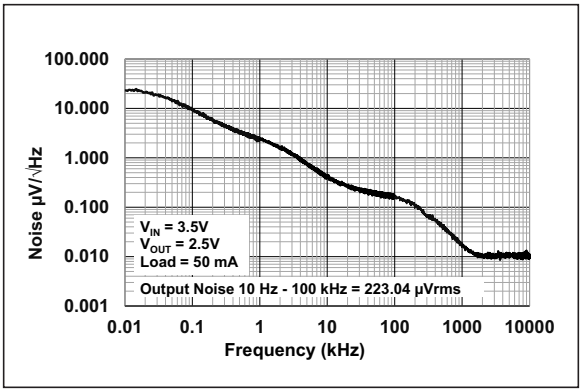


FIGURE 2-13: *Noise vs. Frequency (MCP1812X, V_R = 2.5V).*

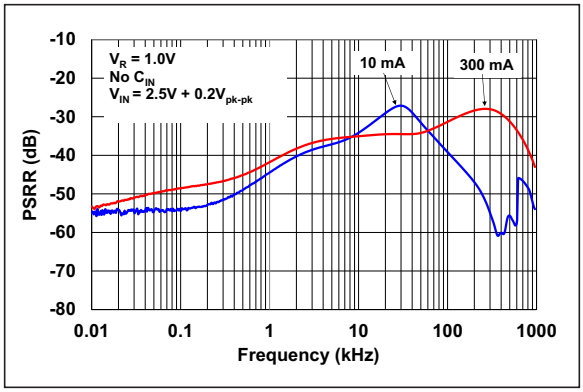


FIGURE 2-16: *Power Supply Ripple Rejection vs. Frequency (MCP1812X, V_R = 1.0V).*

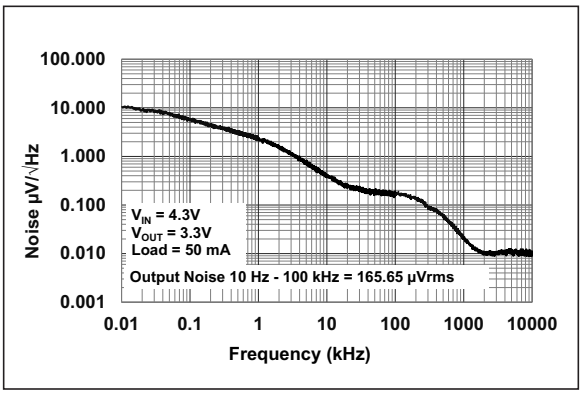


FIGURE 2-14: *Noise vs. Frequency (MCP1811X, V_R = 3.3V).*

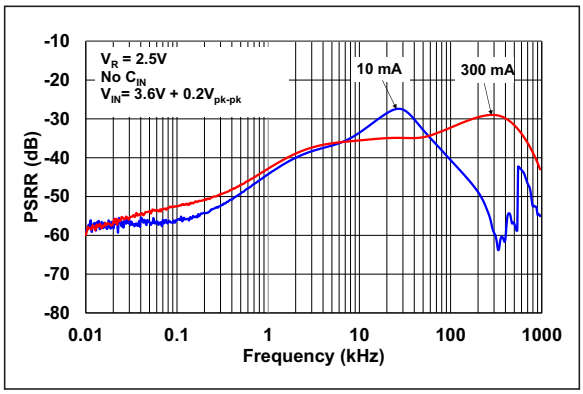


FIGURE 2-17: *Power Supply Ripple Rejection vs. Frequency (MCP1812X, V_R = 2.5V).*

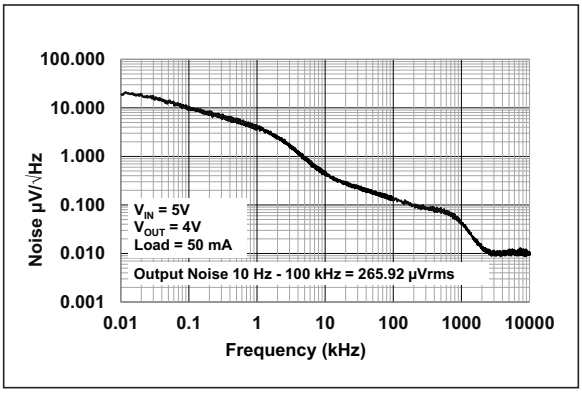


FIGURE 2-15: *Noise vs. Frequency (MCP1811X, V_R = 4.0V).*

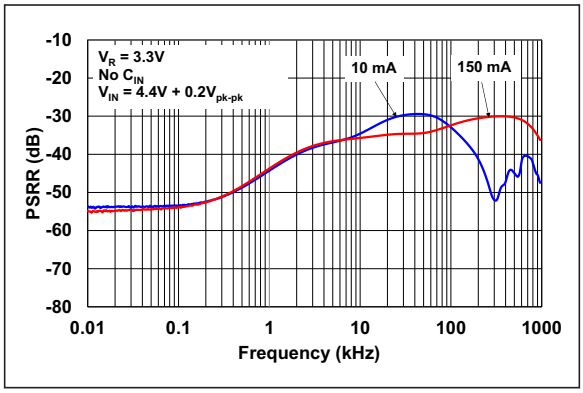


FIGURE 2-18: *Power Supply Ripple Rejection vs. Frequency (MCP1811X, V_R = 3.3V).*

Note: Unless otherwise indicated, C_{IN} = C_{OUT} = 1 µF (MCP1811X) or 2.2 µF (MCP1812X) ceramic type (X7R), I_{OUT} = 1 mA, T_A = +25°C, V_{IN} = V_R + 1V, $\overline{SHDN}$ = 1 MΩ pull-up to V_{IN}.

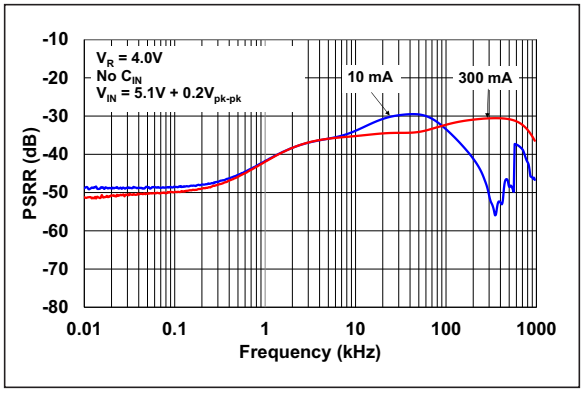


FIGURE 2-19: *Power Supply Ripple Rejection vs. Frequency (MCP1812X, V_R = 4.0V).*

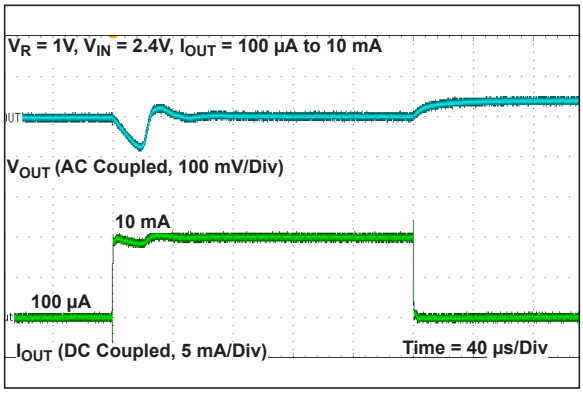


FIGURE 2-20: *Dynamic Load Step (MCP1812X, V_R = 1.0V).*

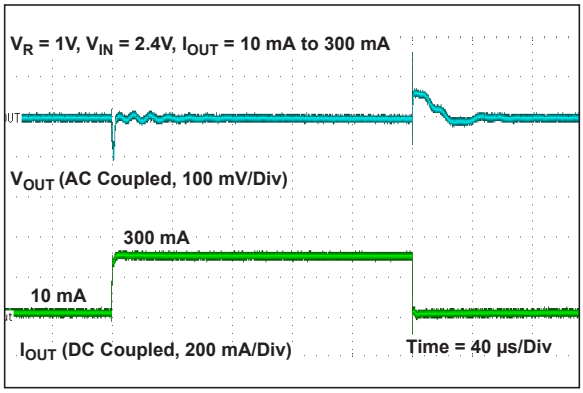


FIGURE 2-21: *Dynamic Load Step (MCP1812X, V_R = 1.0V).*

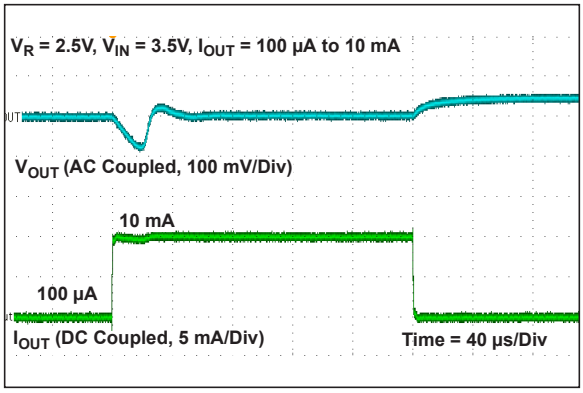


FIGURE 2-22: *Dynamic Load Step (MCP1812X, V_R = 2.5V).*

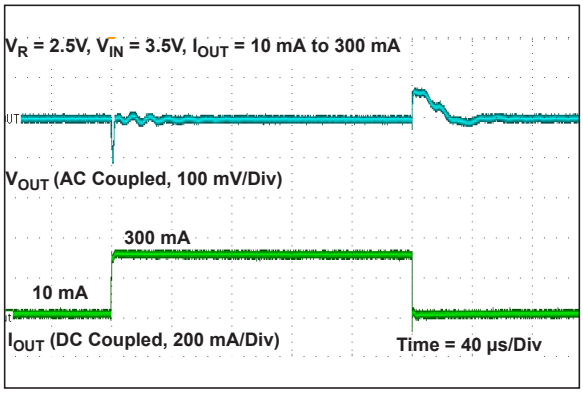


FIGURE 2-23: *Dynamic Load Step (MCP1812X, V_R = 2.5V).*

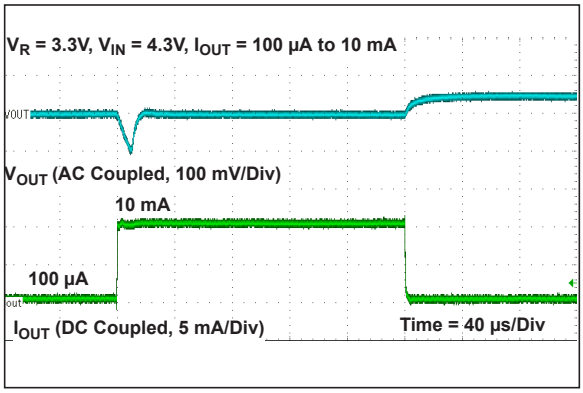


FIGURE 2-24: *Dynamic Load Step (MCP1811X, V_R = 3.3V).*

Note: Unless otherwise indicated, C_{IN} = C_{OUT} = 1 µF (MCP1811X) or 2.2 µF (MCP1812X) ceramic type (X7R), I_{OUT} = 1 mA, T_A = +25°C, V_{IN} = V_R + 1V, $\overline{SHDN}$ = 1 MΩ pull-up to V_{IN}.

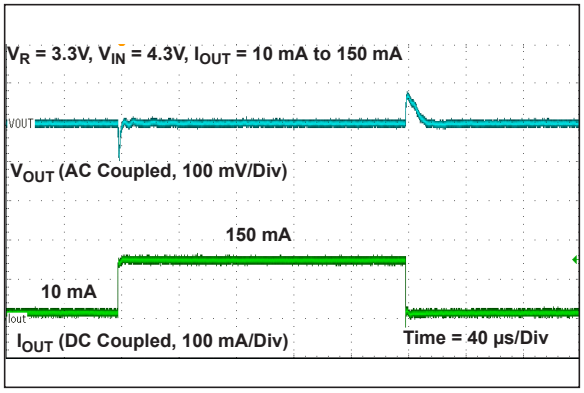


FIGURE 2-25: *Dynamic Load Step (MCP1811X, V_R = 3.3V).*

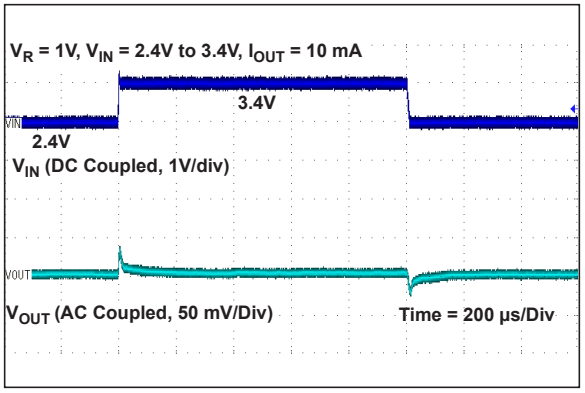


FIGURE 2-28: *Dynamic Line Step (MCP1812X, V_R = 1.0V).*

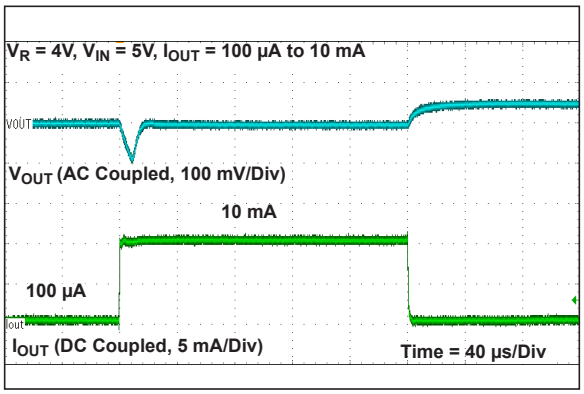


FIGURE 2-26: *Dynamic Load Step (MCP1811X, V_R = 4.0V).*

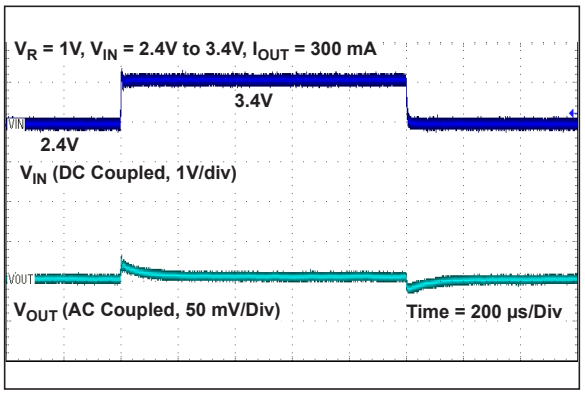


FIGURE 2-29: *Dynamic Line Step (MCP1812X, V_R = 1.0V).*

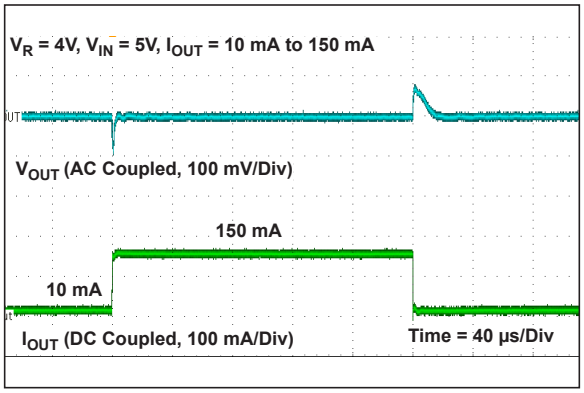


FIGURE 2-27: *Dynamic Load Step (MCP1811X, V_R = 4.0V).*

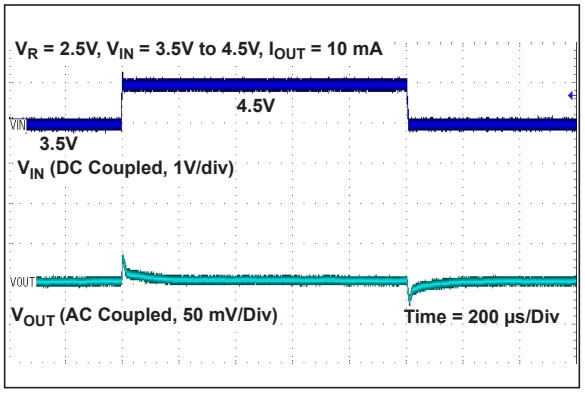


FIGURE 2-30: *Dynamic Line Step (MCP1812X, V_R = 2.5V).*

Note: Unless otherwise indicated, C_{IN} = C_{OUT} = 1 µF (MCP1811X) or 2.2 µF (MCP1812X) ceramic type (X7R), I_{OUT} = 1 mA, T_A = +25°C, V_{IN} = V_R + 1V, $\overline{SHDN}$ = 1 MΩ pull-up to V_{IN}.

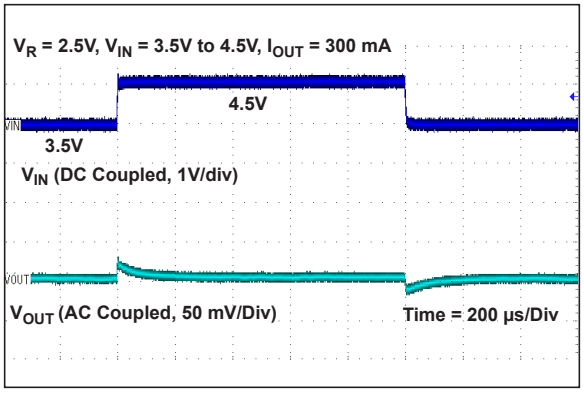


FIGURE 2-31: *Dynamic Line Step (MCP1812X, V_R = 2.5V).*

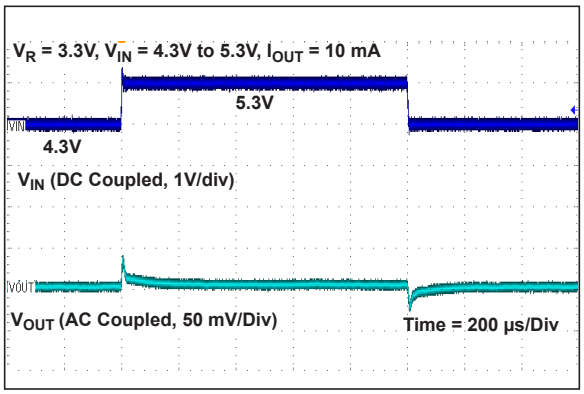


FIGURE 2-32: *Dynamic Line Step (MCP1811X, V_R = 3.3V).*

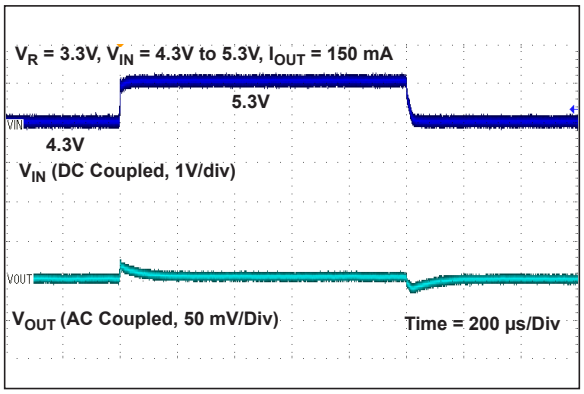


FIGURE 2-33: *Dynamic Line Step (MCP1811X, V_R = 3.3V).*

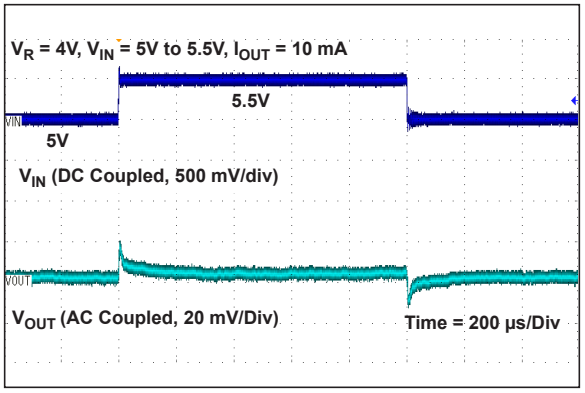


FIGURE 2-34: *Dynamic Line Step (MCP1811X, V_R = 4.0V).*

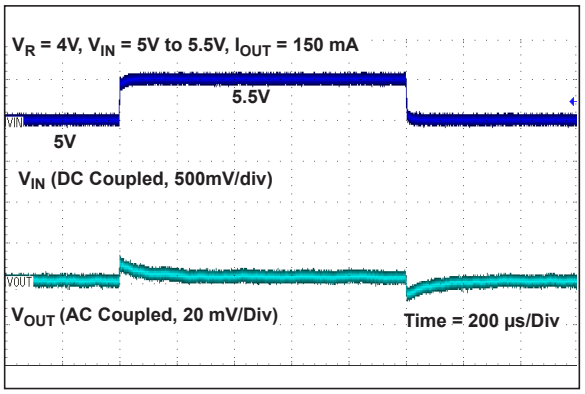


FIGURE 2-35: *Dynamic Line Step (MCP1811X, V_R = 4.0V).*

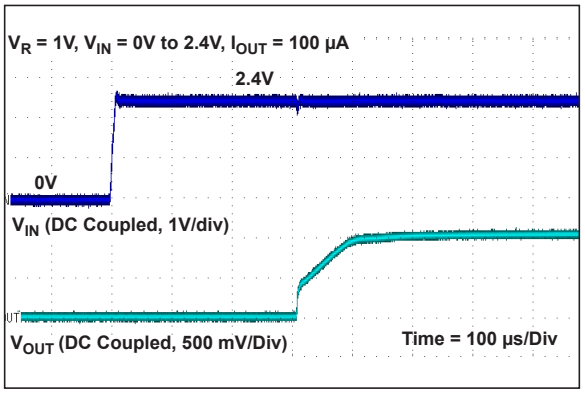


FIGURE 2-36: *Start-up from V_{IN} (MCP1812X, V_R = 1.0V).*

Note: Unless otherwise indicated, C_{IN} = C_{OUT} = 1 µF (MCP1811X) or 2.2 µF (MCP1812X) ceramic type (X7R), I_{OUT} = 1 mA, T_A = +25°C, V_{IN} = V_R + 1V, $\overline{SHDN}$ = 1 MΩ pull-up to V_{IN}.

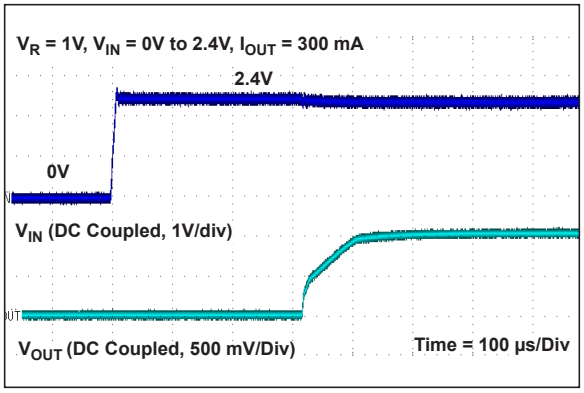


FIGURE 2-37: *Start-up from V_{IN} (MCP1812X, V_R = 1.0V).*

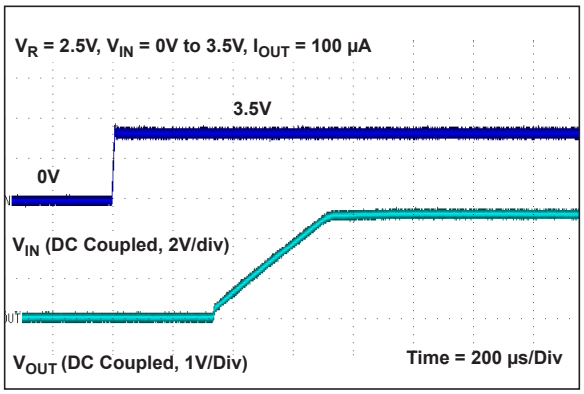


FIGURE 2-38: *Start-up from V_{IN} (MCP1812X, V_R = 2.5V).*

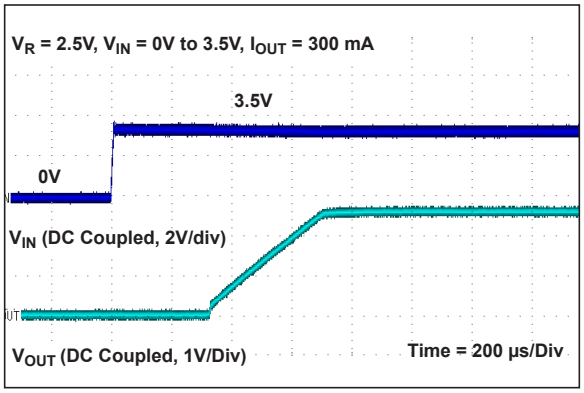


FIGURE 2-39: *Start-up from V_{IN} (MCP1812X, V_R = 2.5V).*

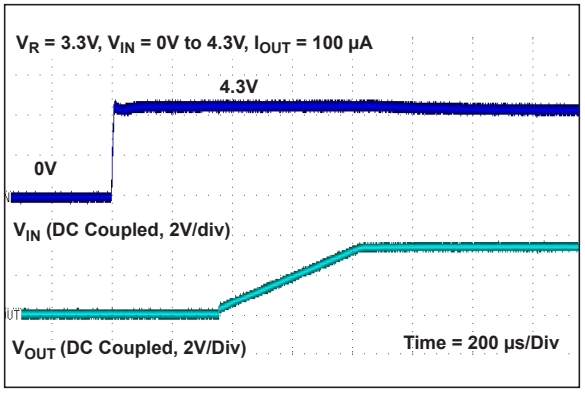


FIGURE 2-40: *Start-up from V_{IN} (MCP1811X, V_R = 3.3V).*

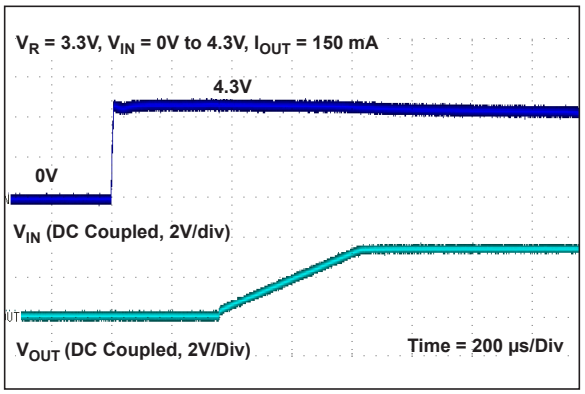


FIGURE 2-41: *Start-up from V_{IN} (MCP1811X, V_R = 3.3V).*

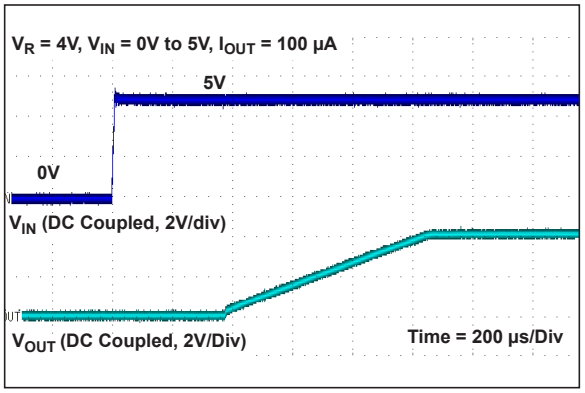


FIGURE 2-42: *Start-up from V_{IN} (MCP1811X, V_R = 4.0V).*

Note: Unless otherwise indicated, C_{IN} = C_{OUT} = 1 µF (MCP1811X) or 2.2 µF (MCP1812X) ceramic type (X7R), I_{OUT} = 1 mA, T_A = +25°C, V_{IN} = V_R + 1V, $\overline{SHDN}$ = 1 MΩ pull-up to V_{IN}.

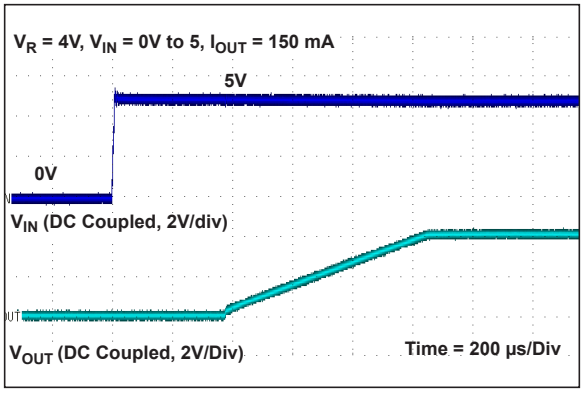


FIGURE 2-43: *Start-up from V_{IN} (MCP1811X, V_R = 4.0V).*

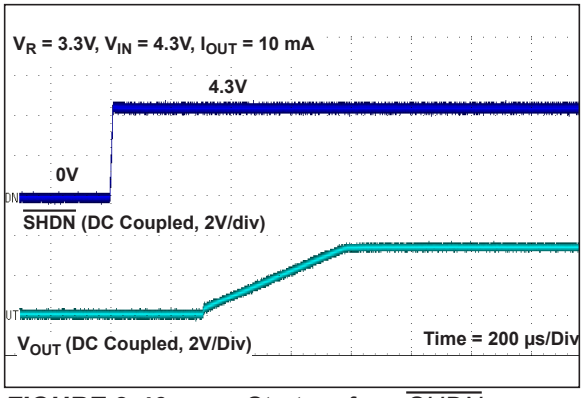


FIGURE 2-46: *Start-up from $\overline{SHDN}$ (MCP1811X, V_R = 3.3V).*

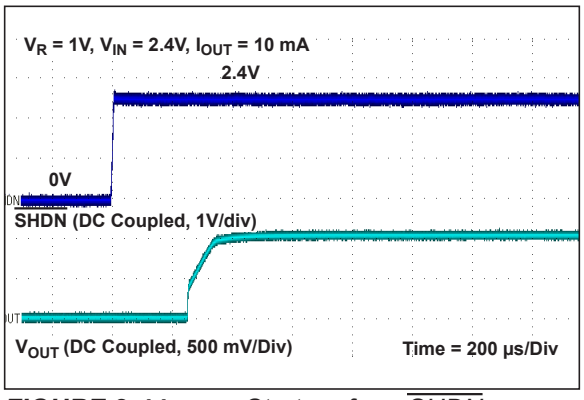


FIGURE 2-44: *Start-up from $\overline{SHDN}$ (MCP1812X, V_R = 1.0V).*

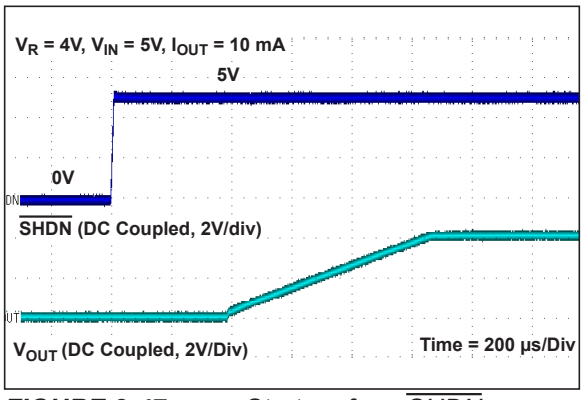


FIGURE 2-47: *Start-up from $\overline{SHDN}$ (MCP1811X, V_R = 4.0V).*

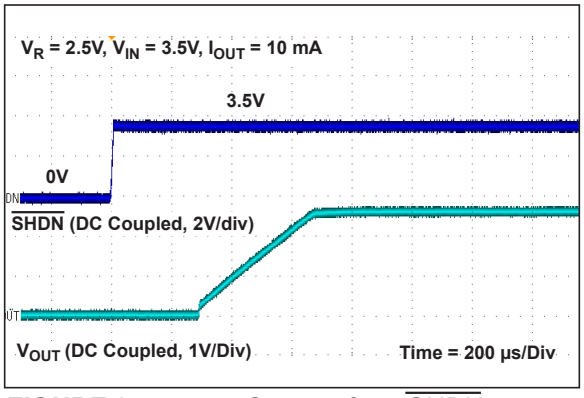


FIGURE 2-45: *Start-up from $\overline{SHDN}$ (MCP1812X, V_R = 2.5V).*

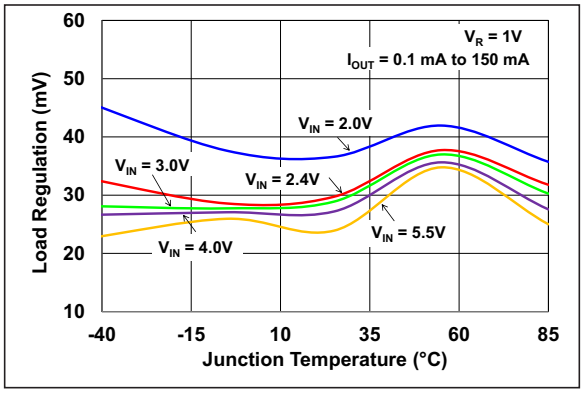


FIGURE 2-48: *Load Regulation vs. Junction Temperature (MCP1811X, V_R = 1.0V).*

Note: Unless otherwise indicated, C_{IN} = C_{OUT} = 1 µF (MCP1811X) or 2.2 µF (MCP1812X) ceramic type (X7R), I_{OUT} = 1 mA, T_A = +25°C, V_{IN} = V_R + 1V, $\overline{SHDN}$ = 1 MΩ pull-up to V_{IN}.

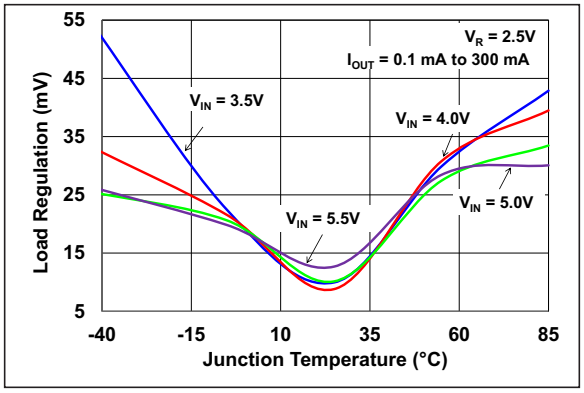


FIGURE 2-49: *Load Regulation vs. Junction Temperature (MCP1812X, V_R = 2.5V).*

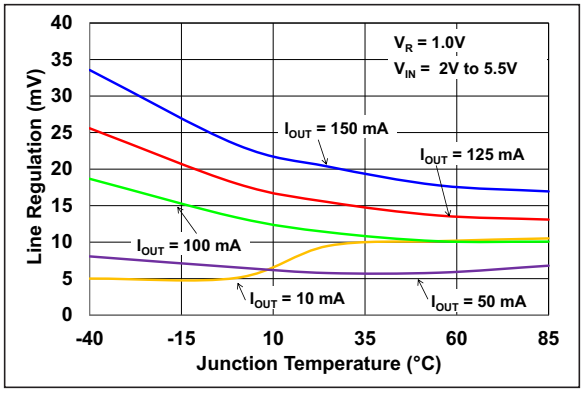


FIGURE 2-52: *Line Regulation vs. Junction Temperature (MCP1811X, V_R = 1.0V).*

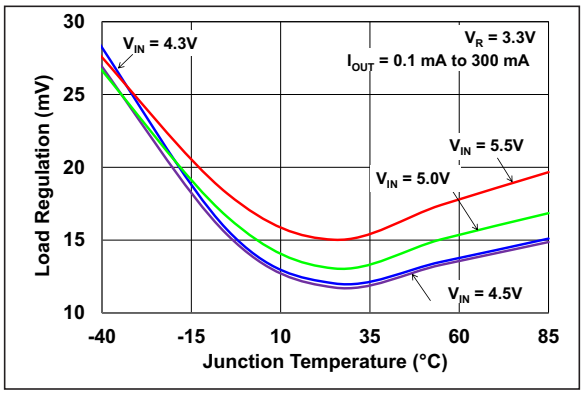


FIGURE 2-50: *Load Regulation vs. Junction Temperature (MCP1812X, V_R = 3.3V).*

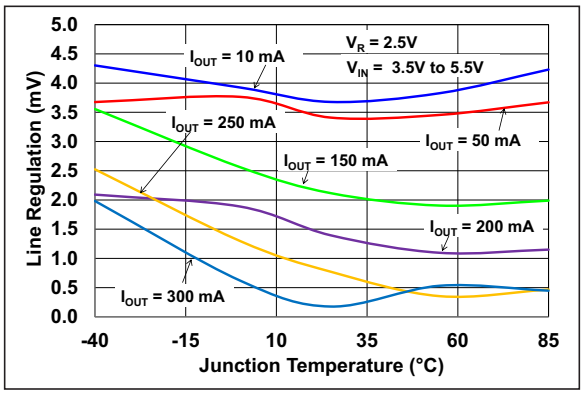


FIGURE 2-53: *Line Regulation vs. Junction Temperature (MCP1812X, V_R = 2.5V).*

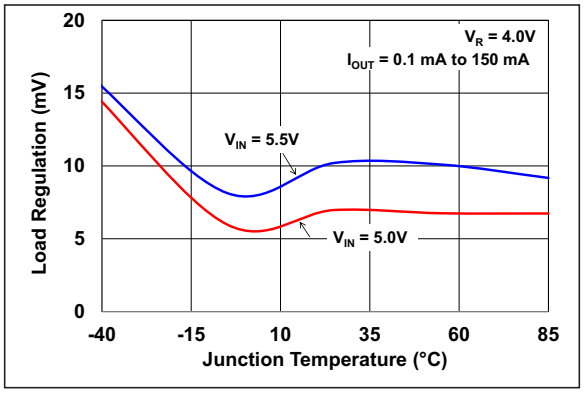


FIGURE 2-51: *Load Regulation vs. Junction Temperature (MCP1811X, V_R = 4.0V).*

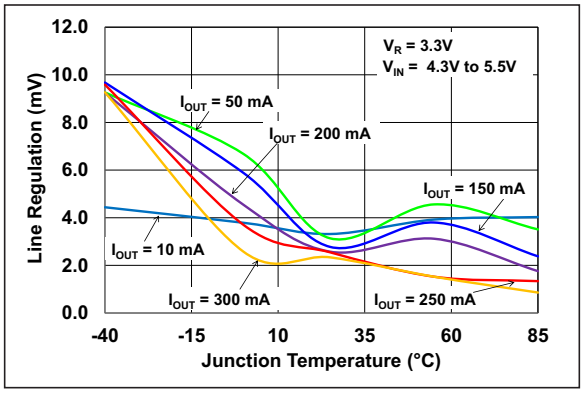


FIGURE 2-54: *Line Regulation vs. Junction Temperature (MCP1812X, V_R = 3.3V).*

Note: Unless otherwise indicated, C_{IN} = C_{OUT} = 1 µF (MCP1811X) or 2.2 µF (MCP1812X) ceramic type (X7R), I_{OUT} = 1 mA, T_A = +25°C, V_{IN} = V_R + 1V, $\overline{SHDN}$ = 1 MΩ pull-up to V_{IN}.

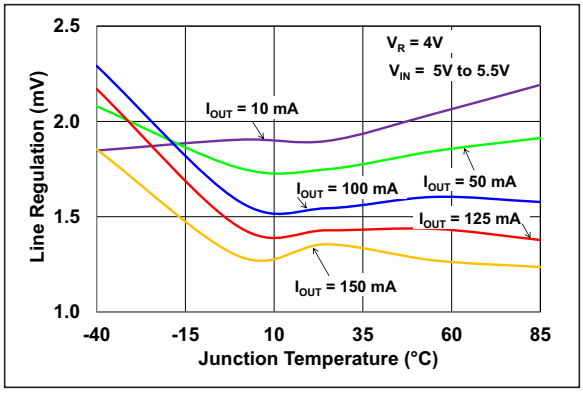


FIGURE 2-55: *Line Regulation vs. Junction Temperature (MCP1811X, V_R = 4.0V).*

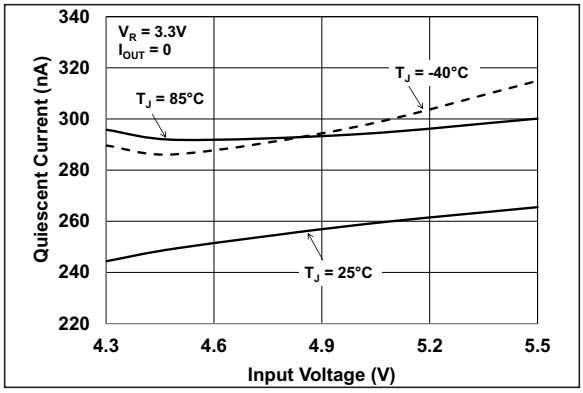


FIGURE 2-58: *Quiescent Current vs. Input Voltage (MCP1812X, V_R = 3.3V).*

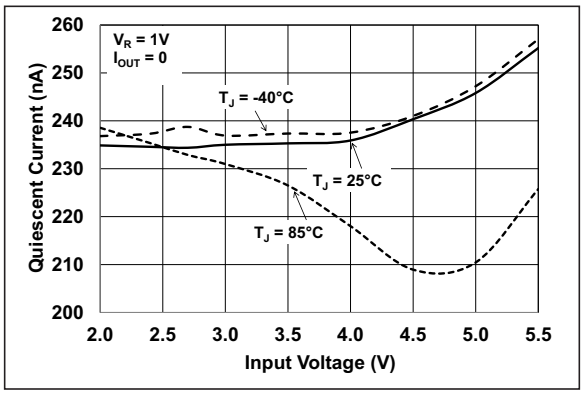


FIGURE 2-56: *Quiescent Current vs. Input Voltage (MCP1811X, V_R = 1.0V).*

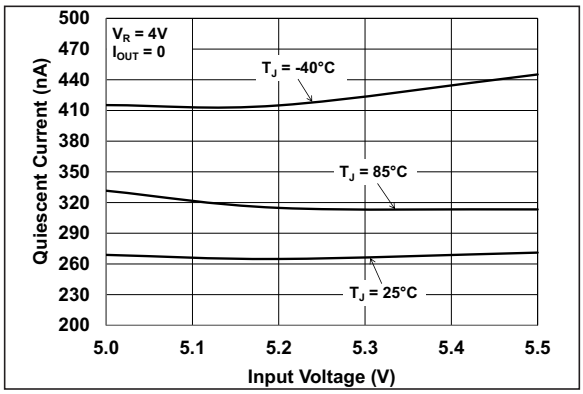


FIGURE 2-59: *Quiescent Current vs. Input Voltage (MCP1811X, V_R = 4.0V).*

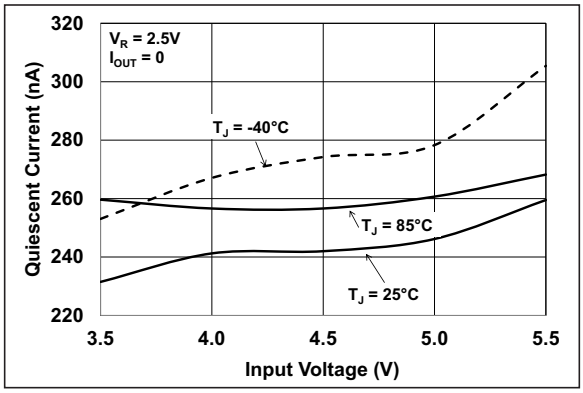


FIGURE 2-57: *Quiescent Current vs. Input Voltage (MCP1812X, V_R = 2.5V).*

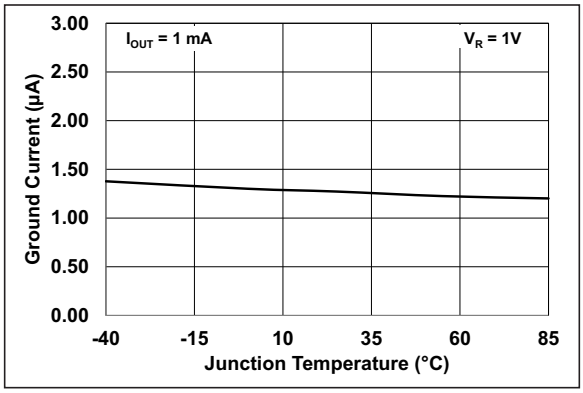


FIGURE 2-60: *Ground Current vs. Temperature (MCP1811X, V_R = 1.0V).*

Note: Unless otherwise indicated, C_{IN} = C_{OUT} = 1 µF (MCP1811X) or 2.2 µF (MCP1812X) ceramic type (X7R), I_{OUT} = 1 mA, T_A = +25°C, V_{IN} = V_R + 1V, $\overline{SHDN}$ = 1 MΩ pull-up to V_{IN}.

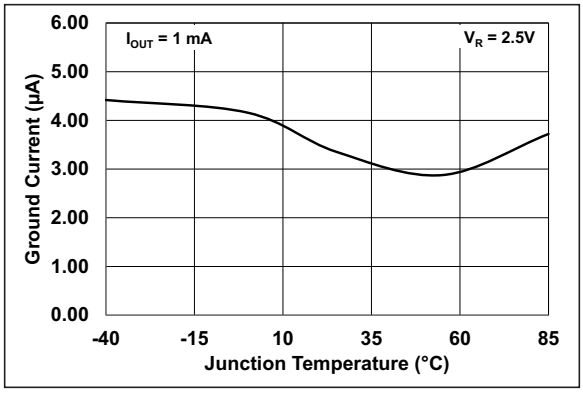


FIGURE 2-61: *Ground Current vs. Temperature (MCP1812X, V_R = 2.5V).*

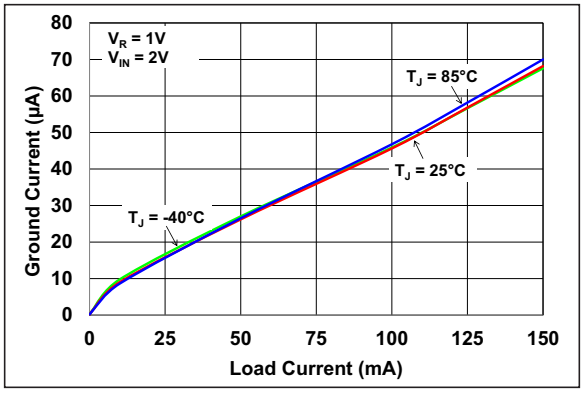


FIGURE 2-64: *Ground Current vs. Load Current (MCP1811X, V_R = 1.0V).*

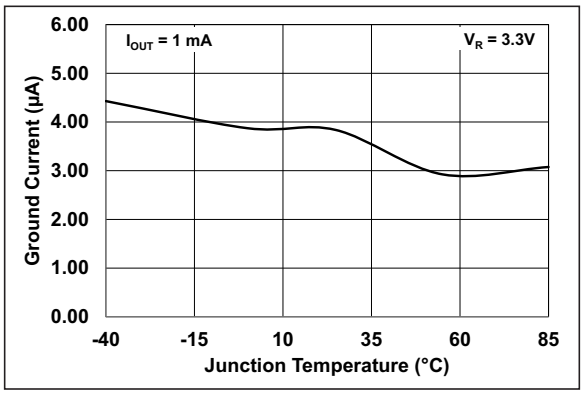


FIGURE 2-62: *Ground Current vs. Temperature (MCP1812X, V_R = 3.3V).*

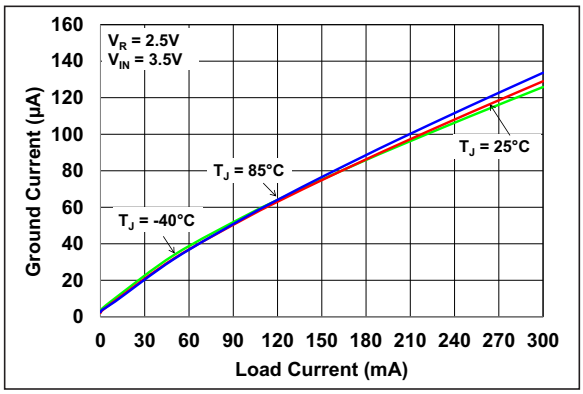


FIGURE 2-65: *Ground Current vs. Load Current (MCP1812X, V_R = 2.5V).*

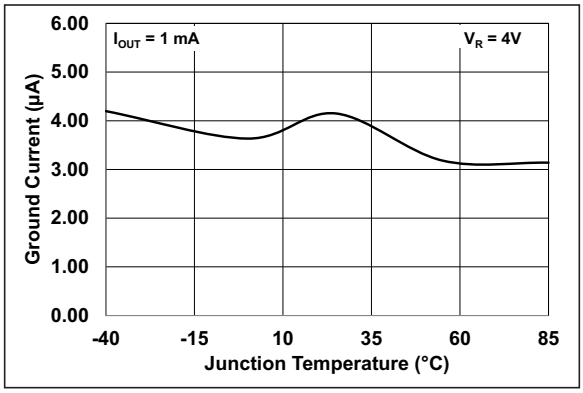


FIGURE 2-63: *Ground Current vs. Temperature (MCP1811X, V_R = 4.0V).*

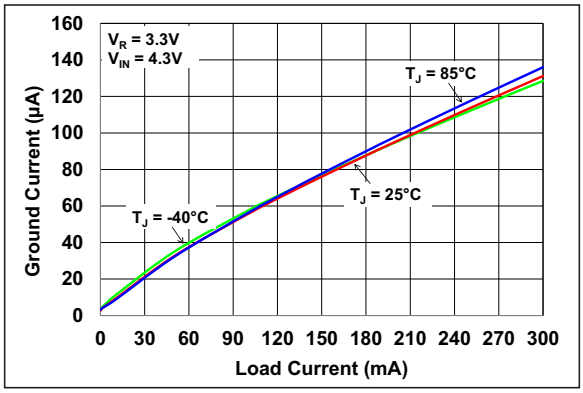


FIGURE 2-66: *Ground Current vs. Load Current (MCP1812X, V_R = 3.3V).*

Note: Unless otherwise indicated, C_{IN} = C_{OUT} = 1 µF (MCP1811X) or 2.2 µF (MCP1812X) ceramic type (X7R), I_{OUT} = 1 mA, T_A = +25°C, V_{IN} = V_R + 1V, $\overline{SHDN}$ = 1 MΩ pull-up to V_{IN}.

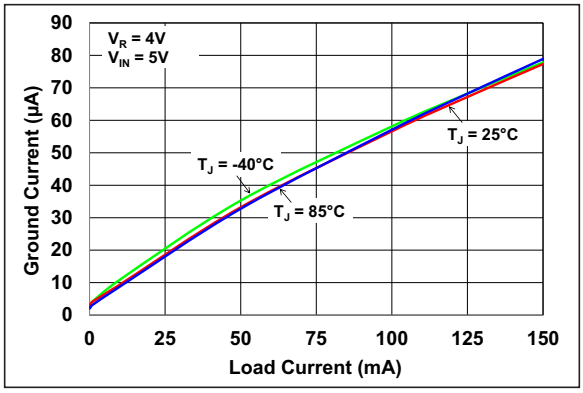


FIGURE 2-67: *Ground Current vs. Load Current (MCP1811X, V_R = 4.0V).*

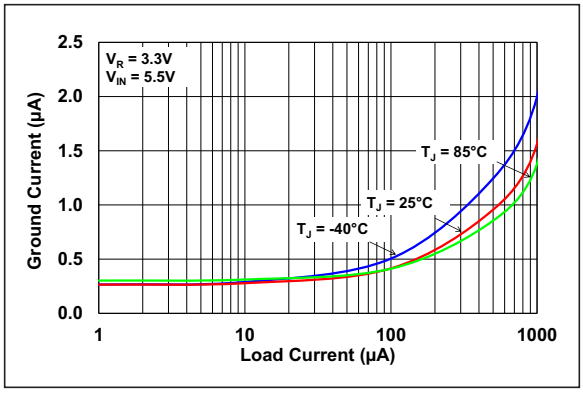


FIGURE 2-70: *Ground Current vs. Very Low Load Current (MCP1811X, V_R = 3.3V).*

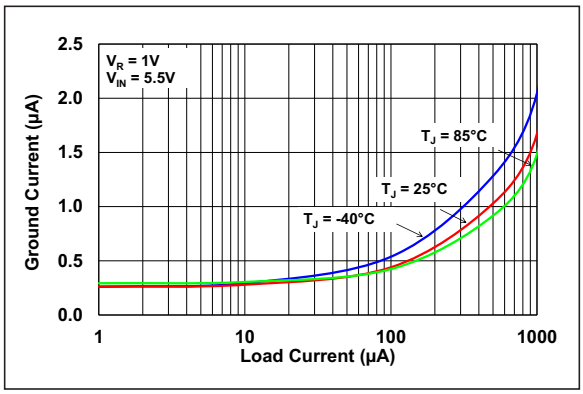


FIGURE 2-68: *Ground Current vs. Very Low Load Current (MCP1812X, V_R = 1.0V).*

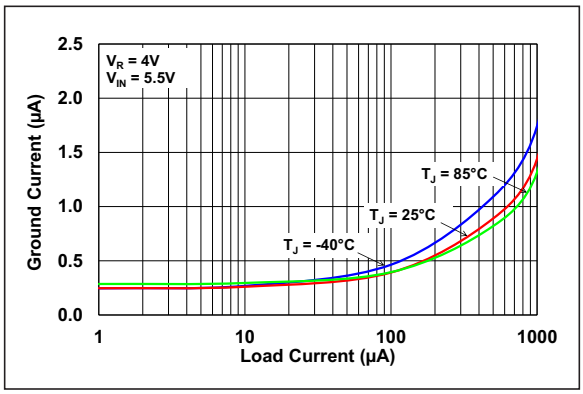


FIGURE 2-71: *Ground Current vs. Very Low Load Current (MCP1811X, V_R = 4.0V).*

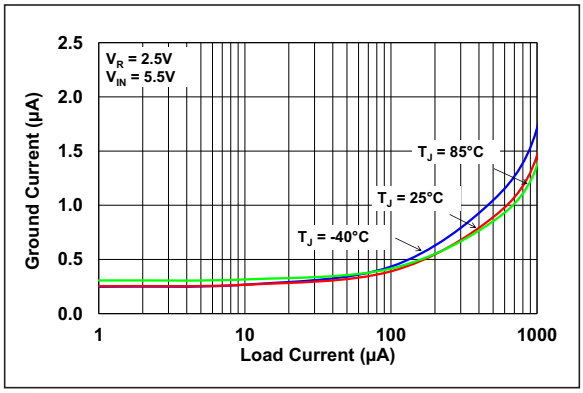


FIGURE 2-69: *Ground Current vs. Very Low Load Current (MCP1812X, V_R = 2.5V).*

3.0 PIN DESCRIPTION

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

MCP1811X/12X 4-Lead 1x1 mm UDFN	MCP1811X/12X 3-Lead SOT-23/SC70	MCP1811X/12X 5-Lead SOT-23/SC70	Symbol	Description
2	3	2	GND	Ground
1	1	5	V_{OUT}	Regulated Output Voltage V_R
—	—	4	NC	Not Connected Pins (should either be left floated or connected to ground)
4	2	1	V_{IN}	Input Voltage Supply
3	—	3	$\overline{SHDN}$	Shutdown Control Input (active-low); do not leave this pin floating
5	—	—	EP	Exposed Thermal Pad, connected to GND

3.1 Ground Pin (GND)

For optimal noise and Power Supply Rejection Ratio (PSRR) performance, the GND pin of the LDO should be tied to an electrically “quiet” ground circuit. The GND pin of the LDO conducts only the ground current, so a wider trace is not required. For powered applications that have switching or noisy circuits, tie the GND pin to the return of the output capacitor. Ground planes help lower the inductance and voltage spikes caused by fast transient load currents.

3.2 Regulated Output Voltage Pin (V_{OUT})

The V_{OUT} pin is the regulated output voltage V_R of the LDO. A minimum output capacitance of 1.0 µF (MCP1811X) and 2.2 µF (MCP1812X) are required for LDO stability. The MCP1811X/12X is stable with ceramic capacitors. See **Section 4.2 “Output Capacitor”** for output capacitor selection guidance.

3.3 Input Voltage Supply Pin (V_{IN})

Connect the input voltage source to V_{IN}. If the input voltage source is located several inches away from the LDO or is a battery, it is recommended that an input capacitor be used. A typical input capacitance value of 1 µF to 10 µF is sufficient for most applications (1 µF is typical for MCP1811X and 2.2 µF is typical for MCP1812X). The type of capacitor used is ceramic. However, the low-ESR characteristics of the ceramic capacitor will yield better noise and PSRR performance at high frequency.

3.4 Shutdown Control Input ($\overline{SHDN}$)

The $\overline{SHDN}$ input is used to turn the LDO output voltage on and off. When the $\overline{SHDN}$ input is at a logic high level, the LDO output voltage is enabled. When the $\overline{SHDN}$ input is pulled to a logic low level, the LDO output voltage is disabled (with output discharge for MCP1811A/12A). When the $\overline{SHDN}$ input is pulled low, the LDO enters in a low-current shutdown state, where the typical quiescent current is 10 nA for MCP1811A/12A and 5 nA for MCP1811B/12B.

4.0 DEVICE OVERVIEW

The MCP1811X/12X family is a 150 mA/300 mA output current, Low-Dropout (LDO) voltage regulator. The Low-Dropout voltage of 400 mV, typical, at 300 mA of current, makes it recommended for long-life battery-powered applications. The input voltage ranges from a minimum of 1.8V to 5.5V. The MCP1811X/12X family features a shutdown control input pin and is available in nine standard fixed output voltage options: 1V, 1.2V, 1.8V, 2.0V, 2.5V, 2.8V, 3.0V, 3.3V and 4.0V. It uses a proprietary voltage reference and sensing scheme to maintain the ultra-low 250 nA quiescent current.

4.1 Output Capabilities and Current Limiting

The MCP1811X/12X LDO is tested and ensured to supply a minimum of 150 mA of output current for MCP1811X and 300 mA of output current for MCP1812X.

The MCP1811X/12X devices do not incorporate an internal voltage divider. This is another design key of achieving ultra-low power consumption. In addition, there is a pull-down switch on the output to limit the overshoot in case of powering an ultra-light load. Due to the increased leakage through the power transistor at elevated temperature (> 60°C), the output voltage can be drifted up (to approximately 210 mV) when the input supply to the output differential is larger than 3V. It is recommended to add a very small dummy load (25 nA, typical) to compensate for the leakage. In conditions other than mentioned above, the device does not require a minimum load to regulate the output voltage within the specified tolerance.

The MCP1811X/12X family also incorporates an output current foldback protection during overload conditions. The MCP1811X/12X devices enter foldback when V_{OUT} falls below 0.6V (typical).

4.2 Output Capacitor

The MCP1811X/12X devices require a minimum output capacitance of 1 µF (2.2 µF for MCP1812X) for output voltage stability. Ceramic capacitors are recommended because of their size, cost and robust environmental qualities.

The output capacitor should be located as close to the LDO output as is practical. Ceramic materials, X7R and X5R, have low-temperature coefficients, and are well within the acceptable ESR range required. A typical 1 µF X7R 0805 capacitor has an ESR of 20 mΩ.

4.3 Input Capacitor

Low input source impedance is necessary for the LDO output to operate properly. When operating from batteries, or in applications with long lead length (> 10 inches) between the input source and the LDO, some input capacitance is recommended. A minimum of 1 µF (2.2 µF for MCP1812X) to 10 µF of capacitance is recommended for most applications.

For applications that have output step load requirements, the input capacitance of the LDO is very important. The input capacitance must provide a low-impedance source. This allows the LDO to respond quickly to the output load step. For good step response performance, the input capacitor should be equivalent to, or of higher value than, the output capacitor. The capacitor should be placed as close to the input of the LDO as is practical. Larger input capacitors will also help reduce any high-frequency noise on the input and output of the LDO, as well as the effects of any inductance that exists between the input source voltage and the input capacitance of the LDO.

4.4 Shutdown Input ($\overline{SHDN}$)

The $\overline{SHDN}$ input is an active-low input signal that turns the LDO on and off. The $\overline{SHDN}$ threshold is a percentage of the input voltage. The maximum input low logic level is 20% of V_{IN} and the minimum high logic level is 70% of V_{IN}.

The $\overline{SHDN}$ pin ignores low going pulses that are up to 400 ns. This small bit of filtering helps to reject any system noise spikes on the $\overline{SHDN}$ input signal.

On the rising edge of the $\overline{SHDN}$ input, the shutdown circuitry has a typical 400 µs delay before allowing the regulator output to turn on. This delay helps to reject any false turn-on signals or noise on the $\overline{SHDN}$ input signal. After the typical 400 µs delay, the regulator starts charging the load capacitor as the output rises from 0V to its final regulated value. The charging current will be limited by the short-circuit current value of the device. If the $\overline{SHDN}$ input signal is pulled low during the typical 400 µs delay period, the timer will be reset and the delay time will start over again on the next rising edge of the $\overline{SHDN}$ input. The total time from the $\overline{SHDN}$ input going high (turn-on) to the output being in regulation shall typically be 400 µs delay time plus output voltage rise time, which is V_R-dependent and may vary from 200 µs up to 1000 µs for a C_{LOAD} = 1.0 µF and for a C_{LOAD} = 2.2 µF. Figure 4-1 shows a timing diagram of the $\overline{SHDN}$ input.

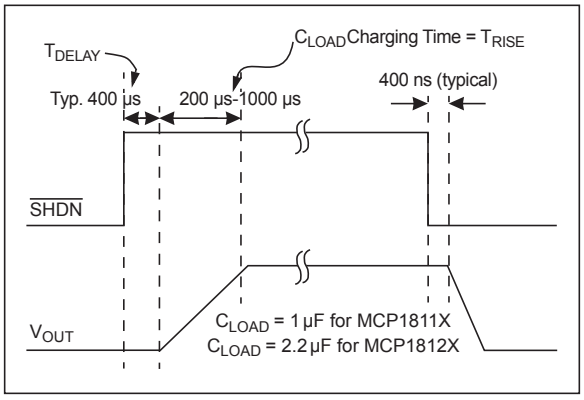


FIGURE 4-1: *Shutdown Input Timing Diagram.*

4.5 Dropout Voltage

Dropout voltage is defined as the input-to-output voltage differential at which the output voltage drops 2% below the nominal value that was measured with a V_R + 1V differential applied. The MCP1811X/12X LDO devices show a Low-Dropout voltage specification of 400 mV (typical) for all V_R, and presents small variations in the dropout value with load and temperature changes.

See **Section 1.0 "Electrical Characteristics"** for maximum dropout voltage specifications.

5.0 APPLICATION CIRCUITS

5.1 Typical Application

The MCP1811A/11B/12A/12B family is used for applications that require ultra-low quiescent current draw.

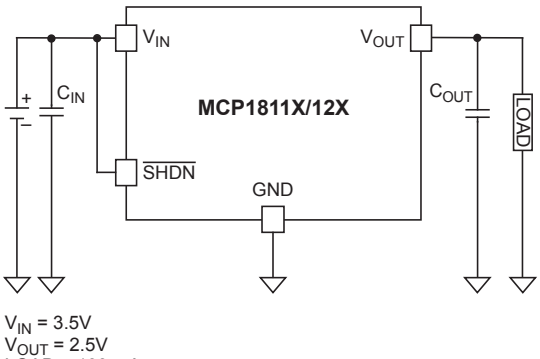


FIGURE 5-1: *Typical Application Circuit.*

5.2 Power Calculations

5.2.1 POWER DISSIPATION

The internal power dissipation within the MCP1811X/12X devices is a function of input voltage, output voltage, output current and ground current. Equation 5-1 can be used to calculate the internal power dissipation for the LDO.

EQUATION 5-1:

$$P_{LDO} = (V_{IN(MAX)} - V_{OUT(MIN)}) \times I_{OUT(MAX)}$$

Where:

P_{LDO} = Internal power dissipation of the LDO active element

$V_{IN(MAX)}$ = Maximum input voltage

$V_{OUT(MIN)}$ = LDO minimum output voltage

$I_{OUT(MAX)}$ = Maximum output current

In addition to the LDO pass element power dissipation, there is power dissipation within the MCP1811X/12X devices as a result of quiescent or ground current. The power dissipation, as a result of the ground current, can be calculated by applying Equation 5-2.

EQUATION 5-2:

$$P_{(IGND)} = V_{IN(MAX)} \times I_{GND}$$

Where:

$P_{(IGND)}$ = Power dissipation due to the ground current of the LDO

$V_{IN(MAX)}$ = Maximum input voltage

I_{GND} = Current flowing out of the GND pin

The total power dissipated within the MCP1811X/12X devices is the sum of the power dissipated in the LDO pass device and the $P(I_{GND})$ term. Because of the CMOS construction, the typical I_{GND} for the MCP1811X/12X devices is 90 µA for MCP1811X and 180 µA for MCP1812X at full load. Operating at a maximum V_{IN} of 5.5V results in a power dissipation of 0.5 mW for MCP1811X and 1 mW for MCP1812X. For most applications, this is small compared to the LDO pass device power dissipation and can be neglected.

The maximum continuous operating junction temperature specified for the MCP1811X/12X family is +85°C. To estimate the internal junction temperature of the MCP1811X/12X devices, the total internal power dissipation is multiplied by the thermal resistance from junction-to-ambient (θ_{JA}) of the device. For example, the thermal resistance from junction to ambient for the 5-Lead SOT-23 package is estimated at 184.82°C/W.

EQUATION 5-3:

$$T_{J(MAX)} = P_{LDO} \times \theta_{JA} + T_{A(MAX)}$$

Where:

$T_{J(MAX)}$ = Maximum continuous junction temperature

P_{LDO} = Total power dissipation of the device

θ_{JA} = Thermal resistance from junction to ambient (see **"Temperature Specifications"**)

$T_{A(MAX)}$ = Maximum ambient temperature

The maximum power dissipation capability for a package can be calculated given the junction-to-ambient thermal resistance and the maximum ambient temperature for the application. Equation 5-4 can be used to determine the package maximum internal power dissipation.

EQUATION 5-4:

$$P_{D(MAX)} = \frac{(T_{J(MAX)} - T_{A(MAX)})}{\theta_{JA}}$$

Where:

$P_{D(MAX)}$ = Maximum power dissipation of the device

EQUATION 5-5:

$$T_{J(RISE)} = P_{D(MAX)} \times \theta_{JA}$$

Where:

$T_{J(RISE)}$ = Rise in the device junction temperature over the ambient temperature

EQUATION 5-6:

$$T_J = T_{J(RISE)} + T_A$$

Where:

T_J = Junction temperature

T_A = Ambient temperature

5.3 Typical Application Examples

Internal power dissipation, junction temperature rise, junction temperature and maximum power dissipation are calculated in the following example. The power dissipation, as a result of ground current, is small enough to be neglected.

5.3.1 POWER DISSIPATION EXAMPLE

EXAMPLE 5-1:

Package

Package Type = 5-Lead SOT-23

Input Voltage

V_{IN} = 3.5V ± 5%

LDO Output Voltage and Current

V_{OUT} = 2.5V

I_{OUT} = 100 mA

Maximum Ambient Temperature

$T_{A(MAX)}$ = +60°C

Internal Power Dissipation

$P_{LDO(MAX)} = (V_{IN(MAX)} - V_{OUT(MIN)}) \times I_{OUT(MAX)}$

P_{LDO} = ((3.5V x 1.05) – (2.5V x 0.96)) x 100 mA

P_{LDO} = 0.127W

5.3.1.1 Device Junction Temperature Rise

The internal junction temperature rise is a function of internal power dissipation and of the thermal resistance, from junction to ambient, for the application. The thermal resistance, from junction to ambient (θ_{JA}), is derived from EIA/JEDEC standards for measuring thermal resistance. The EIA/JEDEC specification is JESD51. The standard describes the test method and board specifications for measuring the thermal resistance from junction to ambient. The actual thermal resistance for a particular application can vary depending on many factors, such as copper area and thickness. Refer to Application Note AN792, *"A Method to Determine How Much Power a SOT-23 Can Dissipate in an Application"* (DS00792) for more information regarding this subject.

EXAMPLE 5-2:

$T_{J(RISE)} = P_{TOTAL} \times \theta_{JA}$

$T_{J(RISE)}$ = 0.127W x 184.82°C/W

$T_{J(RISE)}$ = 23.47°C

5.3.1.2 Junction Temperature Estimate

To estimate the internal junction temperature, the calculated temperature rise is added to the ambient or offset temperature. For this example, the worst-case junction temperature is estimated below:

EXAMPLE 5-3:

$T_J = T_{J(RISE)} + T_{A(MAX)}$

T_J = 23.47°C + 60.0°C

T_J = 83.47°C

5.3.1.3 Maximum Package Power Dissipation at +60°C Ambient Temperature

EXAMPLE 5-4:

5-Lead SOT-23 (θ_{JA} = 184.82°C/W):

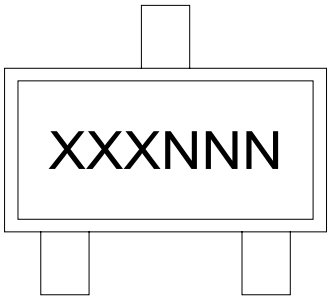
$P_{D(MAX)}$ = (85°C – 60°C)/184.82°C/W

$P_{D(MAX)}$ = 0.135W

6.0 PACKAGING INFORMATION

6.1 Package Marking Information

3-Lead SOT-23



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MCP1811AT-012/TT	AAHNNN
MCP1811AT-018/TT	AAMNNN
MCP1811AT-020/TT	AASNNN
MCP1811AT-025/TT	AAWNNN
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MCP1811AT-030/TT	ABANNN
MCP1811AT-033/TT	ABENNN
MCP1811AT-040/TT	ABONNN
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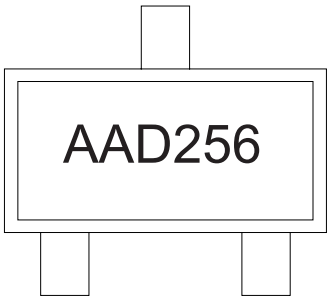
MCP1812BT-040/TT	ABSNNN

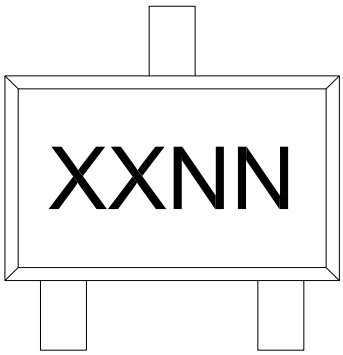
Example



Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

3-Lead SC70



Part Number	Code
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MCP1811AT-018/LB	LINN
MCP1811AT-020/LB	LMNN
MCP1811AT-025/LB	LQNN
MCP1811AT-028/LB	MMNN
MCP1811AT-030/LB	LUNN
MCP1811AT-033/LB	LYNN
MCP1811AT-040/LB	MGNN
MCP1811BT-010/LB	LBNN
MCP1811BT-012/LB	LFNN
MCP1811BT-018/LB	LJNN
MCP1811BT-020/LB	LNNN
MCP1811BT-025/LB	LRNN
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MCP1811BT-040/LB	MHNN
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MCP1812AT-025/LB	LSNN
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MCP1812AT-033/LB	MANN
MCP1812AT-040/LB	MINN
MCP1812BT-010/LB	LDNN
MCP1812BT-012/LB	LHNN
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5-Lead SC70	
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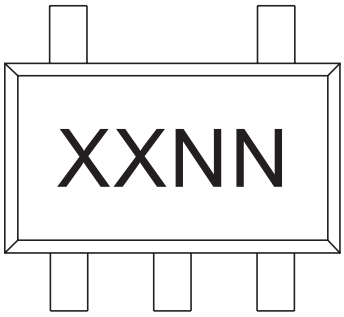
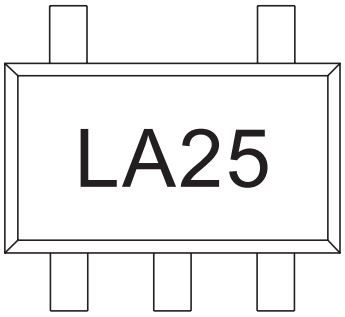
MCP1811BT-012/LT	ECNN
MCP1811BT-018/LT	EHNN

Example

5-Lead SC70



Example



Part Number	Code
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MCP1811BT-030/LT	EUNN
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MCP1811AT-040/LT	FHNN
MCP1811BT-010/LT	DYNN
MCP1811BT-012/LT	ECNN
MCP1811BT-018/LT	EHNN
MCP1811BT-020/LT	EMNN
MCP1811BT-025/LT	EQNN
MCP1811BT-028/LT	FONN
MCP1811BT-030/LT	EUNN
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MCP1812AT-020/LT	ENNN
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MCP1812AT-028/LT	FLNN
MCP1812AT-030/LT	EVNN
MCP1812AT-033/LT	EZNN
MCP1812AT-040/LT	FJNN
MCP1812BT-010/LT	EANN
MCP1812BT-012/LT	EFNN
MCP1812BT-018/LT	EJNN
MCP1812BT-020/LT	EONN
MCP1812BT-025/LT	ESNN
MCP1812BT-028/LT	FMNN
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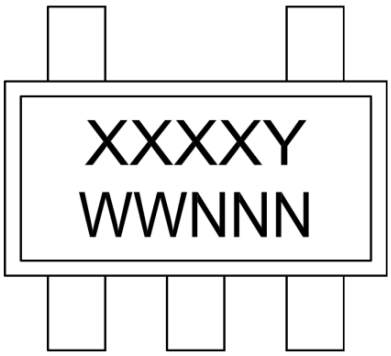
MCP1812BT-033/LT	FANN
MCP1812BT-040/LT	FKNN

5-Lead SOT-23



Part Number	Code
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MCP1811AT-018/OT	AADZY
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MCP1811AT-028/OT	QZNNY
MCP1811AT-030/OT	AAEMY
MCP1811AT-033/OT	ABERY
MCP1811AT-040/OT	QSNNY
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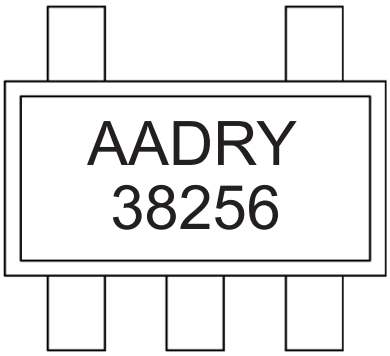
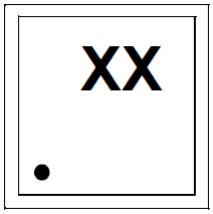
MCP1811BT-012/OT	AADWY
MCP1811BT-018/OT	AAEAY
MCP1811BT-020/OT	AAEEY
MCP1811BT-025/OT	AAEJY
MCP1811BT-028/OT	RANNY
MCP1811BT-030/OT	ABENY
MCP1811BT-033/OT	ABESY
MCP1811BT-040/OT	QTNNY
MCP1812AT-010/OT	AADTY
MCP1812AT-012/OT	AADXY
MCP1812AT-018/OT	AAEBY
MCP1812AT-020/OT	AAEFY
MCP1812AT-025/OT	AAEKY
MCP1812AT-028/OT	QXNN
MCP1812AT-030/OT	ABEPY
MCP1812AT-033/OT	ABETY
MCP1812AT-040/OT	QVNNY
MCP1812BT-010/OT	AADUY
MCP1812BT-012/OT	AADYY
MCP1812BT-018/OT	AAECY
MCP1812BT-020/OT	AAEGY
MCP1812BT-025/OT	AAELY
MCP1812BT-028/OT	QYNNY
MCP1812BT-030/OT	ABEQY
MCP1812BT-033/OT	ABEUY
MCP1812BT-040/OT	QWNNY

Example

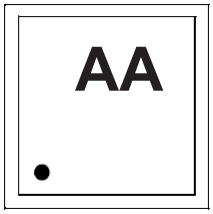


4-Lead 1x1 mm UDFN



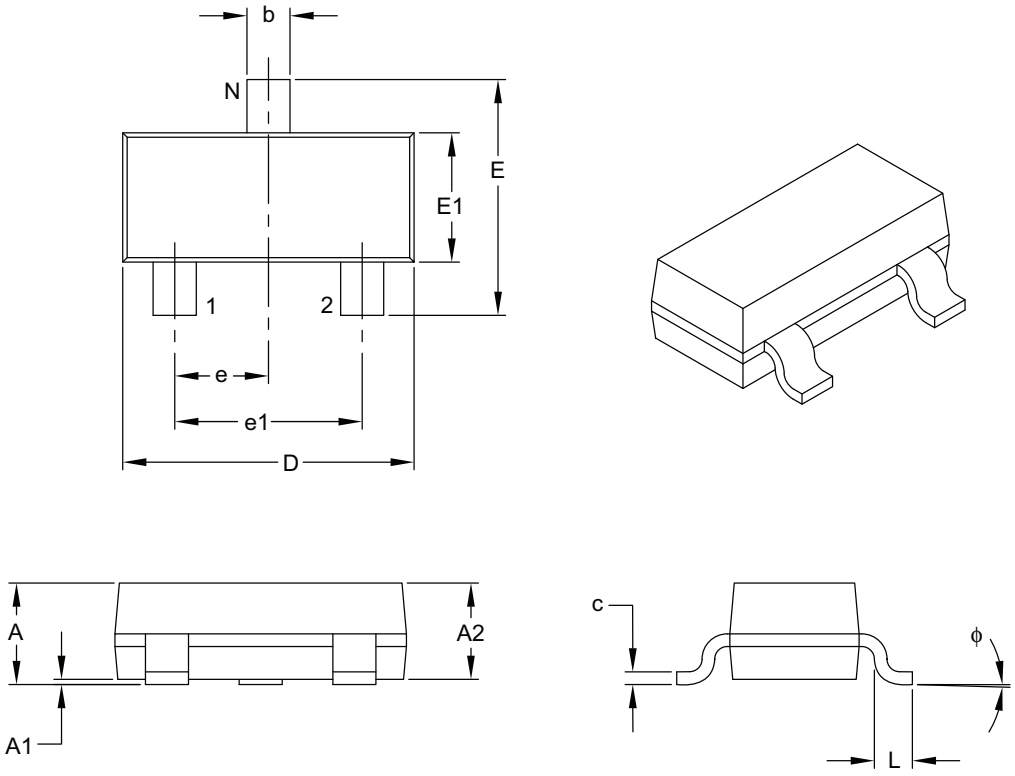
Part Number	Code
MCP1811AT-010/HCA	AA
MCP1811AT-012/HCA	AE
MCP1811AT-018/HCA	AJ
MCP1811AT-020/HCA	AN
MCP1811AT-025/HCA	AS
MCP1811AT-028/HCA	BN
MCP1811AT-030/HCA	AW
MCP1811AT-033/HCA	BA
MCP1811AT-040/HCA	▲H2
MCP1811BT-010/HCA	AB
MCP1811BT-012/HCA	AF
MCP1811BT-018/HCA	AK
MCP1811BT-020/HCA	AP
MCP1811BT-025/HCA	AT
MCP1811BT-028/HCA	BP
MCP1811BT-030/HCA	AX
MCP1811BT-033/HCA	BB
MCP1811BT-040/HCA	▲H3
MCP1812AT-010/HCA	AC
MCP1812AT-012/HCA	AG
MCP1812AT-018/HCA	AL
MCP1812AT-020/HCA	AQ
MCP1812AT-025/HCA	AU
MCP1812AT-028/HCA	BK
MCP1812AT-030/HCA	AY
MCP1812AT-033/HCA	BC
MCP1812AT-040/HCA	▲H4
MCP1812BT-010/HCA	AD
MCP1812BT-012/HCA	AH
MCP1812BT-018/HCA	AM
MCP1812BT-020/HCA	AR
MCP1812BT-025/HCA	AV
MCP1812BT-028/HCA	BL
MCP1812BT-030/HCA	AZ
MCP1812BT-033/HCA	BD
MCP1812BT-040/HCA	▲H5

Example



3-Lead Plastic Small Outline Transistor (TT) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		3	
Lead Pitch	e		0.95 BSC	
Outside Lead Pitch	e1		1.90 BSC	
Overall Height	A	0.89	–	1.12
Molded Package Thickness	A2	0.79	0.95	1.02
Standoff	A1	0.01	–	0.10
Overall Width	E	2.10	–	2.64
Molded Package Width	E1	1.16	1.30	1.40
Overall Length	D	2.67	2.90	3.05
Foot Length	L	0.13	0.50	0.60
Foot Angle	ϕ	0°	–	10°
Lead Thickness	c	0.08	–	0.20
Lead Width	b	0.30	–	0.54

Notes:

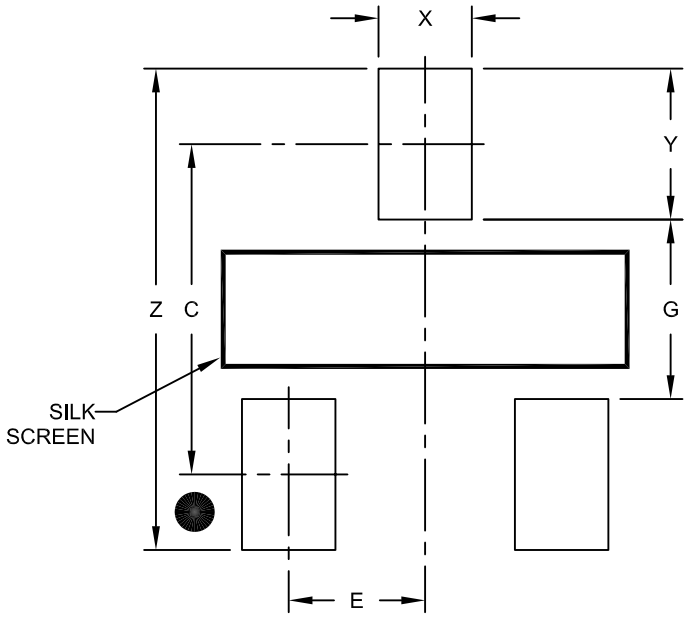
1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-104B

3-Lead Plastic Small Outline Transistor (TT) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.95 BSC	
Contact Pad Spacing	C		2.30	
Contact Pad Width (X3)	X			0.65
Contact Pad Length (X3)	Y			1.05
Distance Between Pads	G	1.25		
Overall Width	Z			3.35

Notes:

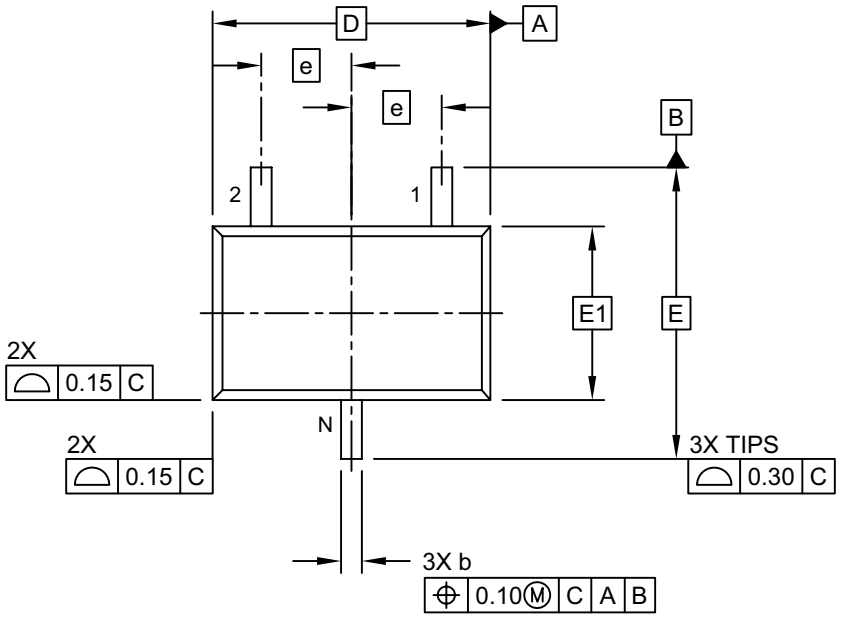
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

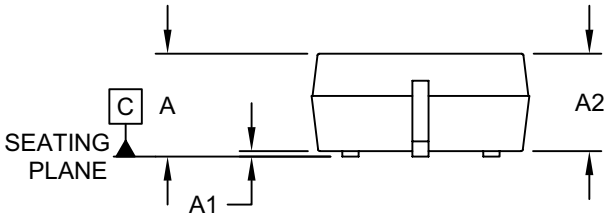
Microchip Technology Drawing No. C04-2104A

3-Lead Plastic Small Outline Transistor (LB) [SC70]

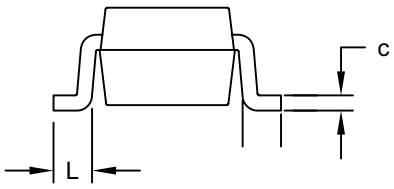
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW

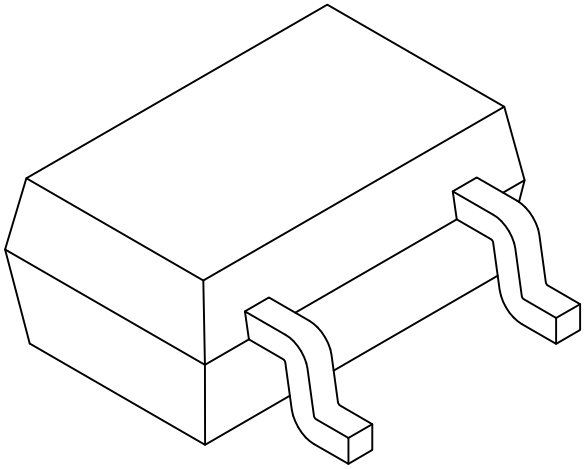


END VIEW

Microchip Technology Drawing C04-060C Sheet 1 of 2

3-Lead Plastic Small Outline Transistor (LB) [SC70]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		3	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	-	1.10
Standoff	A1	0.00	-	0.10
Molded Package Thickness	A2	0.80	-	1.00
Overall Length	D		2.00 BSC	
Exposed Pad Length	D2	2.50	2.60	2.70
Overall Width	E		2.10 BSC	
Exposed Pad Width	E1		1.25 BSC	
Terminal Width	b	0.15	-	0.40
Terminal Length	L	0.10	0.20	0.46
Lead Thickness	c	0.20	-	0.26

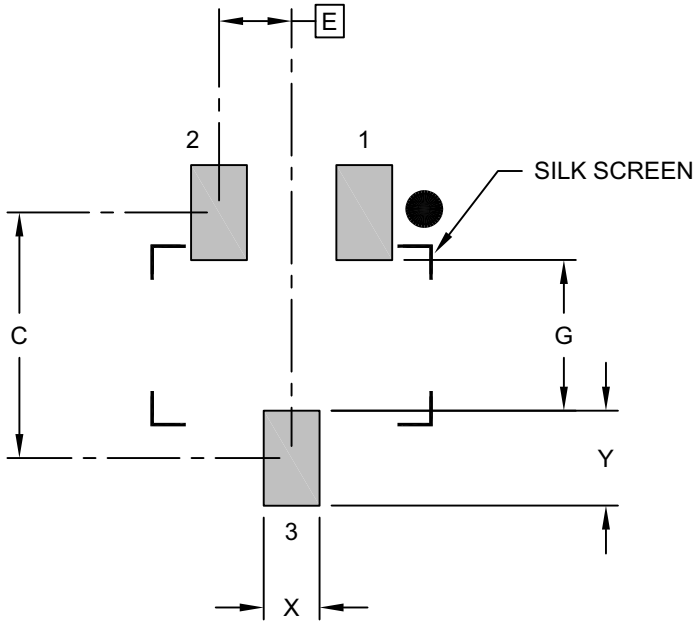
Notes:

1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-060C Sheet 2 of 2

3-Lead Plastic Small Outline Transistor (LB) [SC70]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C		2.20	
Contact Pad Width	X			0.50
Contact Pad Length	Y			0.85
Distance Between Pads	G	1.25		

Notes:

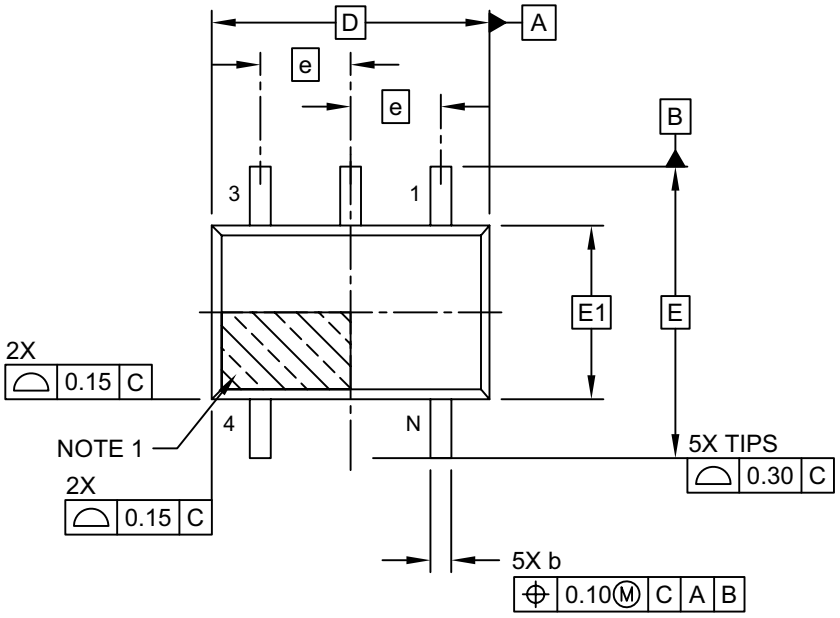
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

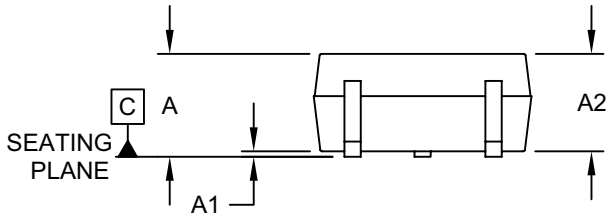
Microchip Technology Drawing No. C04-2060B

5-Lead Plastic Small Outline Transistor (LT) [SC70]

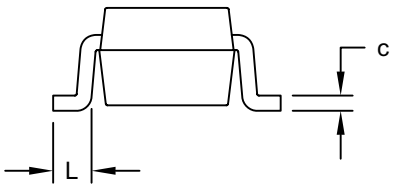
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW

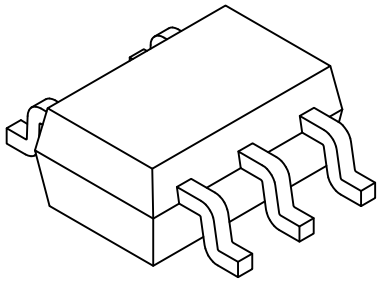


END VIEW

Microchip Technology Drawing C04-061D Sheet 1 of 2

5-Lead Plastic Small Outline Transistor (LT) [SC70]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		5	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	-	1.10
Standoff	A1	0.00	-	0.10
Molded Package Thickness	A2	0.80	-	1.00
Overall Length	D		2.00 BSC	
Exposed Pad Length	D2	2.50	2.60	2.70
Overall Width	E		2.10 BSC	
Exposed Pad Width	E1		1.25 BSC	
Terminal Width	b	0.15	-	0.40
Terminal Length	L	0.10	0.20	0.46
Lead Thickness	c	0.08	-	0.26

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M

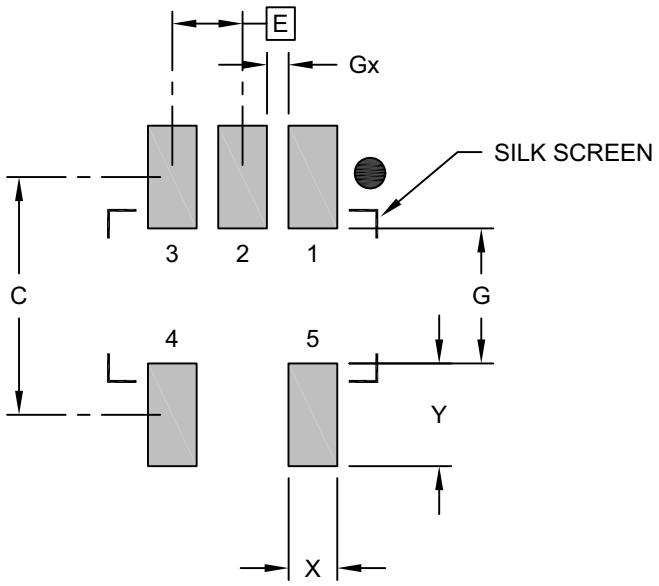
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-061D Sheet 2 of 2

5-Lead Plastic Small Outline Transistor (LT) [SC70]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Contact Pad Spacing	C		2.20	
Contact Pad Width	X			0.45
Contact Pad Length	Y			0.95
Distance Between Pads	G	1.25		
Distance Between Pads	Gx	0.20		

Notes:

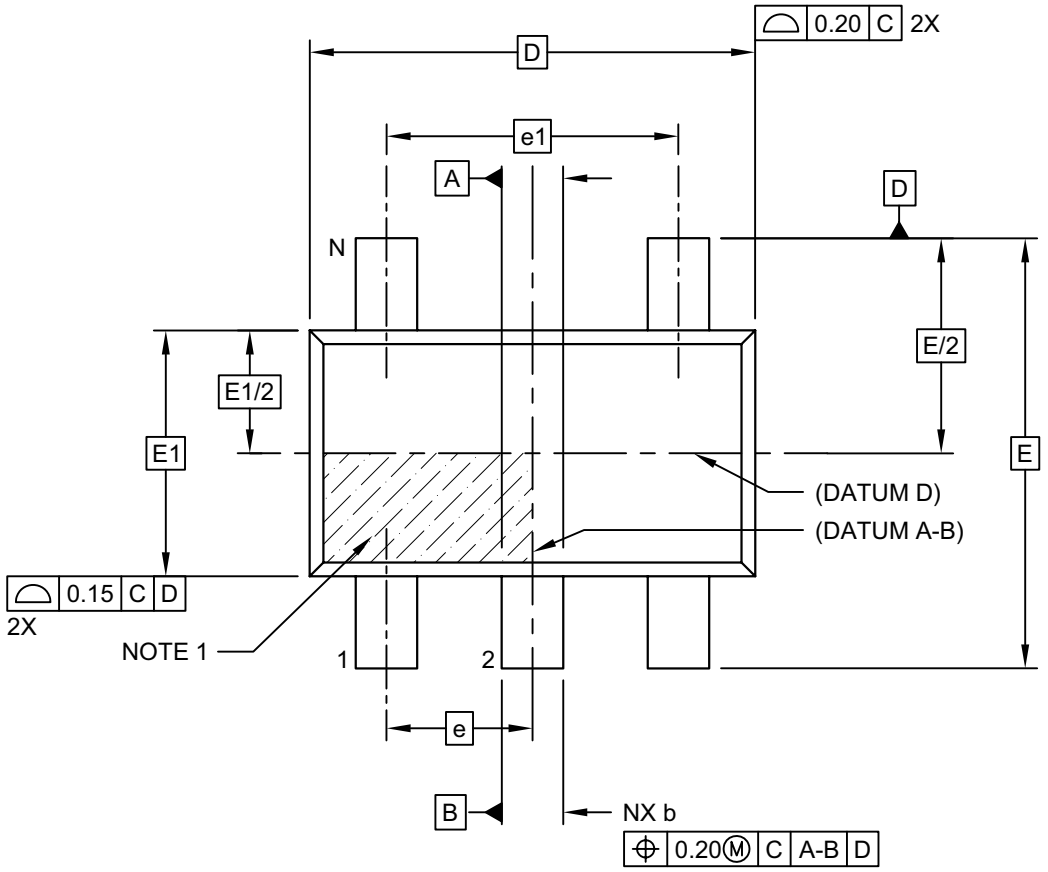
1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

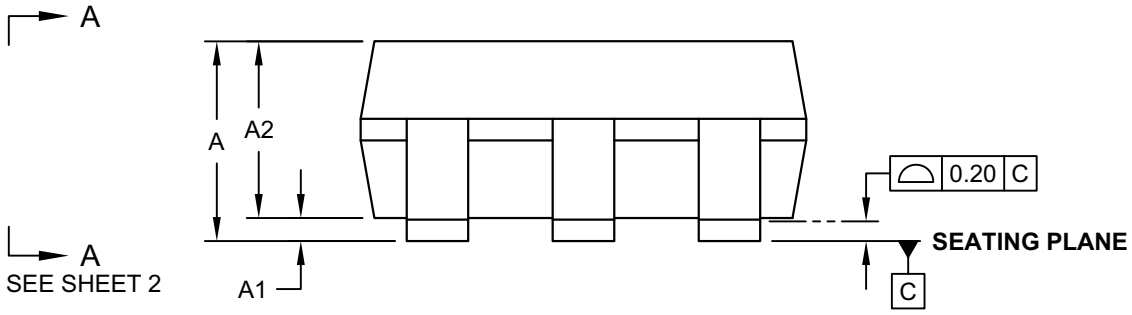
Microchip Technology Drawing No. C04-2061B

5-Lead Plastic Small Outline Transistor (OT) [SOT23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW

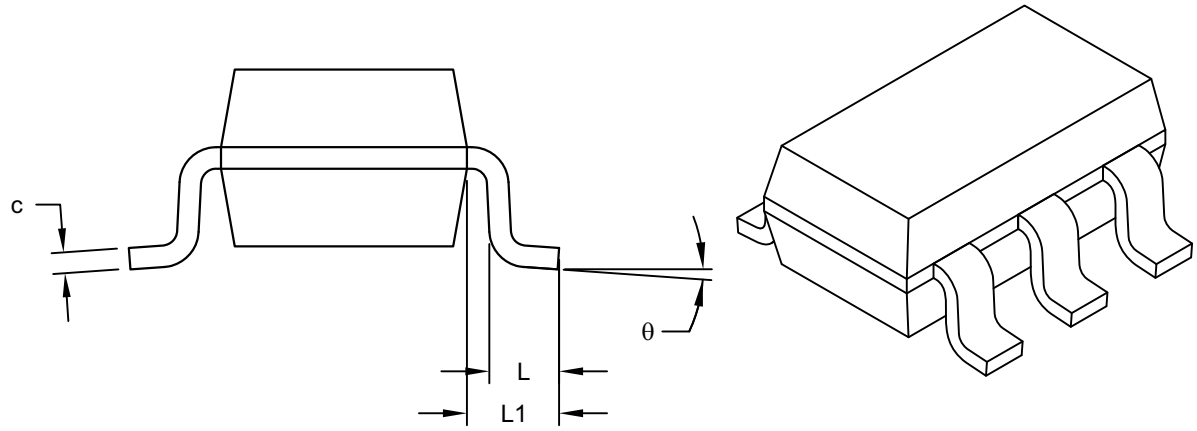


SIDE VIEW

Microchip Technology Drawing C04-091-OT Rev E Sheet 1 of 2

5-Lead Plastic Small Outline Transistor (OT) [SOT23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



VIEW A-A
SHEET 1

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		5	
Pitch	e		0.95 BSC	
Outside lead pitch	e1		1.90 BSC	
Overall Height	A	0.90	-	1.45
Molded Package Thickness	A2	0.89	-	1.30
Standoff	A1	-	-	0.15
Overall Width	E		2.80 BSC	
Molded Package Width	E1		1.60 BSC	
Overall Length	D		2.90 BSC	
Foot Length	L	0.30	-	0.60
Footprint	L1		0.60 REF	
Foot Angle	ϕ	0°	-	10°
Lead Thickness	c	0.08	-	0.26
Lead Width	b	0.20	-	0.51

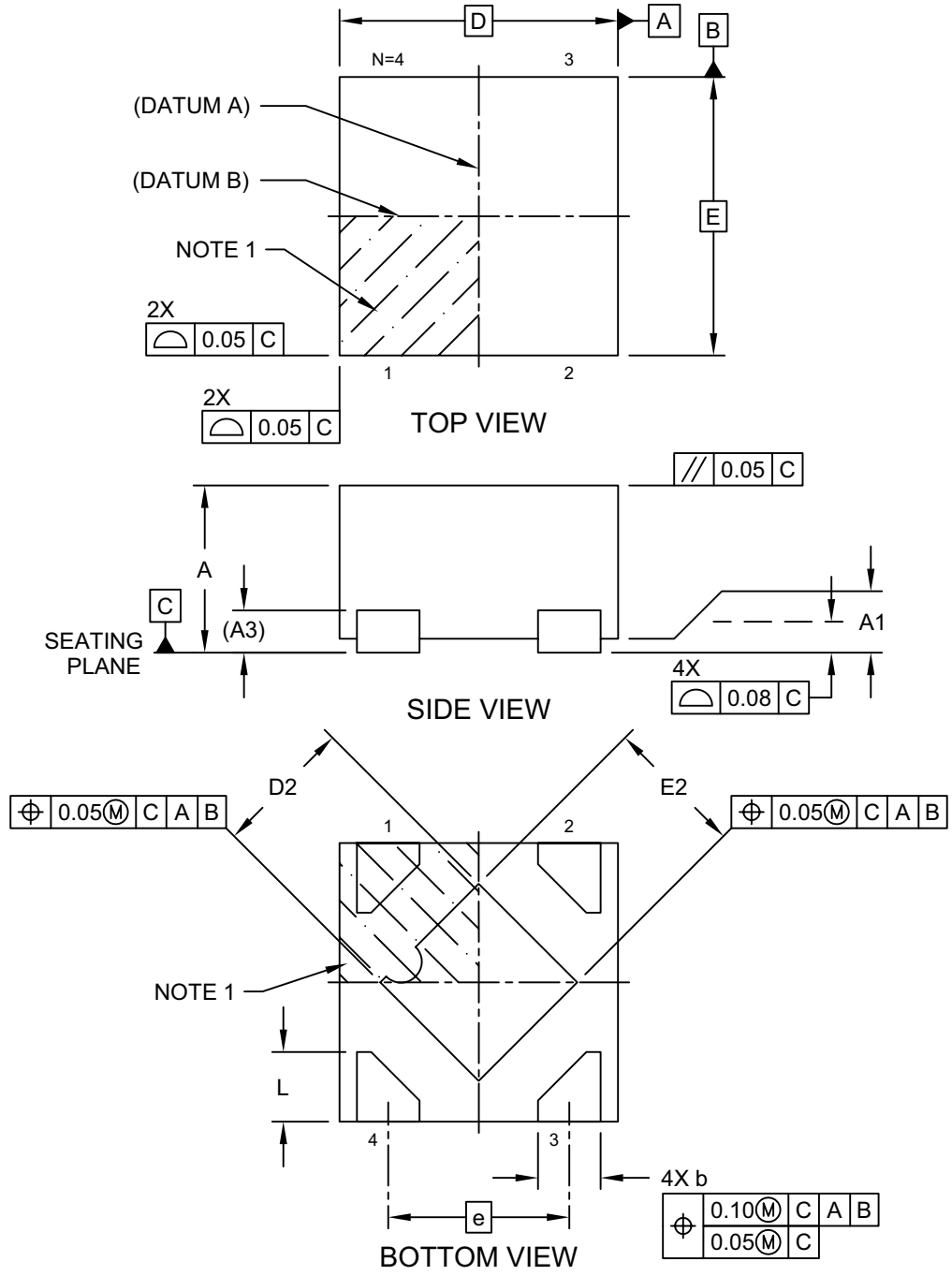
Notes:

1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-091-OT Rev E Sheet 2 of 2

4-Lead Ultra Thin Plastic Dual Flat, No Lead Package (HCA) - 1x1 mm Body [UDFN]

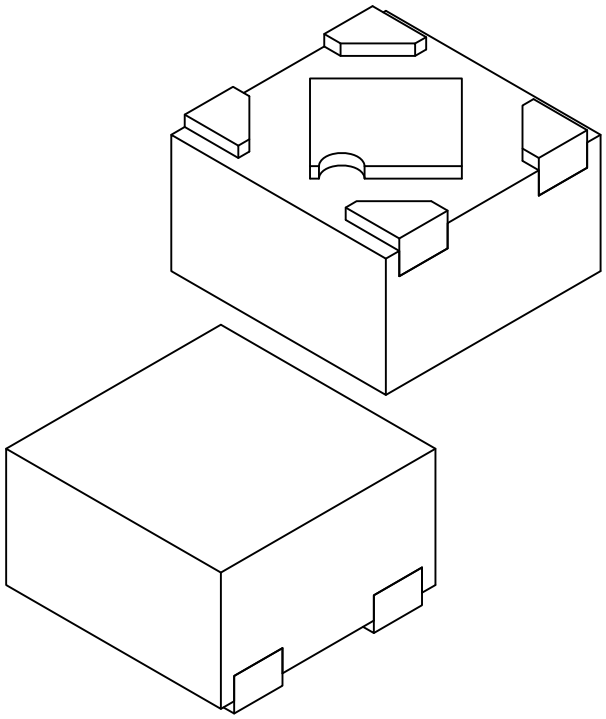
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-1149 Rev A Sheet 1 of 2

4-Lead Ultra Thin Plastic Dual Flat, No Lead Package (HCA) - 1x1 mm Body [UDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		4	
Pitch	e		0.65 BSC	
Overall Height	A	0.50	0.55	0.60
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.152 REF	
Overall Length	D		1.00 BSC	
Exposed Pad Length	D2	0.45	0.50	0.55
Overall Width	E		1.00 BSC	
Exposed Pad Width	E2	0.45	0.50	0.55
Terminal Width	b	0.175	0.225	0.275
Terminal Length	L	0.20	0.25	0.30

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

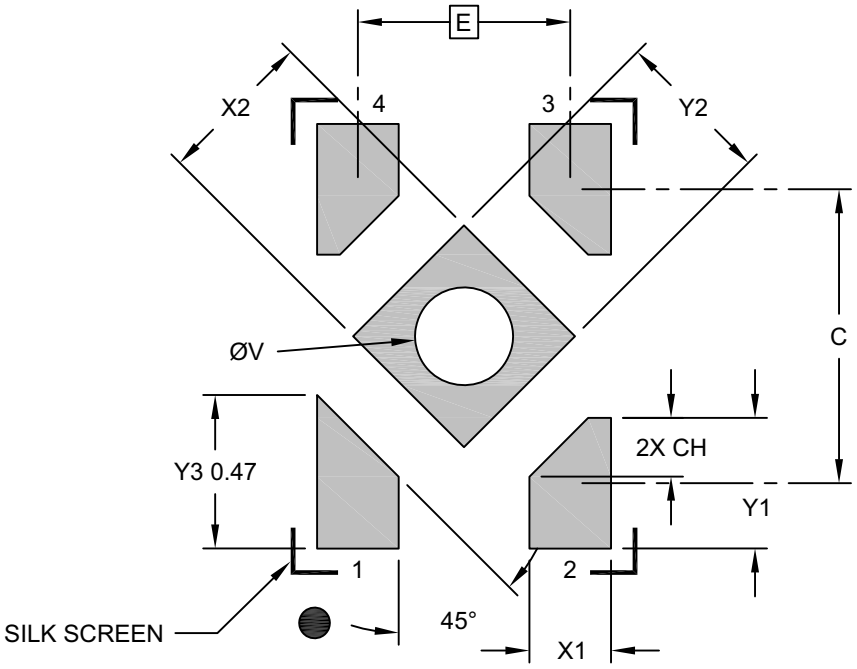
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1149 Rev A Sheet 2 of 2

4-Lead Ultra Thin Plastic Dual Flat, No Lead Package (HCA) - 1x1 mm Body [UDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Center Pad Width	X2			0.48
Center Pad Length	Y2			0.48
Contact Pad Spacing	C		0.90	
Contact Pad Width (X4)	X1			0.25
Contact Pad Length (X3)	Y1			0.40
Terminal 1 Pad Length	Y3			0.47
Contact Pad Chamfer (X3)	CH		0.18	
Thermal Via Diameter	V		0.30	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-3149 Rev A

APPENDIX A: REVISION HISTORY

Revison B (March 2019)

The following is the list of modifications:

1. Updated **Description**.
1. Updated **Package Marking Information**.
2. Updated **Product Identification System**.

Revision A (September 2018)

- Initial release of this document

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X(1)	–	XX	/XX
Device	Tape and Reel Option		Output Voltage	Package

Device:	MCP1811AT: Ultra-Low Quiescent Current LDO Regulator for Long-Life Battery-Powered Applications, Tape and Reel		
Tape and Reel Option:	Blank	=	Standard packaging (tube or tray)
	T	=	Tape and Reel(1)
Standard Output Voltages*	010	=	1V
	012	=	1.2V
	018	=	1.8V
	020	=	2.0V
	025	=	2.5V
	028	=	2.8V
	030	=	3.0V
	033	=	3.3V
	040	=	4.0V
Package:	TT	=	3-Lead Plastic Small Outline Transistor (SOT-23)
	LB	=	3-Lead Plastic Small Outline Transistor (SC70)
	LT	=	5-Lead Plastic Small Outline Transistor (SC70)
	OT	=	5-Lead Plastic Small Outline Transistor (SOT-23)
	HCA	=	4-Lead Plastic Ultra Thin Quad Flatpack, No Lead Package (UDFN)

Examples:

a) MCP1811AT-010/LB: Tape and Reel, 1V Output Voltage, 3-Lead SC70 package

b) MCP1811BT-020/LB: Tape and Reel, 2V Output Voltage, 3-Lead SC70 package

c) MCP1811AT-040/OT: Tape and Reel 4.0V Output Voltage, 5-Lead SOT-23 package

d) MCP1812BT-025/HCA: Tape and Reel, 2.5V Output Voltage, 4-Lead UDFN package

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

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