

NPN Silicon Planar Darlington Transistor
for general NF applications

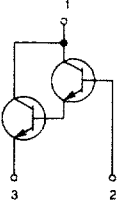
As complementary type, the PNP transistor BCV26 is recommended.

Features

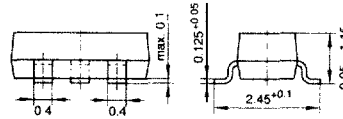
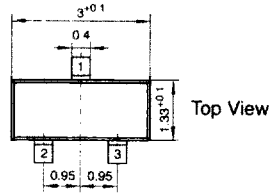
- high collector current
- high current gain

Pin configuration

1 = Collector, 2 = Base, 3 = Emitter



Marking
FF



SOT-23 Plastic Package
Weight approx. 0.008 g
Dimensions in mm

Absolute Maximum Ratings

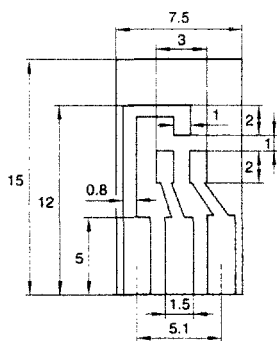
	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	30	V
Collector-Base Voltage	V_{CBO}	40	V
Emitter-Base Voltage	V_{EBO}	10	V
Collector Current	I_C	300	mA
Peak Collector Current	I_{CM}	800	mA
Base Current	I_B	100	mA
Power Dissipation at $T_{SB} = 50\text{ }^\circ\text{C}$	P_{tot}	300 ¹⁾	mW
Junction Temperature	T_j	150	$^\circ\text{C}$
Storage Temperature Range	T_S	-65 to +150	$^\circ\text{C}$

¹⁾ Device on fiberglass substrate, see layout

Characteristics at $T_{amb} = 25\text{ }^{\circ}\text{C}$

	Symbol	Min.	Typ.	Max.	Unit
Collector-Base Cutoff Current at $V_{CBO} = 30\text{ V}$	I_{CBO}	-	-	0.1	μA
Emitter-Base Cutoff Current at $V_{EB} = 10\text{ V}$	I_{EBO}	-	-	0.1	μA
Collector-Emitter Breakdown Voltage at $I_C = 10\text{ mA}$	$V_{(BR)CEO}$	30	-	-	V
Collector-Base Breakdown Voltage at $I_C = 10\text{ }\mu\text{A}$	$V_{(BR)CBO}$	40	-	-	V
Emitter-Base Breakdown Voltage at $I_E = 100\text{ nA}$	$V_{(BR)EBO}$	10	-	-	V
DC Current Gain at $V_{CE} = 5\text{ V}$, $I_C = 1\text{ mA}$ at $V_{CE} = 5\text{ V}$, $I_C = 10\text{ mA}$ at $V_{CE} = 5\text{ V}$, $I_C = 100\text{ mA}$	h_{FE} h_{FE} h_{FE}	4000 10000 20000	- - -	- - -	- - -
Collector-Emitter Saturation Voltage at $I_C = 100\text{ mA}$, $I_B = 0.1\text{ mA}$	V_{CEsat}	-	-	1.0	V
Base-Emitter Saturation Voltage at $I_C = 100\text{ mA}$, $I_B = 0.1\text{ mA}$	V_{BEsat}	-	-	1.5	V
Gain-Bandwidth Product at $V_{CE} = 5\text{ V}$, $I_C = 30\text{ mA}$, $f = 100\text{ MHz}$	f_T	-	220	-	MHz
Collector-Base Capacitance at $V_{CB} = 30\text{ V}$, $I_E = 0$, $f = 1\text{ MHz}$	C_{CBO}	-	3.5	-	pF
Thermal Resistance Junction to Ambient Air	R_{thA}	-	-	430 ¹⁾	K/W

¹⁾ Device on fiberglass substrate, see layout below

Layout for R_{thA} test

Thickness: Fiberglass 1.5 mm
Copper leads 0.3 mm