

54AC/74AC251 • 54ACT/74ACT251 8-Input Multiplexer with TRI-STATE® Output

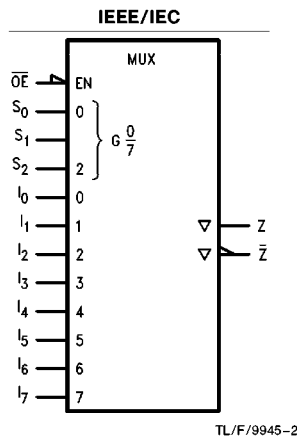
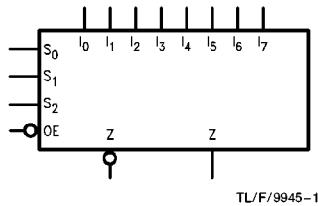
General Description

The 'AC/'ACT251 is a high-speed 8-input digital multiplexer. It provides, in one package, the ability to select one bit of data from up to eight sources. It can be used as universal function generator to generate any logic function of four variables. Both true and complementary outputs are provided.

Features

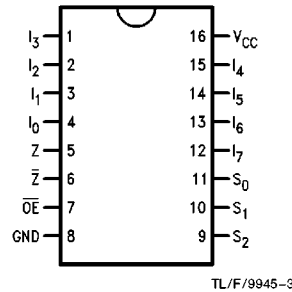
- I_{CC} reduced by 50%
- Multifunctional capability
- On-chip select logic decoding
- Inverting and noninverting TRI-STATE outputs
- Outputs source/sink 24 mA
- 'ACT251 has TTL-compatible inputs
- Standard Military Drawing (SMD)
 - 'AC251: 5962-87692
 - 'ACT251: 5962-89599

Logic Symbols

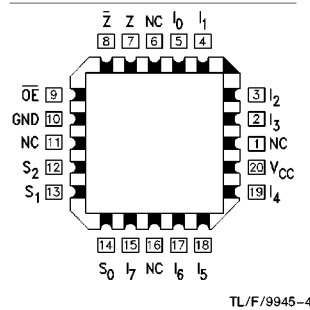


Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



Pin Assignment for LCC



Pin Names	Description
S ₀ -S ₂	Select Inputs
OE	TRI-STATE Output Enable Input
I ₀ -I ₇	Multiplexer Inputs
Z	TRI-STATE Multiplexer Output
Z̄	Complementary TRI-STATE Multiplexer Output

TRI-STATE® is a registered trademark of National Semiconductor Corporation.
FACT™ is a trademark of National Semiconductor Corporation.

54AC/74AC251 • 54ACT/74ACT251 8-Input Multiplexer with TRI-STATE Output

Functional Description

This device is a logical implementation of a single-pole, 8-position switch with the switch position controlled by the state of three Select inputs, S_0 , S_1 , S_2 . Both true and complementary outputs are provided. The Output Enable input (\overline{OE}) is active LOW. When it is activated, the logic function provided at the output is:

$$Z = \overline{OE} \cdot (I_0 \cdot \overline{S_0} \cdot \overline{S_1} \cdot \overline{S_2} + I_1 \cdot S_0 \cdot \overline{S_1} \cdot \overline{S_2} + I_2 \cdot \overline{S_0} \cdot S_1 \cdot \overline{S_2} + I_3 \cdot S_0 \cdot S_1 \cdot \overline{S_2} + I_4 \cdot \overline{S_0} \cdot \overline{S_1} \cdot S_2 + I_5 \cdot S_0 \cdot \overline{S_1} \cdot S_2 + I_6 \cdot \overline{S_0} \cdot S_1 \cdot S_2 + I_7 \cdot S_0 \cdot S_1 \cdot S_2)$$

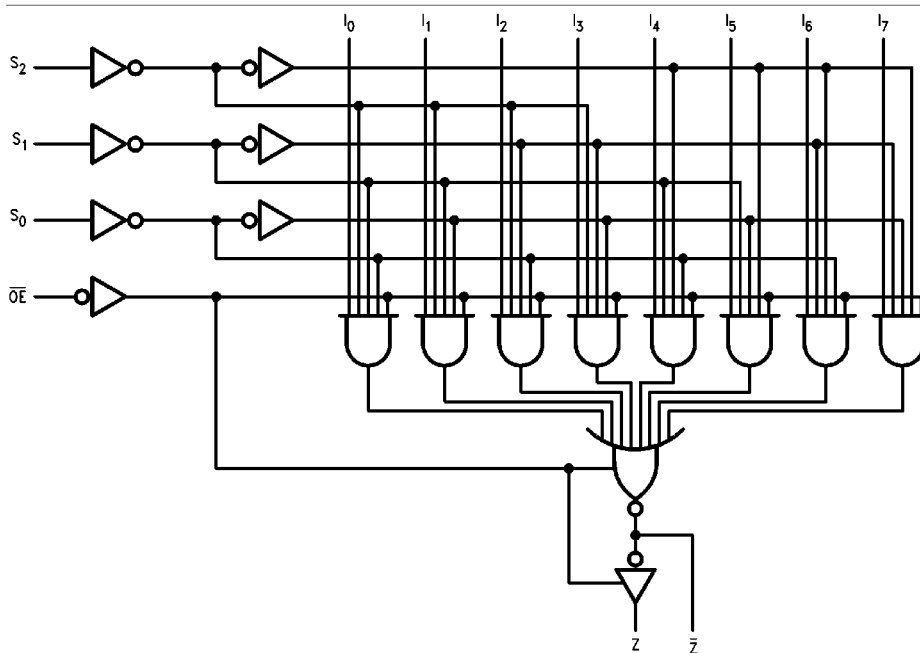
When the Output Enable is HIGH, both outputs are in the high impedance (High Z) state. This feature allows multiplexer expansion by tying the outputs of up to 128 devices together. When the outputs of the TRI-STATE devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. The Output Enable signals should be designed to ensure there is no overlap in the active-LOW portion of the enable voltages.

Truth Table

\overline{OE}	Inputs			Outputs	
	S_2	S_1	S_0	\overline{Z}	Z
H	X	X	X	Z	Z
L	L	L	L	$\overline{I_0}$	I_0
L	L	L	H	$\overline{I_1}$	I_1
L	L	H	L	$\overline{I_2}$	I_2
L	L	H	H	$\overline{I_3}$	I_3
L	H	L	L	$\overline{I_4}$	I_4
L	H	L	H	$\overline{I_5}$	I_5
L	H	H	L	$\overline{I_6}$	I_6
L	H	H	H	$\overline{I_7}$	I_7

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
 Z = High Impedance

Logic Diagram



TL/F/9945-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	-0.5V to +7.0V
DC Input Diode Current (I_{IK})	
$V_I = -0.5V$	-20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage (V_I)	-0.5V to $V_{CC} + 0.5V$
DC Output Diode Current (I_{OK})	
$V_O = -0.5V$	-20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage (V_O)	-0.5V to $V_{CC} + 0.5V$
DC Output Source or Sink Current (I_O)	± 50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	± 50 mA
Storage Temperature (T_{STG})	-65°C to +150°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	-40°C to +85°C
54AC/ACT	-55°C to +125°C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
'AC Devices	
V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
'ACT Devices	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC		54AC		74AC		Units	Conditions
			$T_A = +25^\circ\text{C}$		$T_A = -55^\circ\text{C to } +125^\circ\text{C}$		$T_A = -40^\circ\text{C to } +85^\circ\text{C}$			
			Typ	Guaranteed Limits						
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1		2.1		V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		4.5	2.25	3.15	3.15		3.15			
		5.5	2.75	3.85	3.85		3.85			
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9		0.9		V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		4.5	2.25	1.35	1.35		1.35			
		5.5	2.75	1.65	1.65		1.65			
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9		2.9		V	$I_{OUT} = -50 \mu\text{A}$
		4.5	4.49	4.4	4.4		4.4			
		5.5	5.49	5.4	5.4		5.4			
V_{OL}	Maximum Low Level Output Voltage	3.0		2.56	2.4		2.46		V	* $V_{IN} = V_{IL}$ or V_{IH} -12 mA $I_{OH} = -24 \text{ mA}$ -24 mA
		4.5		3.86	3.7		3.76			
		5.5		4.86	4.7		4.76			
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1		0.1		V	$I_{OUT} = 50 \mu\text{A}$
		4.5	0.001	0.1	0.1		0.1			
		5.5	0.001	0.1	0.1		0.1			
V_{OL}	Maximum Low Level Output Voltage	3.0		0.36	0.50		0.44		V	* $V_{IN} = V_{IL}$ or V_{IH} 12 mA $I_{OL} = 24 \text{ mA}$ 24 mA
		4.5		0.36	0.50		0.44			
		5.5		0.36	0.50		0.44			
I_{IN}	Maximum Input Leakage Current	5.5		± 0.1	± 1.0		± 1.0		μA	$V_I = V_{CC}, \text{GND}$

*All outputs loaded; thresholds on input associated with output under test.

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V _{CC} (V)	74AC		54AC		74AC		Units	Conditions
			T _A = +25°C		T _A = -55°C to +125°C		T _A = -40°C to +85°C			
			Typ	Guaranteed Limits						
I _{OZ}	Maximum TRI-STATE® Current	5.5		±0.5	±10.0	±10.0	±5.0	±5.0	μA	V _I (OE) = V _{IL} , V _{IH} V _I = V _{CC} , V _{GND} V _O = V _{CC} , GND
I _{OLD}	†Minimum Dynamic Output Current	5.5			50	50	75	75	mA	V _{OLD} = 1.65V Max
I _{OHD}		5.5			-50	-50	-75	-75	mA	V _{OHD} = 3.85V Min
I _{CC}	Maximum Quiescent Supply Current	5.5		4.0	80.0	80.0	40.0	40.0	μA	V _{IN} = V _{CC} or GND

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.

I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V _{CC} (V)	74ACT		54ACT		74ACT		Units	Conditions
			T _A = +25°C		T _A = -55°C to +125°C		T _A = -40°C to +85°C			
			Typ	Guaranteed Limits						
V _{IH}	Minimum High Level Input Voltage	4.5	1.5	2.0	2.0	2.0	2.0	2.0	V	V _{OUT} = 0.1V or V _{CC} - 0.1V
		5.5	1.5	2.0	2.0	2.0	2.0	2.0		
V _{IL}	Maximum Low Level Input Voltage	4.5	1.5	0.8	0.8	0.8	0.8	0.8	V	V _{OUT} = 0.1V or V _{CC} - 0.1V
		5.5	1.5	0.8	0.8	0.8	0.8	0.8		
V _{OH}	Minimum High Level Output Voltage	4.5	4.49	4.4	4.4	4.4	4.4	4.4	V	I _{OUT} = -50 μA
		5.5	5.49	5.4	5.4	5.4	5.4	5.4		
		4.5		3.86	3.70	3.76	3.76	3.76	V	*V _{IN} = V _{IL} or V _{IH} -24 mA I _{OH} -24 mA
		5.5		4.86	4.70	4.76	4.76	4.76		
V _{OL}	Maximum Low Level Output Voltage	4.5	0.001	0.1	0.1	0.1	0.1	0.1	V	I _{OUT} = 50 μA
		5.5	0.001	0.1	0.1	0.1	0.1	0.1		
		4.5		0.36	0.50	0.44	0.44	0.44	V	*V _{IN} = V _{IL} or V _{IH} 24 mA I _{OL} 24 mA
		5.5		0.36	0.50	0.50	0.44	0.44		
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	±1.0	±1.0	μA	V _I = V _{CC} , GND
I _{OZ}	Maximum TRI-STATE® Current	5.5		±0.5	±10.0	±10.0	±5.0	±5.0	μA	V _I = V _{IL} , V _{IH} V _O = V _{CC} , GND
I _{CC} T	Maximum I _{CC} /Input	5.5	0.6		1.6	1.6	1.5	1.5	mA	V _I = V _{CC} - 2.1V
I _{OLD}	†Minimum Dynamic Output Current	5.5			50	50	75	75	mA	V _{OLD} = 1.65V Max
I _{OHD}		5.5			-50	-50	-75	-75	mA	V _{OHD} = 3.85V Min
I _{CC}	Maximum Quiescent Supply Current	5.5		4.0	80.0	80.0	40.0	40.0	μA	V _{IN} = V _{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics

Symbol	Parameter	V _{CC} * (V)	74AC			54AC		74AC		Units
			T _A = +25°C C _L = 50 pF			T _A = -55°C to +125°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF		
			Min	Typ	Max	Min	Max	Min	Max	
t _{PLH}	Propagation Delay S _n to Z or \bar{Z}	3.3 5.0	1.5 1.5	11.5 8.5	17.5 12.5	1.0 1.0	21.0 15.5	1.5 1.5	19.0 13.5	ns
t _{PHL}	Propagation Delay S _n to Z or \bar{Z}	3.3 5.0	1.5 1.5	11.0 8.0	17.5 12.5	1.0 1.0	21.0 15.5	1.5 1.5	19.0 13.5	ns
t _{PLH}	Propagation Delay I _n to Z or \bar{Z}	3.3 5.0	1.5 1.5	10.0 7.0	14.0 10.0	1.0 1.0	17.0 12.0	1.5 1.5	15.5 11.0	ns
t _{PHL}	Propagation Delay I _n to Z or \bar{Z}	3.3 5.0	1.5 1.5	9.0 6.5	14.0 10.0	1.0 1.0	16.5 12.0	1.5 1.5	15.5 11.0	ns
t _{PZH}	Output Enable Time $\bar{O}E$ to Z or \bar{Z}	3.3 5.0	1.5 1.5	7.5 5.5	11.0 8.0	1.0 1.0	13.0 10.0	1.5 1.5	12.0 9.0	ns
t _{PZL}	Output Enable Time $\bar{O}E$ to Z or \bar{Z}	3.3 5.0	1.5 1.5	7.5 5.5	11.0 8.0	1.0 1.0	13.0 10.0	1.5 1.5	12.0 9.0	ns
t _{PHZ}	Output Disable Time $\bar{O}E$ to Z or \bar{Z}	3.3 5.0	1.5 1.5	8.5 7.0	11.5 9.5	3.5 2.5	14.0 11.0	1.5 1.5	13.0 10.0	ns
t _{PLZ}	Output Disable Time $\bar{O}E$ to Z or \bar{Z}	3.3 5.0	1.5 1.5	7.0 5.5	11.0 8.0	4.0 3.0	13.0 10.0	1.5 1.5	12.0 8.5	ns

*Voltage Range 3.3 is 3.3V ± 0.3V
Voltage Range 5.0 is 5.0V ± 0.5V

AC Electrical Characteristics

Symbol	Parameter	V _{CC} * (V)	74ACT			54ACT		74ACT		Units
			T _A = +25°C C _L = 50 pF			T _A = -55°C to +125°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF		
			Min	Typ	Max	Min	Max	Min	Max	
t _{PLH}	Propagation Delay S _n to Z or \bar{Z}	5.0	2.5	7.0	15.5	1.0	18.5	2.0	17.0	ns
t _{PHL}	Propagation Delay S _n to Z or \bar{Z}	5.0	2.5	7.5	16.5	1.0	19.5	2.5	18.5	ns
t _{PLH}	Propagation Delay I _n to Z or \bar{Z}	5.0	2.5	5.5	12.0	1.0	14.0	2.0	13.0	ns
t _{PHL}	Propagation Delay I _n to Z or \bar{Z}	5.0	2.5	6.5	12.5	1.0	15.0	2.5	14.0	ns
t _{PZH}	Output Enable Time $\bar{O}E$ to Z or \bar{Z}	5.0	1.5	5.0	8.5	1.0	10.0	1.5	9.0	ns
t _{PZL}	Output Enable Time $\bar{O}E$ to Z or \bar{Z}	5.0	1.5	4.5	8.5	1.0	10.0	1.5	9.5	ns
t _{PHZ}	Output Disable Time $\bar{O}E$ to Z or \bar{Z}	5.0	2.0	6.0	12.0	1.0	13.5	2.0	13.0	ns
t _{PLZ}	Output Disable Time $\bar{O}E$ to Z or \bar{Z}	5.0	1.5	4.5	8.5	1.0	9.5	1.5	9.0	ns

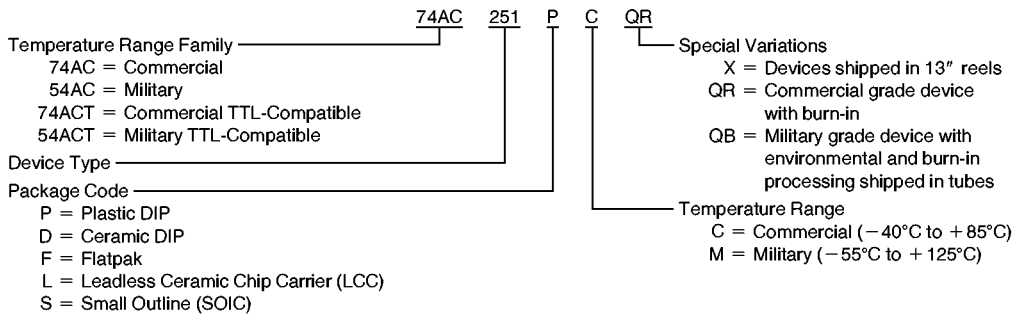
*Voltage Range 5.0 is 5.0V ± 0.5V

Capacitance

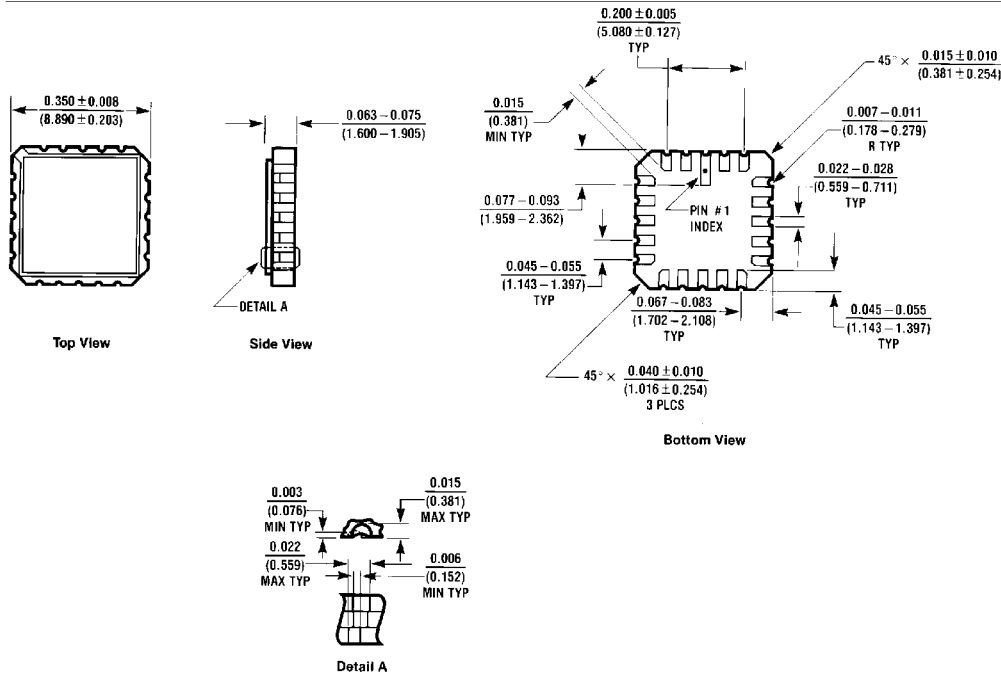
Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = OPEN$
C_{PD}	Power Dissipation Capacitance	70.0	pF	$V_{CC} = 5.0V$

Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



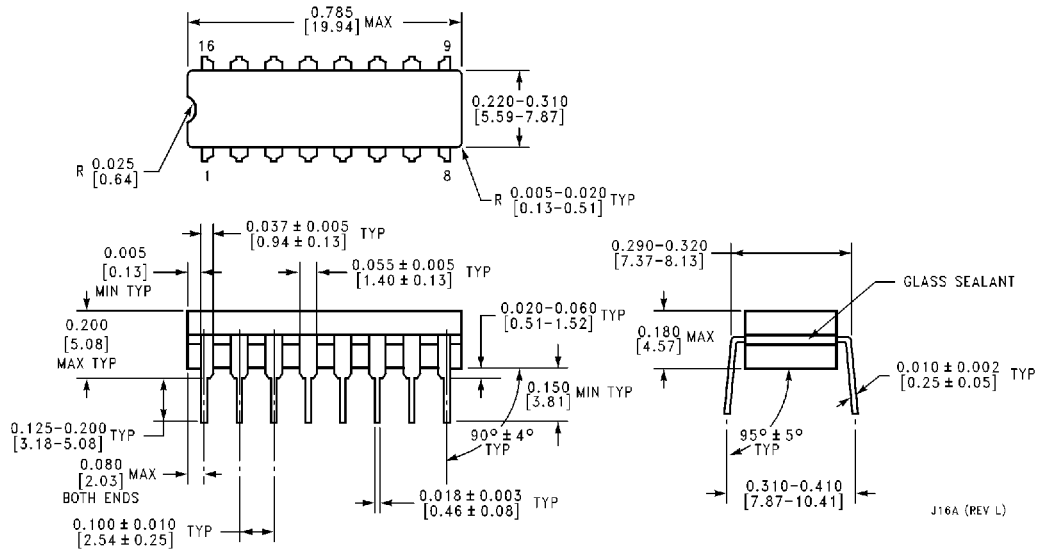
Physical Dimensions inches (millimeters)



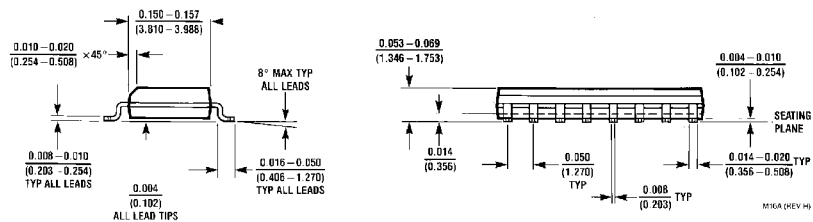
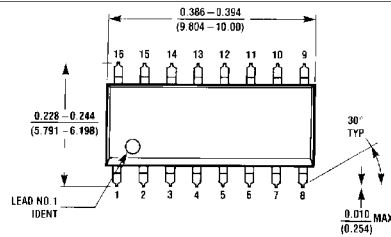
20 Terminal Ceramic Leadless Chip Carrier (L)
NS Package Number E20A

E20A (REV D)

Physical Dimensions inches (millimeters) (Continued)

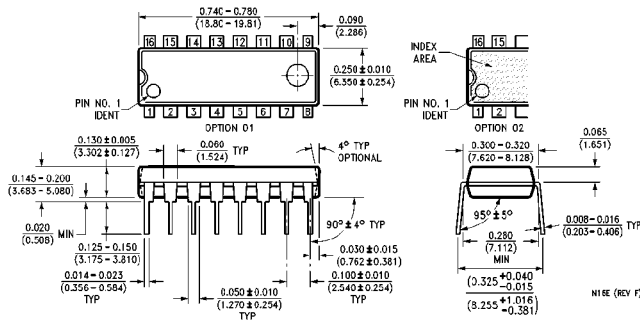


**16 Lead Ceramic Dual-In-Line Package (D)
 NS Package Number J16A**

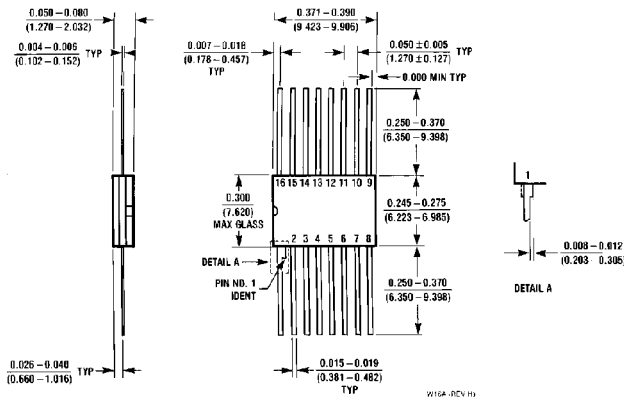


**16 Lead Small Outline Integrated Circuit (S)
 NS Package Number M16A**

Physical Dimensions inches (millimeters) (Continued)



**16 Lead Plastic Dual-In-Line Package (P)
NS Package Number N16E**



**16 Lead Ceramic Flatpak (F)
NS Package Number W16A**

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



National Semiconductor Corporation
2900 Semiconductor Drive
P.O. Box 58090
Santa Clara, CA 95052-8090
Tel: 1(800) 272-9959
TWX: (910) 339-9240

National Semiconductor GmbH
Livy-Gargan-Str. 10
D-82256 Fürstenfeldbruck
Germany
Tel: (81-41) 35-0
Telex: 527649
Fax: (81-41) 35-1

National Semiconductor Japan Ltd.
Sumitomo Chemical
Engineering Center
Bldg. 7F
1-7-1, Nakase, Mihama-Ku
Chiba-City,
Chiba Prefecture 261
Tel: (043) 299-2300
Fax: (043) 299-2500

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semicondutores Do Brazil Ltda.
Rue Deputado Lacerda Franco
120-3A
Sao Paulo-SP
Brazil 05418-000
Tel: (55-11) 212-5066
Telex: 391-1131931 NSBR BR
Fax: (55-11) 212-1181

National Semiconductor (Australia) Pty. Ltd.
Building 16
Business Park Drive
Monash Business Park
Nottingham, Melbourne
Victoria 3168 Australia
Tel: (3) 558-9999
Fax: (3) 558-9998

National does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and National reserves the right at any time without notice to change said circuitry and specifications.