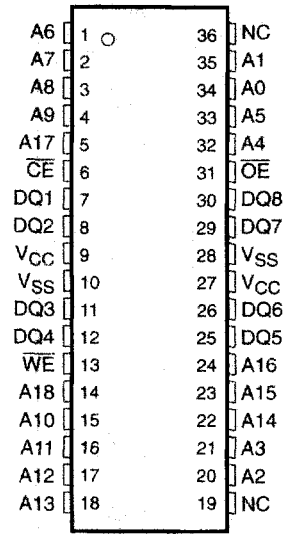
- **Single 5-V ± 10% Power Supply**
- **Fast Access Time 20/25/35 ns**
- **Equal Address and Chip-Enable Access Time**
- **All Inputs and Outputs Are TTL-Compatible**
- **3-State Outputs**
- **Power Operation: 220/210/200 mA Maximum, Active AC**
- **Low-Power Standby**
- **Ceramic Package Options:**
  - **36-Pin, 400-mil CSOJ (HJA Suffix)**
  - **36-Pin, 500 mil Flatpack (HKE Suffix)**
- **Operating Free-Air Temperature Range –55°C to 125°C**

HJA/HKE PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0–A18	Address Inputs
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
$\overline{CE}$	Chip Enable
DQ1–DQ8	Data Input/Output
NC	No Connection
V_{CC}	5-V Power Supply
V_{SS}	Ground

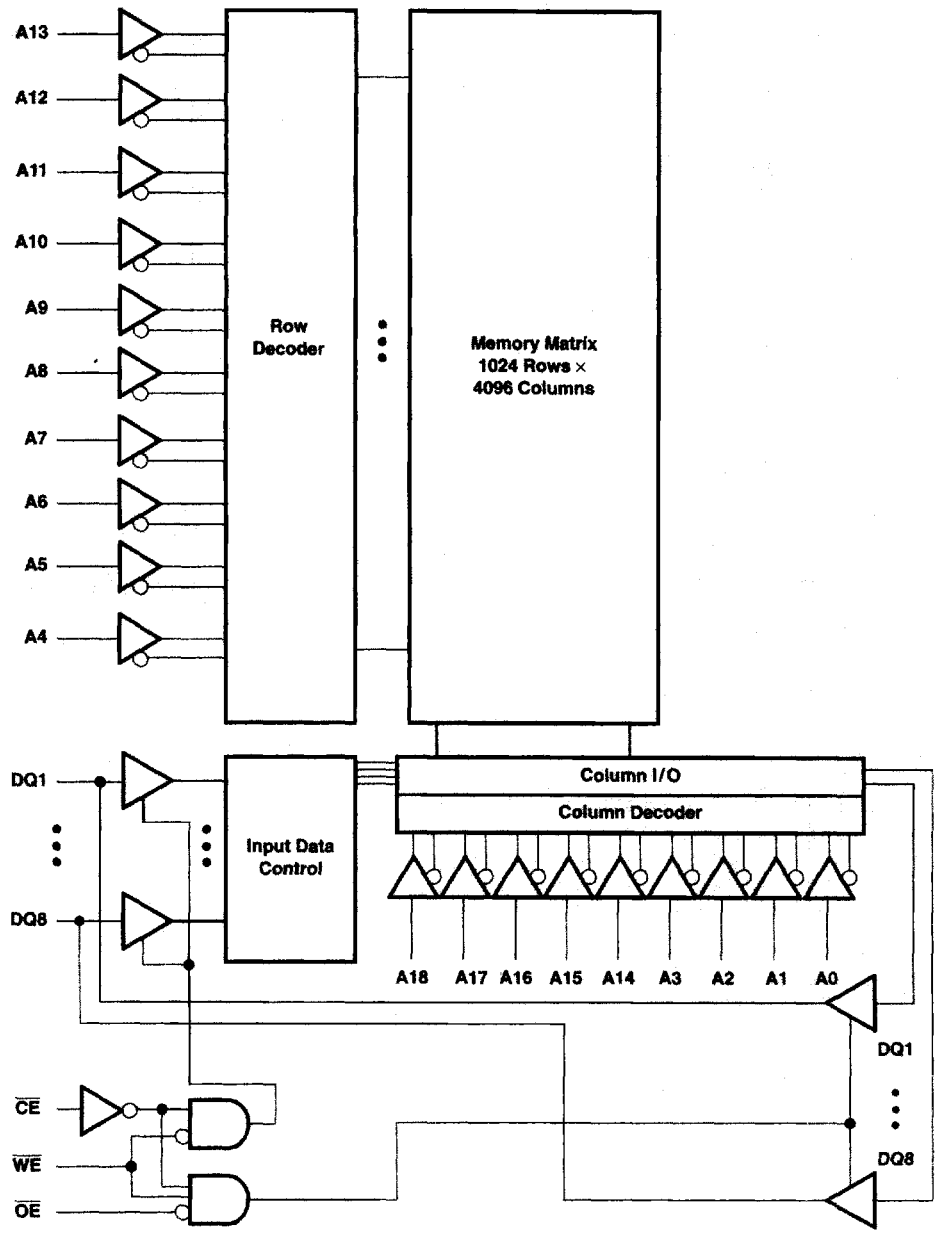
description

The SMJ684002 is a 4194304-bit static random-access memory (SRAM), organized as 524288-words of 8-bits. The SMJ684002 is fabricated using high-performance silicon-gate CMOS technology. Static design eliminates the need for external clocks or timing strobes while CMOS circuitry reduces power consumption and provides for greater reliability.

The SMJ684002 is equipped with chip-enable ($\overline{CE}$) and output-enable ($\overline{OE}$) pins, allowing for greater system flexibility and eliminating bus-contention problems. When either input (output-enable or chip-enable) is high, it forces the outputs into the high-impedance state. The SMJ684002 is available in a 500-mil, 36-lead, surface-mount package (HKE suffix) and a 400-mil, 36-lead, flatpack (HJA suffix).

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high-impedance circuits.

functional block diagram



operation

address (A0–A18)

Nineteen address lines allow access to each of the 512K 8-bit words in RAM.

data inputs/data outputs (DQ1–DQ8)

Data can be written into the device when $\overline{CE}$ and $\overline{WE}$ are low. DQ1–DQ8 are TTL compatible. The device is placed in a low-power standby mode with the DQs in the high-impedance state when a logic high is on $\overline{CE}$. The device remains active with high-impedance DQs when $\overline{OE}$ and $\overline{WE}$ are high, and when $\overline{CE}$ is low.

chip enable ($\overline{CE}$)

Whenever $\overline{CE}$ is low, the device is active. Standby mode is reached when $\overline{CE}$ is high. Data is retained during standby.

write enable ($\overline{WE}$)

The read or write mode is selected through the use of $\overline{WE}$. $\overline{WE}$ must be high for the read mode and low for the write mode. $\overline{WE}$ must be high when address changes occur to prevent writing data erroneously into new memory locations. $\overline{WE}$ is irrelevant when the device is in standby mode.

output enable ($\overline{OE}$)

When in the read mode, $\overline{OE}$ controls the state of the DQs. A high on $\overline{OE}$ places the DQs in the high-impedance state, while a low provides data on the outputs.

truth table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	MODE	I/O PIN	CYCLE	CURRENT
H	X	X	Not selected	Hi-Z	—	I_{SB1}–I_{SB2}
L	H	H	Output disabled	Hi-Z	—	I_{CCA}
L	L	H	Read	D_{OUT}	Read	I_{CCA}
L	X	L	Write	Hi-Z	Write	I_{CCA}

X = don't care

absolute maximum ratings over operating free air temperature†

Supply voltage range, V_{CC} ..... –0.5 V to 7 V
Voltage relative to V_{SS} for any pin except V_{CC} ..... – 0.5 to V_{CC} + 0.5 V
Output current per I/O ..... ± 20 mA
Power dissipation ..... 1 W
Operating free-air temperature range, T_A ..... – 55°C to 125°C
Storage temperature range, T_{stg} ..... – 65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage (see Note 1)	2.2		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage (see Note 2)	– 0.5		0.8	V
T_A	Operating free-air temperature	– 55		125	°C

NOTES: 1. V_{IH}(MAX) = V_{CC} + 0.3-V dc; V_{IH}(MAX) = V_{CC} + 2-V ac (pulse width ≤ 2 ns).
2. V_{IL}(MIN) = – 0.5-V dc; V_{IL}(MIN) = – 2-V ac (pulse width ≤ 2 ns).

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS‡	'684002-20		'684002-25		'684002-35		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	V_{CC} = 4.5 V, I_{OH} = – 4 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5 V, I_{OL} = 8 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	All inputs, V_{IN} = 0 to V_{CC}	– 1	1	– 1	1	– 1	1	µA
I_O	Output current (leakage)	$\overline{CE}$ = V_{IH}, V_{OUT} = 0 to V_{CC}	– 1	1	– 1	1	– 1	1	µA
I_{CC}	AC active supply current	V_{CC} = 5.5 V, I_O = 0 mA f = MAX = $1/t_{C(R)}$		220		210		200	mA
I_{SB1}	AC standby current	V_{CC} = 5.5 V, $\overline{CE}$ ≥ V_{IH}(MAX) No other restrictions on other inputs f = MAX = $1/t_{C(R)}$		60		50		40	mA
I_{SB2}	CMOS standby current	$\overline{CE}$ ≥ V_{CC} – 0.2 V, V_{IH} ≤ V_{SS} + 0.2 V, or ≥ V_{CC} – 0.2 V V_{CC}= 5.5 V, f = 0 MHz		15		15		15	

‡ For conditions shown as MIN/MAX, use the appropriate value specified in the recommended operating conditions table.

capacitance over recommended ranges of supply voltage,§ f = 1 MHz, V_{OUT} = 0 V, V_{IN} = 0 V, T_A = 25°C

PARAMETER			MIN	MAX	UNIT
C_i	Input capacitance	All inputs except clocks and DQs		10	pF
		$\overline{CE}$, $\overline{OE}$, $\overline{WE}$		12	
$C_{i/o}$	Input/output capacitance	DQ1–DQ8		14	pF

§ Capacitance measurements are made on sample basis only.

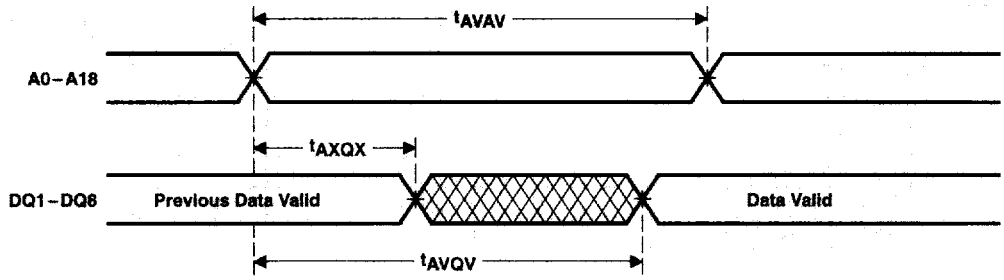
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

read cycle timing (see Note 3)

		JEDEC SYMBOL	MCM6246-20		MCM6246-25		MCM6246-35		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(R)}$	Cycle time, read (see Notes 4 and 5)	t_{AVAV}	20		25		35		ns
$t_{a(A)}$	Access time, address	t_{AVQV}		20		25		35	ns
$t_{a(E)}$	Access time, enable (see Note 6)	t_{ELQV}		20		25		35	ns
$t_{a(G)}$	Access time, output enable	t_{OLQV}		6		8		10	ns
$t_{h(A)}$	Hold time, output from address change	t_{AXQX}	5		5		5		ns
$t_{en(E)}$	Enable low to output active (see Notes 7, 8, and 9)	t_{ELQX}	5		5		5		ns
$t_{en(G)}$	Enable time, output low to output active (see Notes 7, 8, and 9)	t_{OLQX}	0		0		0		ns
$t_{dis(E)}$	Disable time, output high to output high-impedance (see Notes 7, 8, and 9)	t_{EHQZ}	0	8	0	10	0	12	ns
$t_{dis(G)}$	Disable time, output high to output high-impedance (see Notes 7, 8, and 9)	t_{OHQZ}	0	8	0	10	0	12	ns

NOTES: 3. $\overline{WE}$ is high for read cycle.
4. Product sensitivities to noise require grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
5. All read-cycle timings are referenced from the last valid address to the first transitioning address.
6. Addresses are valid prior to or coincident with $\overline{CE}$ going low.
7. At any given voltage and temperature, $t_{EHQZ}MAX < t_{ELQX}MIN$, and $t_{OHQZ}MAX < t_{OLQX}MIN$, both for a given device and from device to device.
8. Transition is measured at ± 500 mV from steady-state voltage with load in Figure 1 (b).
9. This parameter is specified by design but not tested.

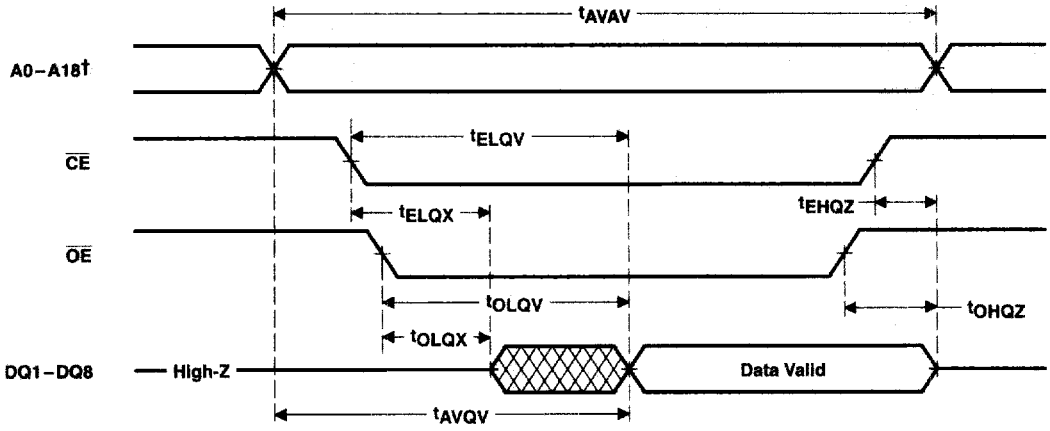
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)



NOTE: Chip-enable and output-enable are held in their active state. $\overline{WE}$ is high; therefore, it stays selected.

Figure 1. Read-Cycle Timing (Device Continuously Selected)

PARAMETER MEASUREMENT INFORMATION



† Addresses are valid prior to, or coincident with, $\overline{CE}$ going low or $\overline{CE}$ going high, $\overline{WE}$ is high.

Figure 2. Read-Cycle Timing (Enable Controlled)

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

write-cycle timing – $\overline{WE}$ controlled (see Notes 4, 10, and 11)

		JEDEC SYMBOL	'684002-20		'684002-25		'684002-35		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(W)}$	Cycle time, write (see Note 12)	t_{AVAV}	20		25		35		ns
$t_{su(A)}$	Setup time, address	t_{AVWL}	0		0		0		ns
$t_{su(AWH)}$	Setup time., address valid to end of write	t_{AVWH}	15		17		20		ns
$t_{w(W)}$	Pulse duration, write	t_{WLEH}	15		17		20		ns
$t_{w(D)}$	Pulse duration, data valid to end of write	t_{DVWH}	10		10		15		ns
$t_{h(D)}$	Hold time, data from end of write	t_{WHDX}	0		0		0		ns
$t_{dis(W)}$	Disable time, write low to data high-impedance (see Notes 8, 9, and 13)	t_{WLQZ}	0	8	0	10	0	15	ns
$t_{en(W)}$	Enable time, write high to output active (see Notes 8, 9, and 13)	t_{WHQX}	5		5		5		ns
$t_{h(A)}$	Hold time address, from end of write	t_{WHAX}	0		0		0		ns

NOTES: 4. Product sensitivities to noise require grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
8. Transition is measured ± 500 mV from steady-state voltage with load in Figure 1 (b).
9. This parameter is specified by design but not tested.
10. A write occurs during the overlap of $\overline{CE}$ low and $\overline{WE}$ low.
11. If $\overline{OE}$ goes low coincident with or after $\overline{WE}$ goes low, the output remains in the high-impedance state.
12. All write-cycle timings are referenced from the last valid address to the first transitioning address.
13. At any given voltage and temperature, $t_{WLQZ}MAX < t_{WHQX}MIN$ both for a given device and from device to device.

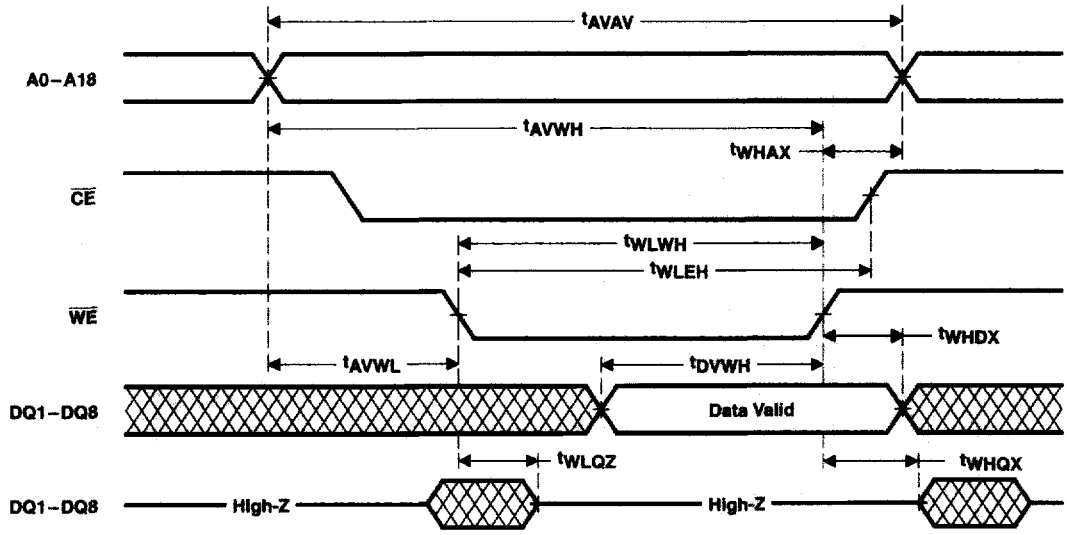


Figure 3. Write-Cycle Timing (Write Enable Controlled)

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

write-cycle timing – $\overline{CE}$ controlled (see Notes 4, 10, and 11)

		JEDEC SYMBOL	684002-20		684002-25		684002-35		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(W)}$	Cycle time, write (see Note 12)	t_{AVAV}	20		25		35		ns
$t_{su(A)}$	Setup time, address	t_{AVEL}	0		0		0		ns
$t_{w(AWH)}$	Pulse duration, address valid to end of write	t_{AVEH}	15		17		20		ns
$t_{w(E)}$	Pulse duration, enable (see Notes 14 and 15)	t_{ELEH}	15		17		20		ns
		t_{ELWH}	15		17		20		
$t_{w(W)}$	Pulse duration, write	t_{WLEH}	15		17		20		ns
$t_{su(D)}$	Setup time, data valid to end of write	t_{DVEH}	10		10		15		ns
$t_{h(D)}$	Hold time, data from end of write	t_{EHDX}	0		0		0		ns
$t_{h(A)}$	Hold time address from end of write	t_{EHAX}	0		0		0		ns

NOTES: 4. Product sensitivities to noise require grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
10. A write occurs during the overlap of $\overline{CE}$ low and $\overline{WE}$ low.
11. If $\overline{OE}$ goes low coincident with or after $\overline{WE}$ goes low, the output remains in a high-impedance state.
12. All write-cycle timings are referenced from the last valid address to the first transitioning address.
14. If $\overline{CE}$ goes high coincident with or before $\overline{WE}$ goes high, the output remains in a high-impedance state.
15. If $\overline{CE}$ goes low coincident with or after $\overline{WE}$ goes low, the output remains in a high-impedance state.

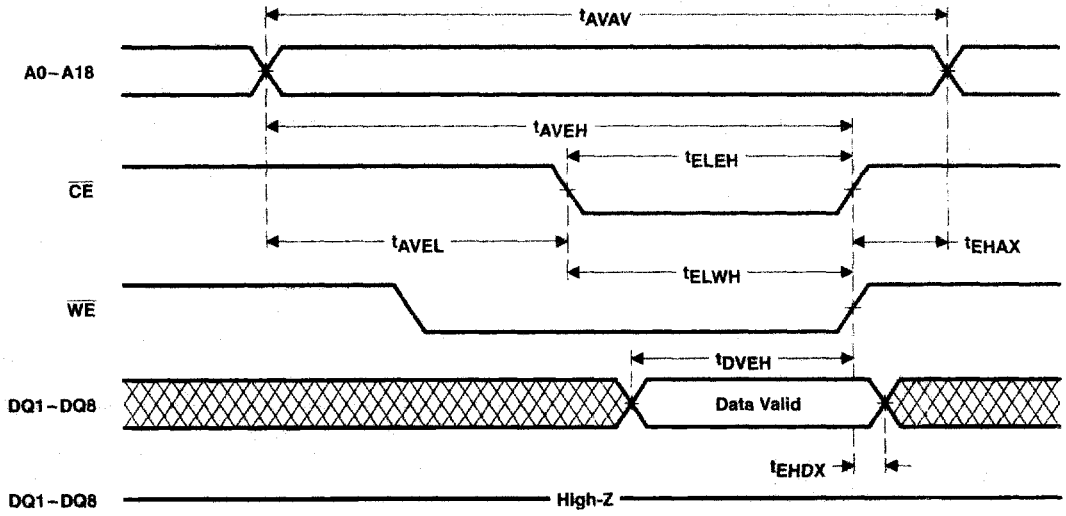
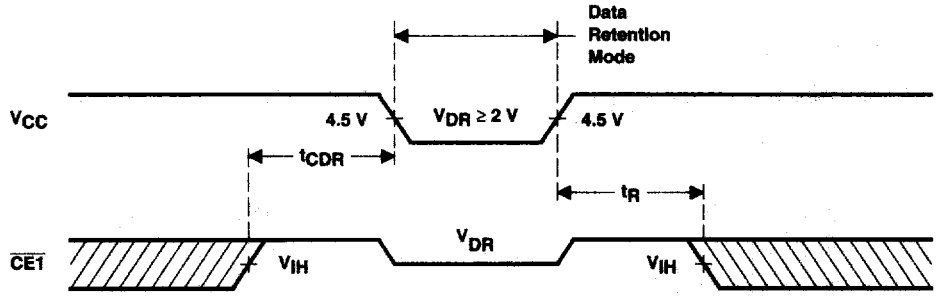


Figure 4. Write-Cycle Timing (Chip-Enable Controlled)

data-retention characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS	'5C1008-20		'5C1008-25		'5C1008-35		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{CC}	Data-retention voltage supply	V_{CC} = 2 V $\overline{CE} \geq V_{CC} - 0.2$ V $V_{IN} \geq V_{CC} - 0.2$ V or ≤ 0.2 V	2		2		2		V
$I_{CC\ DR}$	Data-retention current			2		2		2	mA
t_{CDR}	Retention time†		0		0		0		ns
t_R	Operation recovery time†		20		25		35		ns

† This parameter is tested initially and after any design or process change.

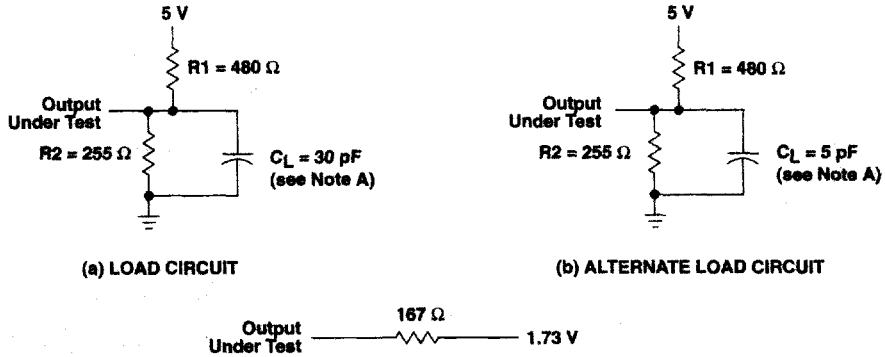


NOTE A: For t_R and t_{CDR}: $\overline{CE1} \geq V_{CC} - 0.2$ V or CE2 ≤ 0.2 V, $V_{IN} \geq V_{CC} - 0.2$ V or ≤ 0.2 V

Figure 5. Data-Retention Waveform

PARAMETER MEASUREMENT INFORMATION

PARAMETER	VALUE
Input pulse levels	0 V to 3 V
Input rise and fall times	2 ns
Input and output reference levels	1.5 V
Output load	See Figure 1



(a) LOAD CIRCUIT

(b) ALTERNATE LOAD CIRCUIT

(c) THEVENIN EQUIVALENT OF (a) OR (b)

NOTE A: C_L includes probe and fixture capacitances.

Figure 6. Output Load Circuits