Preliminary **Synchronous Communication SRAM**

Features

- 256K x 36 or 512K x 18 organization
- 3.3 V or 2.5 V Power Supply and I/O
- LVTTL Input and Output levels
- 100% bus utilization at high frequencies
- Optimized control logic for minimum control signal interface
- $\overline{CKE}$ to enable or suspend clock operations
- Three chip enable pins ($\overline{CE}$, $\overline{CE2}$, CE2) for depth expansion with double cycle deselect
- Single Read/Write control pin ($\overline{R/W}$)
- Individual Byte Write Controls
- Synchronous Pipeline Mode of Operation with fully coherent Self-Timed Late-Late-Write
- Registered control inputs, addresses and data I/O.
- Burst feature supports interleaved or linear burst orders
- SNOOZE Mode, for reduced stand-by power.
- 100 pin TQFP package

Description

The IBM0418/36A86L/SQKA 8Mb SRAMs are Synchronous Pipeline SRAMs using Late-Late-Write protocol and optimized I/O timing parameters to permit 100% bus utilization for any sequence of READ & WRITE operations.

The clock input (CLK) is used to register all synchronous input pins on its rising edge. Synchronous inputs include clock enable ($\overline{CKE}$), chip enable ($\overline{CE}$, CE2 and $\overline{CE2}$), cycle start input (ADV/$\overline{LD}$), all addresses (SA), read/write control ($\overline{R/W}$), byte write controls ($\overline{BWa}$, $\overline{BWb}$, $\overline{BWc}$, $\overline{BWd}$) and all data inputs (DQ).

Asynchronous inputs include output enable ($\overline{OE}$), which may be carefully timed to optimally reduce bus turn-around time, and snooze enable (ZZ). Static burst mode pin (MODE) selects between interleaved and linear burst modes, and should be tied HIGH (or left unconnected) for interleaved burst order (or if Burst Mode is not used), or tied LOW for linear burst order.

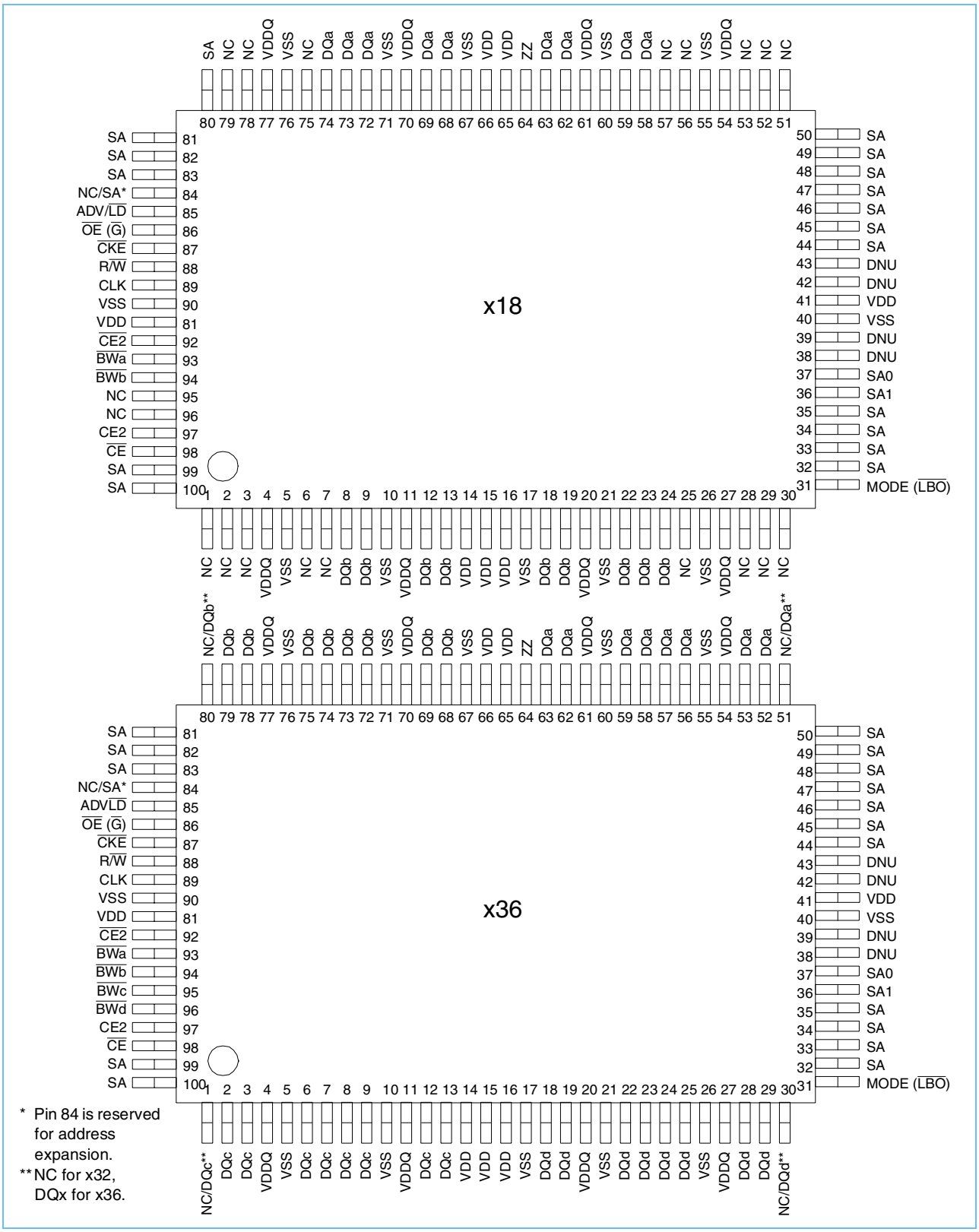
READ, WRITE and DESELECT cycles (see cycle truth table) are initiated with ADV/$\overline{LD}$ = LOW. Subsequent READ or WRITE operations can load new Addresses (ADV/$\overline{LD}$ = LOW), or use the internally generated burst address if ADV/$\overline{LD}$ = HI (see Burst Sequence Truth tables) based on the initial address that was loaded.

For WRITE operations, Byte Write inputs ($\overline{BWa}$, $\overline{BWb}$, $\overline{BWc}$, $\overline{BWd}$) are registered on each cycle the address is either loaded externally, or advanced from the internal burst counter, data is registered two (active) cycles later.

Snooze Mode is enabled by switching asynchronous signal ZZ High. When the SRAM is in Snooze mode, the outputs will go to a High-Z state, and the SRAM will draw a standby current of I_{SB2Z} after a delay of t_{ZZI}. SRAM data will be preserved during SNOOZE Mode, but any READ or WRITE operation that is pending while entering SNOOZE Mode is not guaranteed. A recovery time (t_{ZZR}) is required before the SRAM resumes normal operation.

The SRAM operates from a single 3.3 V or 2.5 V power supply, and supports LVTTL I/O levels.

Pinout (Top View)



Ordering Information (These are all possible sorts; some may not be qualified or others added)

Part Number	Organization	Function	V_{DD}/V_{DDQ} (Volts)	Cycle/Access (ns)
IBM0418A86LQKA-6	512K x 18	LVTTL Pipeline	2.5/2.5	6.0/3.5
IBM0418A86LQKA-7	512K x 18	LVTTL Pipeline	2.5/2.5	6.7/3.8
IBM0418A86LQKA-7F	512K x 18	LVTTL Pipeline	2.5/2.5	7.5/4.2
IBM0418A86LQKA-8F	512K x 18	LVTTL Pipeline	2.5/2.5	8.5/4.5
IBM0418A86LQKA-10	512K x 18	LVTTL Pipeline	2.5/2.5	10.0/5.0
IBM0418A86SQKA-6	512K x 18	LVTTL Pipeline	3.3/3.3	6.0/3.5
IBM0418A86SQKA-7	512K x 18	LVTTL Pipeline	3.3/3.3	6.7/3.8
IBM0418A86SQKA-7F	512K x 18	LVTTL Pipeline	3.3/3.3	7.5/4.2
IBM0418A86SQKA-8F	512K x 18	LVTTL Pipeline	3.3/3.3	8.5/4.5
IBM0418A86SQKA-10	512K x 18	LVTTL Pipeline	3.3/3.3	10.0/5.0
IBM0436A86LQKA-6	256K x 36	LVTTL Pipeline	2.5/2.5	6.0/3.5
IBM0436A86LQKA-7	256K x 36	LVTTL Pipeline	2.5/2.5	6.7/3.8
IBM0436A86LQKA-7F	256K x 36	LVTTL Pipeline	2.5/2.5	7.5/4.2
IBM0436A86LQKA-8F	256K x 36	LVTTL Pipeline	2.5/2.5	8.5/4.5
IBM0436A86LQKA-10	256K x 36	LVTTL Pipeline	2.5/2.5	10.0/5.0
IBM0436A86SQKA-6	256K x 36	LVTTL Pipeline	3.3/3.3	6.0/3.5
IBM0436A86SQKA-7	256K x 36	LVTTL Pipeline	3.3/3.3	6.7/3.8
IBM0436A86SQKA-7F	256K x 36	LVTTL Pipeline	3.3/3.3	7.5/4.2
IBM0436A86SQKA-8F	256K x 36	LVTTL Pipeline	3.3/3.3	8.5/4.5
IBM0436A86SQKA-10	256K x 36	LVTTL Pipeline	3.3/3.3	10.0/5.0

Pin Descriptions

Symbol	Type	Description
CLK	Input	**Clock:** This signal registers the address, data, chip enables, byte write enables and burst control inputs on its rising edge. All synchronous inputs must meet setup and hold times around clock's rising edge.
CKE	Input	**Synchronous Clock Enable:** This active LOW input enables the CLK input. When HIGH, the CLK input is ignored, and the previous cycle is extended.
CE CE2	Input	**Synchronous Chip enable:** These active LOW inputs are used to enable the device and is sampled only when a new external address is loaded (ADV/$\overline{LD}$ LOW). Double cycle deselect protocol.
CE2	Input	**Synchronous Chip enable:** This active HIGH input is used to enable the device and is sampled only when a new external address is loaded (ADV/$\overline{LD}$ LOW). Double cycle deselect protocol.
ADV/$\overline{LD}$	Input	**Synchronous Address Advance/Load:** When LOW, a new address is loaded into the device (and Burst counter). When HIGH, the internal burst counter is advanced and used (R/$\overline{W}$ is ignored).
SA0 SA1 SA	Input	**Synchronous Address Inputs.** SA0 and SA1 are the least significant Address bits, and are used to set the Burst Address counter for Burst operations. Pin 84 is reserved as the High order Address for the 16Mb Late-Late-Write SRAM.
BWa BWb BWc BWd	Input	**Synchronous Byte Writes:** These inputs allow individual bytes to be written (LOW), or masked (HIGH) during a WRITE operation. BYTE WRITEs are registered on the same clock edge as the WRITE Address (whether it is an externally provided or internally generated Address). These inputs have no affect during a READ operation.
R/W	Input	**Read/Write:** This synchronous input, sampled at the rising edge of CLK when ADV/$\overline{LD}$ is low, determines whether a READ (HIGH) or WRITE (LOW) operation is initiated. For WRITE operations, the Byte Write Enable inputs provide Byte control for partial WRITE operations.
OE	Input	**Output Enable:** This active LOW, asynchronous input enables the Output Drivers.
MODE($\overline{LBO}$)	Input	**Mode:** A LOW on this pin selects Linear Burst order. A HIGH or NC will default Interleaved Burst order. Do not change input state once device is operating.
DQa DQb DQc DQd	Input/Output	**Data I/Os:** DQa is Data Input and Output for Byte "a". DQb is for Byte "b",DQc is for Byte "c" and DQd is for Byte "d".
ZZ	Input	**Snooze Enable:** This active HIGH, asynchronous input causes the chip to enter Snooze Mode, which is a low standby-current state. While ZZ is HIGH, all other inputs are ignored, and data in the memory array is retained. Pin may be left unconnected.
NC	NC	**No Connect:** These pins can be left unconnected, or may be connected to GND to minimize thermal impedance or any other DC input.
VDD	Supply	**Power Supply:** See DC Electrical Characteristics and Recommended DC Operating Conditions for range.
VDDQ	Supply	**Isolated Output Buffer Supply**: See DC Electrical Characteristics and Recommended DC Operating Conditions for range.
VSS	Supply	**Ground:** GND.
DNU	NC/Input	**Do Not Use.** Reserved pins. These can either be left unconnected or wired to GND to improve thermal impedance

SRAM Features

Late-Late-Write

In Late-Late-Write function, WRITE data must be registered on the N+2 clock cycle and addresses and controls registered on the N base clock cycle. READ data is available in the N+1 clock cycle. READ data is valid a full cycle plus access time from the time the address is registered. WRITE data must be provided with set-up time 2 cycles after the valid address. This provides 100% bus utilization. In the unique case when a read cycle occurs after a write cycle to the same address, WRITE data information is stored temporarily in holding registers. During the first write cycle preceded by a read cycle, the SRAM array will be updated with the address and data from the holding registers. Read cycle addresses are monitored to determine if read data is supplied from the SRAM array or the write buffer holding registers. By-passing the SRAM array occurs on a byte-by-byte basis. When only one byte is written during a write cycle, read data from the address last written will have new byte data from the write buffer and the remaining bytes from the SRAM array. Late-Late-Write is extremely similar to Late-Write; just one additional cycle is needed to register the write data.

Burst Mode

The IBM0418/36A86 SRAM can operate in either linear or interleave burst modes using LBO pin. Addresses are loaded via the ADV/LD pin. Once an address is loaded, it is designated as either a write or read address from the initial address load. All burst addresses produced by ADV pulses are either read or write as designated by the initial address. Only read OR write operation within a burst loaded address is supported.

Power Down Mode

Power Down Mode, or “Sleep Mode,” is accomplished by switching asynchronous signal ZZ high. When powering-down the SRAM inputs must be dropped first and VDDQ must be dropped before or simultaneously with V_{DD}.

Power-Up Requirements

In order to guarantee the optimum internally regulated supply voltage, the SRAM requires 50 μs of power-up time after V_{DD} reaches its operating range. SRAM power-up requires V_{DD} to be powered before or simultaneously with V_{DDQ} and inputs after V_{DDQ}. V_{DDQ} should not exceed V_{DD} supply by more than 0.4V during power-up.

Sleep Mode Operation

Sleep mode is a low power mode initiated by bringing the asynchronous ZZ pin HIGH. During sleep mode, all other inputs are ignored and outputs are brought to a High-Z state. Sleep mode current and output High Z are guaranteed after the specified sleep mode enable time. During sleep mode, the array data contents are preserved. Sleep mode must not be initiated until after all pending operations have completed, as any pending operation is not guaranteed to properly complete after sleep mode is initiated. Sense amp data is lost. Normal operation can be resumed by bringing ZZ low, but only after specified sleep mode recovery time.

Cycle Definition Truth Table (see notes 1, 2, 3, 4)

Operation	Address used	CE	CE2	CE2	ZZ	ADV/ LD	R/$\overline{W}$	BWx	OE	CKE	CLK	DQ	Notes
Deselect Cycle	None	H	X	X	L	L	X	X	X	L	L→H	High-Z	
Deselect Cycle	None	X	H	X	L	L	X	X	X	L	L→H	High-Z	
Deselect Cycle	None	X	X	L	L	L	X	X	X	L	L→H	High-Z	
Deselect Cycle (Continue)	None	X	X	X	L	H	X	X	X	L	L→H	High-Z	5
READ Cycle (Begin Burst)	External	L	L	H	L	L	H	X	L	L	L→H	Q	
READ Cycle (Continue Burst)	Next	X	X	X	L	H	X	X	L	L	L→H	Q	5, 6
No Op /Dummy READ (Begin Burst)	External	L	L	H	L	L	H	X	H	L	L→H	High-Z	7
Dummy READ (Continue Burst)	Next	X	X	X	L	H	X	X	H	L	L→H	High-Z	5, 6, 7
WRITE Cycle (Begin Burst)	External	L	L	H	L	L	L	L	X	L	L→H	D	8
WRITE Cycle (Continue Burst)	Next	X	X	X	L	H	X	L	X	L	L→H	D	5, 6, 8
No Op /WRITE Abort (Begin Burst)	None	L	L	H	L	L	L	H	X	L	L→H	High-Z	7, 8
WRITE Abort (Continue Burst)	Next	X	X	X	L	H	X	H	X	L	L→H	High-Z	5, 6, 7, 8
Clock Disabled (Stall)	Current	X	X	X	L	X	X	X	X	H	L→H	Held	9
SNOOZE Mode	None	X	X	X	H	X	X	X	X	X	X	High-Z	

1. X="Don't care", H=Logic "High", L= Logic "Low". $\overline{BWx}$=H means all byte write inputs ($\overline{BWa}$, $\overline{BWb}$, $\overline{BWc}$, $\overline{BWd}$) are "High". $\overline{BWx}$=L means one or more byte write signals are "Low". (see truth table for READ/WRITE commands for more info on byte enable control).
2. All inputs except $\overline{OE}$ and ZZ must meet setup and hold times around the rising edge of CLK
3. $\overline{CKE}$ held "High" will insert wait states. Internal device registers will hold their previous values.
4. On-chip circuitry is included to ensure that outputs are held in High-Z during power-up.
5. Continue BURST Cycles are initiated with the ADV/$\overline{LD}$ pin held high. The type of cycle that is performed (DESELECT, READ or WRITE) is determined by the initial DESELECT or Begin READ/WRITE burst cycle.
6. The address counter is incremented for all CONTINUE BURST cycles (see Burst Sequence truth table for Burst order and wrap information).
7. DUMMY READ and WRITE ABORT cycles can be considered Non-Operations or "No Ops". All $\overline{BWx}$ inputs must be High to prevent a WRITE operation from being performed.
8. $\overline{OE}$ may be tied LOW to reduce the number of control pins for the SRAM. The device will automatically tri-state the output drivers during a WRITE cycle. By carefully controlling the $\overline{OE}$ timings, cycle time improvements can be obtained.
9. If a Clock Disable ($\overline{CKE}$ = High) command is issued during a READ operation, the DQ bus will remain active (Low-Z). If it occurs during a WRITE operation, the bus will remain inactive (High-Z), and any pending DATA-IN is delayed by an additional cycle. No operation will be performed during the Clock Disable cycle.

Interleaved Burst Sequence Truth Table (MODE=HI or NC)

First Address (External)	Second Address (Internal)	Third Address (Internal)	Fourth Address (Internal)
X...X00	X...X01	X...X10	X...X11
X...X01	X...X00	X...X11	X...X10
X...X10	X...X11	X...X00	X...X01
X...X11	X...X10	X...X01	X...X00

Linear Burst Sequence Truth Table (MODE=LOW)

First Address (External)	Second Address (Internal)	Third Address (Internal)	Fourth Address (Internal)
X...X00	X...X01	X...X10	X...X11
X...X01	X...X10	X...X11	X...X00
X...X10	X...X11	X...X00	X...X01
X...X11	X...X00	X...X01	X...X10

Read/Write Command Truth Table

FUNCTION	R/$\overline{W}$	BWa	BWb	BWc	BWd
READ	H	X	X	X	X
Abort Write (No Operation)	L	H	H	H	H
WRITE Byte “a”	L	L	H	H	H
WRITE Byte “b”	L	H	L	H	H
WRITE Byte “c”	L	H	H	L	H
WRITE Byte “d”	L	H	H	H	L

1. Any combination of $\overline{BWx}$ inputs may be used during WRITE operations to perform partial Byte Writes.
2. Shaded area of table does not apply to the x18 part, as only $\overline{BWa}$ and $\overline{BWb}$ are provided.

Absolute Maximum Ratings

Item	Symbol	Rating	Units	Notes
Power Supply Voltage	V_{DD}	-0.5 to 4.3	V	1
Output Power Supply Voltage	V_{DDQ}	-0.5 to V_{DD}	V	1
Input Voltage	V_{IN}	-0.5 to V_{DD} +0.5	V	1, 2
DQ Input Voltage	V_{DQIN}	-0.5 to V_{DDQ}+0.5	V	1
Junction Temperature	T_J	150	°C	1
Operating Temperature	T_A	0 to 70	°C	1
Storage Temperature	T_{STG}	-55 to +150	°C	1
Short Circuit Output Current	I_{OUT}	25	mA	1

1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Excludes DQ inputs.

Recommended DC Operating Conditions (T_A=0 to +70 °C)

Parameter	Symbol		Min.	Typ.	Max.	Units	Notes
Supply Voltage	V_{DD}	2.5V	2.25	2.5	2.75	V	1
		3.3V	3.0	3.3	3.63		
Output Driver Supply Voltage	V_{DDQ}	2.5V	2.25	2.5	V_{DD}	V	1
		3.3V	3.135	3.3	V_{DD}		
Input High Voltage	V_{IH}	2.5V	1.7	—	V_{DDQ} + 0.3	V	1, 2
		3.3V	2.0	—	V_{DDQ} + 0.3		
Input Low Voltage	V_{IL}		-0.3	—	0.8	V	1, 3
Input Leakage Current	IL_I		-2.0		2.0	µA	5
Output High Voltage (I_{OH}=-4.0mA)	V_{OH}	2.5V	2.0			V	1, 4
		3.3V	2.4				
Output Low Voltage (I_{OL}=8.0mA)	V_{OL}	2.5V	—		0.2	V	1, 4
		3.3V	—		0.4		
Output Leakage Current	IL_O		-4.0		4.0	µA	

1. All voltages referenced to V_{SS}. All V_{DD}, V_{DDQ} and V_{SS} pins must be connected.
2. V_{IH}(Max)DC = V_{DDQ} + 0.3 V, V_{IH}(Max)AC = V_{DDQ} + 0.85 V (pulse width ≤ 4.0ns).
3. V_{IL}(Min)DC = - 0.3 V, V_{IL}(Min)AC= -1.5 V (pulse width ≤ 4.0ns)
4. Driver AC characteristics are higher than the shown DC values. See AC Test Loading figure for actual test conditions.
5. MODE pin has an internal pull-up, and IL_I = +/-100µA.

DC Electrical Characteristics (T_A=0 to +70 °C, V_{DD}=3.3 ± 10% or 2.5V ± 10%V)

Parameter	Symbol	Max.					Units	Notes
		-6	-7	-7F	-8F	-10		
Average Power Supply Current - Operating Device Selected; V_{IL} ≥ all inputs ≥ V_{IH}; Cycle time ≥ t_{KHKH} (min); V_{DD}=max.; Outputs open	I_{DD}	450	400	350	300	250	mA	1, 2
Average Power Supply Current - Idle Device Selected; V_{SS} + 0.2 ≥ all inputs ≥ V_{DD} - 0.2; CKE ≥ V_{DD} - 0.2; Cycle time ≥ t_{KHKH} (min); V_{DD}=max	I_{DD1}	20	18	15	12	10	mA	1, 2
CMOS Standby Current Device De-selected; V_{SS} + 0.2 ≥ all inputs ≥ V_{DD} - 0.2; All inputs static; Clocks idle; V_{DD}=max	I_{SB2}	10	10	10	10	10	mA	2
TTL Standby Current Device De-selected; V_{IL} ≥ all inputs ≥ V_{IH}; All inputs static; Clock frequency = 0; V_{DD}=max	I_{SB3}	25	25	25	25	25	mA	2
Clock Running Current Device Selected; V_{SS} + 0.2 ≥ all inputs ≥ V_{DD} - 0.2; Cycle time ≥ t_{KHKH} (min); V_{DD}=max	I_{SB4}	95	85	75	65	60	mA	2
SNOOZE Mode Current ZZ ≥ $V_{IH;}$ V_{DD}=max	I_{SB2Z}	10	10	10	10	10	mA	

1. I_{DD} does not include I_{DDQ} (output driver supply) current. Current increases with faster cycle times. I_{DDQ} is a function of Clock Frequency and output load.
2. See Cycle Definition Truth Table for complete definition of “Selected” and “Deselected” cycles.

TQFP Thermal Characteristics

Item	Symbol	Rating	Units
Thermal Resistance Junction to Ambient	RΘJA	32	°C/W
Thermal Resistance Junction to Case	RΘJC	4	°C/W

Capacitance (T_A=0 to +70 °C, V_{DD}=3.3 ± 10%V, f=1MHz)

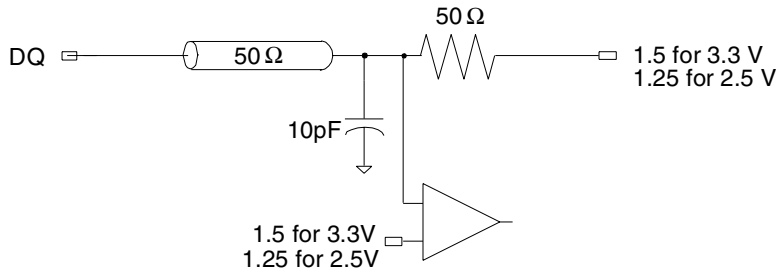
Parameter	Symbol	Test Condition	Max	Units	Notes
Control and Address Input Capacitance	C_{IN}	V_{IN} = 0V	4	pF	1
Data I/O Capacitance (DQ0-DQ35)	C_{OUT}	V_{OUT} = 0V	5	pF	1

1. Capacitance Values are sampled.

AC Test Conditions (T_A=0 to +70 °C, V_{DD} &V_{DDQ}=3.3 ± 10% V, See AC Test Loading figure below.)

Parameter	Symbol	V_{DD}/V_{DDQ}± 10%	Conditions	Units	Notes
Output Driver Supply Voltage	V_{DDQ}	2.5V	2.5	V	
		3.3V	1.8		
Input High Level	V_{IH}	2.5V	2.0	V	
		3.3V	1.5		
Input Low Level	V_{IL}		VSS	V	
Input Timing Reference Voltage		2.5V	1.25	V	
		3.3V	1.5		
Output Reference Voltage	V_{REF}	2.5V	1.25	V	
		3.3V	0.90		
Input Rise Time	T_R		0.5	ns	
Input Fall Time	T_F		0.5	ns	

AC Test Loading

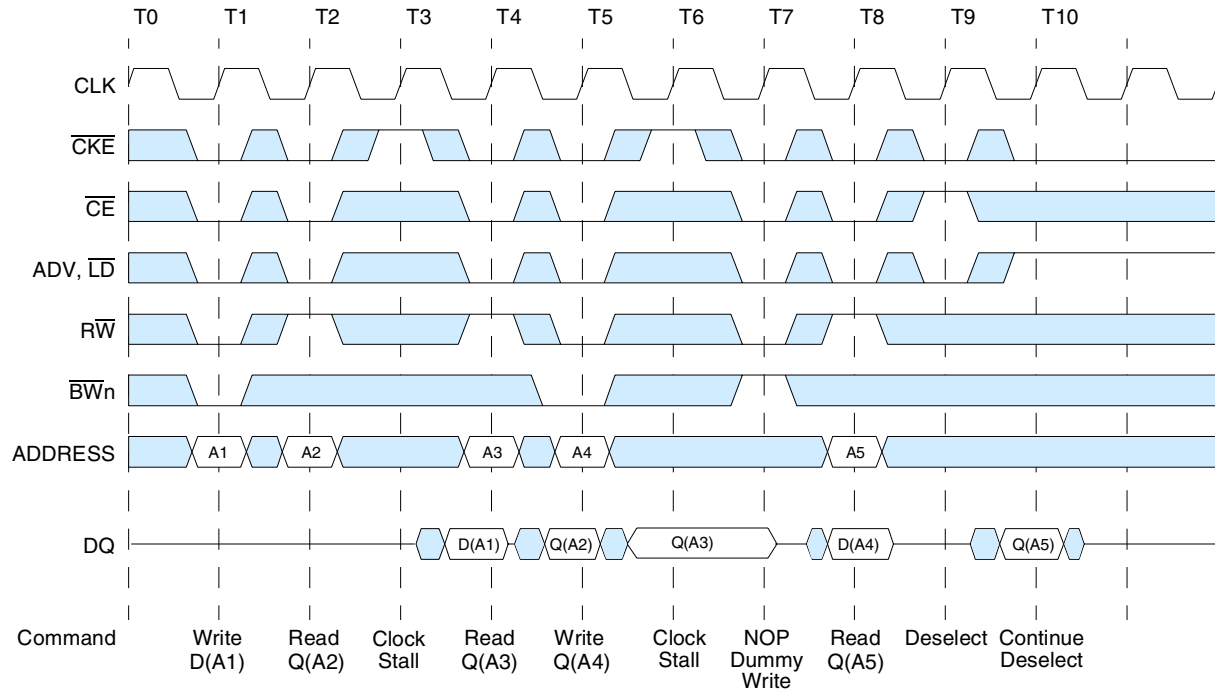


AC Characteristics (T_A=0 to +70 °C, V_{DD} &V_{DDQ} = 2.5 or 3.3V)

Parameter		Symbol	-6		-7		-7F		-8F		-10		Units	Notes
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Clock	Cycle Time	t_{KHKH}	6.0	—	6.7	—	7.5	—	8.5	—	10	—	ns	
	Clock High Pulse Width	t_{KHKL}	2.0	—	2.2	—	2.5	—	2.5	—	3.0	—	ns	
	Clock Low Pulse Width	t_{KLKH}	2.0	—	2.2	—	2.5	—	2.5	—	3.0	—	ns	
	Clock Enable Set-up time	t_{EVKH}	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns	
	Clock Enable Hold time	t_{KHEX}	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	ns	
Output Times	Clock to Output Valid	t_{KHQV}	—	3.5	—	3.8	—	4.2	—	4.5	—	5.0	ns	1
	Clock to Output Invalid	t_{KHQX}	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns	1
	Clock High to Output Low-Z	t_{KHQX1}	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns	1, 2
	Clock High to Output High-Z	t_{KHQZ}	1.5	3.0	1.5	3.0	1.5	3.5	1.5	3.5	1.5	3.5	ns	1, 2
	Output Enable to Output Valid	t_{GLQV}	—	3.5	—	4.0	—	4.2	—	4.5	—	5.0	ns	1
	Output Enable to Low-Z	t_{GLQX}	0.0	—	0.0	—	0.0	—	0.0	—	0.0	—	ns	1, 2
	Output Enable to High-Z	t_{GHQZ}	—	3.0	—	3.0	—	3.5	—	4.0	—	4.0	ns	1, 2
Setup Times	Address Setup Time	t_{AVKH}	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns	
	Sync Select Setup Time	t_{CVKH}	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns	
	Write Enables Setup Time	t_{WVKH}	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns	
	Data In Setup Time	t_{DVKH}	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns	
Hold Times	Address Hold Time	t_{KHAX}	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	ns	
	Sync Select Hold Time	t_{KHCX}	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	ns	
	Write Enables Hold Time	t_{KHWX}	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	ns	
	Data In Hold Time	t_{KHDX}	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	ns	
Snooze Mode	ZZ active to input ignored	t_{ZZ}	0.0	2(t_{KHKH})	0.0	2(t_{KHKH})	0.0	2(t_{KHKH})	0.0	2(t_{KHKH})	0.0	2(t_{KHKH})	ns	
	ZZ inactive to input sampled	t_{RZZ}	0.0	2(t_{KHKH})	0.0	2(t_{KHKH})	0.0	2(t_{KHKH})	0.0	2(t_{KHKH})	0.0	2(t_{KHKH})	ns	
	ZZ active to snooze current	t	0.0	2(t_{KHKH})	0.0	2(t_{KHKH})	0.0	2(t_{KHKH})	0.0	2(t_{KHKH})	0.0	2(t_{KHKH})	ns	
	ZZ inactive to exit snooze current	t_{RZZI}	0.0	—	0.0	—	0.0	—	0.0	—	0.0	—	ns	

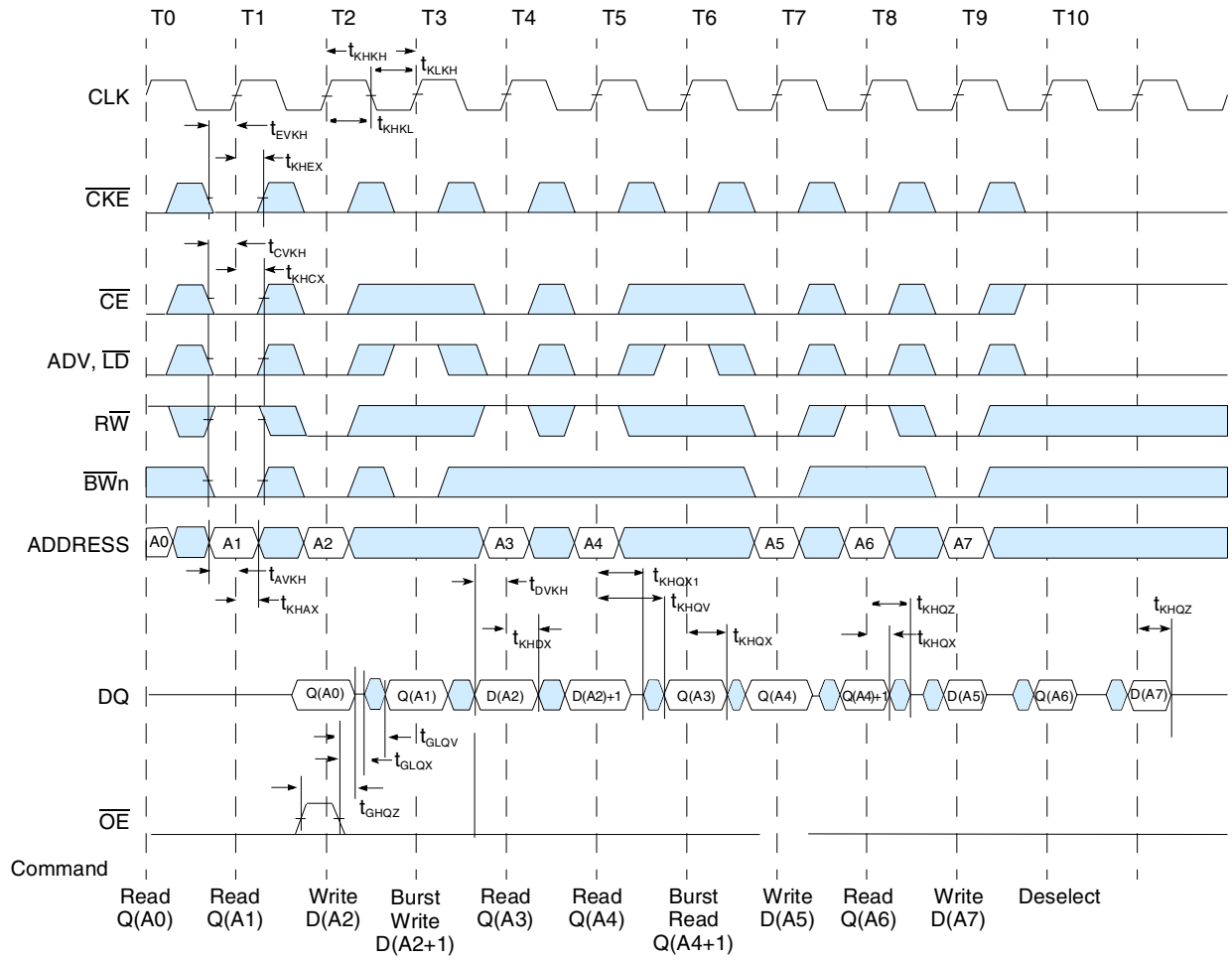
1. See AC Test Loading figure on page 10.
2. This parameter is sampled. Transition is measured ± 200mV from steady-state.

Timing Diagram (NOP, Stall, and Deselect Cycles)



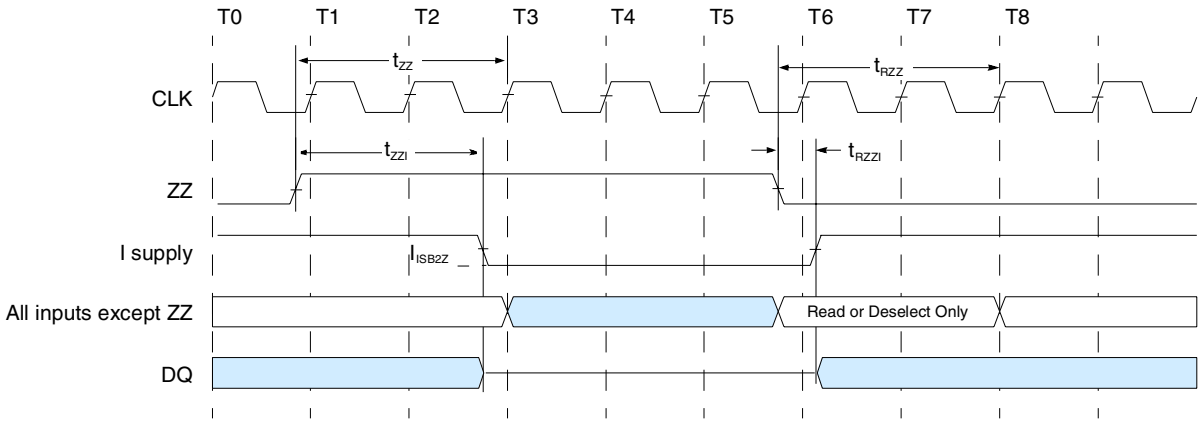
Q(A3) data extended from $\overline{CKE}$ High

Timing Diagram (Read Write Cycles)



Q(A1) data is gated by asynchronous $\overline{OE}$. Read data can always be gated by $\overline{OE}$; even burst generated addresses data.

Timing Diagram (Sleep Mode)



Revision Log

Rev	Contents of Modification
8/26/99	Initial public release (00).
9/16/99	Corrected V_{DD}/V_{DDQ} column in Ordering Information table. Release document version 01.
9/27/99	Changed name of product to Synchronous Communication SRAM. Fixed notes on Cycle Definition Truth Table on page 6 Release document version 02.

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9/27/99