

# SN54LV4051A, SN74LV4051A 8-CHANNEL ANALOG MULTIPLEXERS/DEMULTIPLEXERS

SCLS428H – MAY 1999 – REVISED APRIL 2005

- 2-V to 5.5-V  $V_{CC}$  Operation
- Support Mixed-Mode Voltage Operation on All Ports
- High On-Off Output-Voltage Ratio
- Low Crosstalk Between Switches
- Individual Switch Controls
- Extremely Low Input Current
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

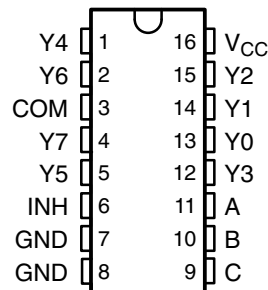
## description/ordering information

These 8-channel CMOS analog multiplexers/demultiplexers are designed for 2-V to 5.5-V  $V_{CC}$  operation.

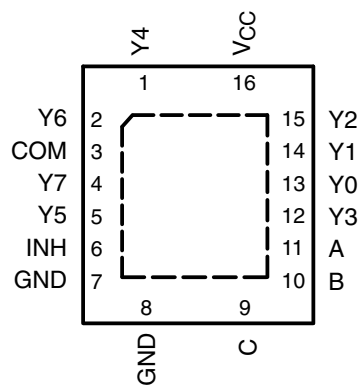
The 'LV4051A devices handle both analog and digital signals. Each channel permits signals with amplitudes up to 5.5 V (peak) to be transmitted in either direction.

Applications include signal gating, chopping, modulation or demodulation (modem), and signal multiplexing for analog-to-digital and digital-to-analog conversion systems.

SN54LV4051A . . . J OR W PACKAGE  
SN74LV4051A . . . D, DB, DGV, N, NS, OR PW PACKAGE  
(TOP VIEW)



SN74LV4051A . . . RGY PACKAGE  
(TOP VIEW)



## ORDERING INFORMATION

$T_A$	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING	
–40°C to 85°C	PDIP – N	Tube of 25	SN74LV4051AN	SN74LV4051AN	
	QFN – RGY	Reel of 1000	SN74LV4051ARGYR	LW051A	
	SOIC – D	Tube of 40	SN74LV4051AD	LV4051A	
		Reel of 2500	SN74LV4051ADR		
	SOP – NS	Reel of 2000	SN74LV4051ANSR	74LV4051A	
	SSOP – DB	Tube of 90	Reel of 2000	SN74LV4051ADBR	LW051A
			Reel of 2000	SN74LV4051APWR	
			Reel of 250	SN74LV4051APWT	
Reel of 2000			SN74LV4051ADGVR	LW051A	
–55°C to 125°C	CDIP – J	Tube of 25	SNJ54LV4051AJ	SNJ54LV4051AJ	
	CFP – W	Tube of 150	SNJ54LV4051AW	SNJ54LV4051AW	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

UNLESS OTHERWISE NOTED this document contains PRODUCTION DATA information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2005, Texas Instruments Incorporated

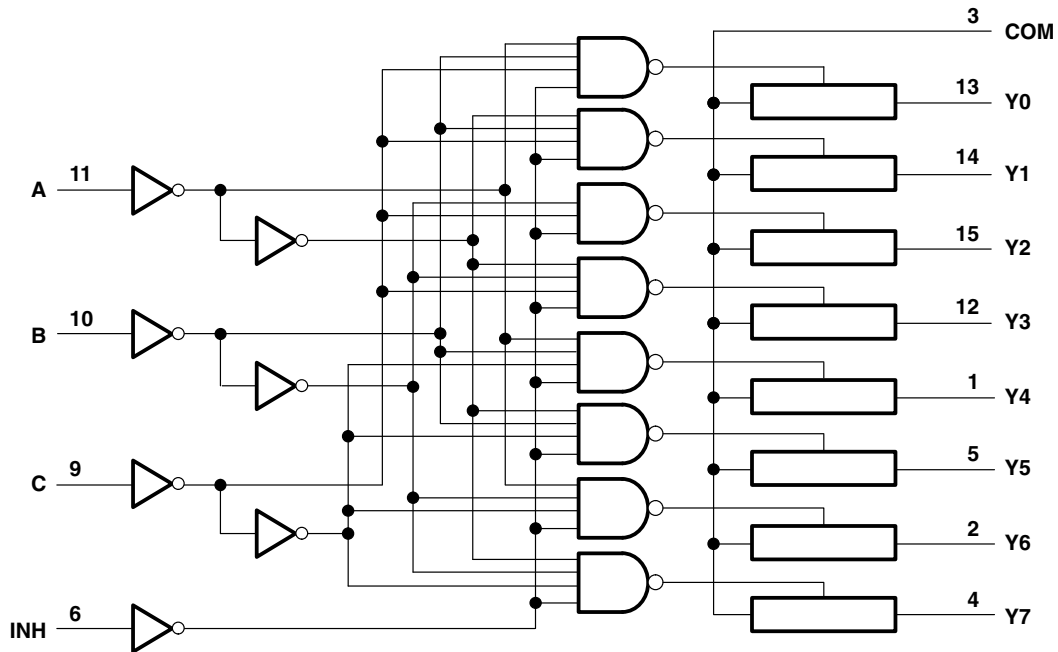
# SN54LV4051A, SN74LV4051A 8-CHANNEL ANALOG MULTIPLEXERS/DEMULTIPLEXERS

SCLS428H – MAY 1999 – REVISED APRIL 2005

FUNCTION TABLE

INPUTS				ON CHANNEL
INH	C	B	A	
L	L	L	L	Y0
L	L	L	H	Y1
L	L	H	L	Y2
L	L	H	H	Y3
L	H	L	L	Y4
L	H	L	H	Y5
L	H	H	L	Y6
L	H	H	H	Y7
H	X	X	X	None

logic diagram (positive logic)



# SN54LV4051A, SN74LV4051A 8-CHANNEL ANALOG MULTIPLEXERS/DEMULPLEXERS

SCLS428H – MAY 1999 – REVISED APRIL 2005

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$	–0.5 V to 7.0 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to 7.0 V
Switch I/O voltage range, $V_{IO}$ (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–20 mA
I/O diode current, $I_{IOK}$ ( $V_{IO} < 0$ )	–50 mA
Switch through current, $I_T$ ( $V_{IO} = 0$ to $V_{CC}$ )	±25 mA
Continuous current through $V_{CC}$ or GND	±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3): D package	73°C/W
(see Note 3): DB package	82°C/W
(see Note 3): DGV package	120°C/W
(see Note 3): N package	67°C/W
(see Note 3): NS package	64°C/W
(see Note 3): PW package	108°C/W
(see Note 4): RGY package	39°C/W
Storage temperature range, $T_{stg}$	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.  
 2. This value is limited to 5.5 V maximum.  
 3. The package thermal impedance is calculated in accordance with JESD 51-7.  
 4. The package thermal impedance is calculated in accordance with JESD 51-5.

## recommended operating conditions (see Note 5)

		SN54LV4051A		SN74LV4051A		UNIT
		MIN	MAX	MIN	MAX	
$V_{CC}$	Supply voltage	2‡	5.5	2‡	5.5	V
$V_{IH}$	High-level input voltage, control inputs	$V_{CC} = 2$ V	1.5	1.5		V
		$V_{CC} = 2.3$ V to 2.7 V	$V_{CC} \times 0.7$	$V_{CC} \times 0.7$		
		$V_{CC} = 3$ V to 3.6 V	$V_{CC} \times 0.7$	$V_{CC} \times 0.7$		
		$V_{CC} = 4.5$ V to 5.5 V	$V_{CC} \times 0.7$	$V_{CC} \times 0.7$		
$V_{IL}$	Low-level input voltage, control inputs	$V_{CC} = 2$ V		0.5	0.5	V
		$V_{CC} = 2.3$ V to 2.7 V		$V_{CC} \times 0.3$	$V_{CC} \times 0.3$	
		$V_{CC} = 3$ V to 3.6 V		$V_{CC} \times 0.3$	$V_{CC} \times 0.3$	
		$V_{CC} = 4.5$ V to 5.5 V		$V_{CC} \times 0.3$	$V_{CC} \times 0.3$	
$V_I$	Control input voltage	0	5.5	0	5.5	V
$V_{IO}$	Input/output voltage	0	$V_{CC}$	0	$V_{CC}$	V
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 2.3$ V to 2.7 V		200	200	ns/V
		$V_{CC} = 3$ V to 3.6 V		100	100	
		$V_{CC} = 4.5$ V to 5.5 V		20	20	
$T_A$	Operating free-air temperature	–55	125	–40	85	°C

‡ With supply voltages at or near 2 V, the analog switch on-state resistance becomes very nonlinear. It is recommended that only digital signals be transmitted at these low supply voltages.

NOTE 5: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to TI application report *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

# SN54LV4051A, SN74LV4051A

## 8-CHANNEL ANALOG MULTIPLEXERS/DEMULPLEXERS

SCLS428H – MAY 1999 – REVISED APRIL 2005

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54LV4051A		SN74LV4051A		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
r <sub>on</sub> On-state switch resistance	I <sub>T</sub> = 2 mA, V <sub>I</sub> = V <sub>CC</sub> or GND, V <sub>INH</sub> = V <sub>IL</sub> (see Figure 1)	2.3 V		38	180		225		225	Ω
		3 V		30	150		190		190	
		4.5 V		22	75		100		100	
r <sub>on(p)</sub> Peak on-state resistance	I <sub>T</sub> = 2 mA, V <sub>I</sub> = V <sub>CC</sub> to GND, V <sub>INH</sub> = V <sub>IL</sub>	2.3 V		113	500		600		600	Ω
		3 V		54	180		225		225	
		4.5 V		31	100		125		125	
Δr <sub>on</sub> Difference in on-state resistance between switches	I <sub>T</sub> = 2 mA, V <sub>I</sub> = V <sub>CC</sub> to GND, V <sub>INH</sub> = V <sub>IL</sub>	2.3 V		2.1	30		40		40	Ω
		3 V		1.4	20		30		30	
		4.5 V		1.3	15		20		20	
I <sub>I</sub> Control input current	V <sub>I</sub> = 5.5 V or GND	0 to 5.5 V					±0.1		±1	μA
I <sub>S(off)</sub> Off-state switch leakage current	V <sub>I</sub> = V <sub>CC</sub> and V <sub>O</sub> = GND, or V <sub>I</sub> = GND and V <sub>O</sub> = V <sub>CC</sub> , V <sub>INH</sub> = V <sub>IH</sub> (see Figure 2)	5.5 V					±0.1		±1	μA
I <sub>S(on)</sub> On-state switch leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND, V <sub>INH</sub> = V <sub>IL</sub> (see Figure 3)	5.5 V					±0.1		±1	μA
I <sub>CC</sub> Supply current	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5 V						20	20	μA
C <sub>IC</sub> Control input capacitance	f = 10 MHz	3.3 V		2						pF
C <sub>IS</sub> Common terminal capacitance		3.3 V		23.4						pF
C <sub>OS</sub> Switch terminal capacitance		3.3 V		5.7						pF
C <sub>F</sub> Feedthrough capacitance		3.3 V		0.5						pF

switching characteristics over recommended operating free-air temperature range, V<sub>CC</sub> = 2.5 V ± 0.2 V (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	T <sub>A</sub> = 25°C			SN54LV4051A		SN74LV4051A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>PLH</sub> t <sub>PHL</sub> Propagation delay time	COM or Y <sub>n</sub>	Y <sub>n</sub> or COM	C <sub>L</sub> = 15 pF, (see Figure 4)		1.9	10		16		16	ns
t <sub>PZH</sub> t <sub>PZL</sub> Enable delay time	INH	COM or Y <sub>n</sub>	C <sub>L</sub> = 15 pF, (see Figure 5)		6.6	18		23		23	ns
t <sub>PHZ</sub> t <sub>PLZ</sub> Disable delay time	INH	COM or Y <sub>n</sub>	C <sub>L</sub> = 15 pF, (see Figure 5)		7.4	18		23		23	ns
t <sub>PLH</sub> t <sub>PHL</sub> Propagation delay time	COM or Y <sub>n</sub>	Y <sub>n</sub> or COM	C <sub>L</sub> = 50 pF, (see Figure 5)		3.8	12		18		18	ns
t <sub>PZH</sub> t <sub>PZL</sub> Enable delay time	INH	COM or Y <sub>n</sub>	C <sub>L</sub> = 50 pF, (see Figure 5)		7.8	28		35		35	ns
t <sub>PHZ</sub> t <sub>PLZ</sub> Disable delay time	INH	COM or Y <sub>n</sub>	C <sub>L</sub> = 50 pF, (see Figure 5)		11.5	28		35		35	ns

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

# SN54LV4051A, SN74LV4051A 8-CHANNEL ANALOG MULTIPLEXERS/DEMULPLEXERS

SCLS428H – MAY 1999 – REVISED APRIL 2005

**switching characteristics over recommended operating free-air temperature range,  
V<sub>CC</sub> = 3.3 V ± 0.3 V (unless otherwise noted)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	T <sub>A</sub> = 25°C			SN54LV4051A		SN74LV4051A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay time	COM or Yn	Yn or COM	C <sub>L</sub> = 15 pF, (see Figure 4)	1.2	6	10	10	10	10	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Enable delay time	INH	COM or Yn	C <sub>L</sub> = 15 pF, (see Figure 5)	4.7	12	15	15	15	15	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Disable delay time	INH	COM or Yn	C <sub>L</sub> = 15 pF, (see Figure 5)	5.7	12	15	15	15	15	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay time	COM or Yn	Yn or COM	C <sub>L</sub> = 50 pF, (see Figure 4)	2.5	9	12	12	12	12	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Enable delay time	INH	COM or Yn	C <sub>L</sub> = 50 pF, (see Figure 5)	5.5	20	25	25	25	25	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Disable delay time	INH	COM or Yn	C <sub>L</sub> = 50 pF, (see Figure 5)	8.8	20	25	25	25	25	ns

**switching characteristics over recommended operating free-air temperature range,  
V<sub>CC</sub> = 5 V ± 0.5 V (unless otherwise noted)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	T <sub>A</sub> = 25°C			SN54LV4051A		SN74LV4051A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay time	COM or Yn	Yn or COM	C <sub>L</sub> = 15 pF, (see Figure 4)	0.6	4	7	7	7	7	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Enable delay time	INH	COM or Yn	C <sub>L</sub> = 15 pF, (see Figure 5)	3.5	8	10	10	10	10	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Disable delay time	INH	COM or Yn	C <sub>L</sub> = 15 pF, (see Figure 5)	4.4	8	10	10	10	10	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay time	COM or Yn	Yn or COM	C <sub>L</sub> = 50 pF, (see Figure 4)	1.5	6	8	8	8	8	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Enable delay time	INH	COM or Yn	C <sub>L</sub> = 50 pF, (see Figure 5)	4	14	18	18	18	18	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Disable delay time	INH	COM or Yn	C <sub>L</sub> = 50 pF, (see Figure 5)	6.2	14	18	18	18	18	ns

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

# SN54LV4051A, SN74LV4051A 8-CHANNEL ANALOG MULTIPLEXERS/DEMULTIPLEXERS

SCLS428H – MAY 1999 – REVISED APRIL 2005

analog switch characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			UNIT	
					MIN	TYP	MAX		
Frequency response (switch on)	COM or Y <sub>n</sub>	Y <sub>n</sub> or COM	C <sub>L</sub> = 50 pF, R <sub>L</sub> = 600 Ω, f <sub>in</sub> = 1 MHz (sine wave) (see Note 6 and Figure 6)	2.3 V	20			MHz	
				3 V	25				
				4.5 V	35				
Crosstalk (control input to signal output)	INH	COM or Y <sub>n</sub>	C <sub>L</sub> = 50 pF, R <sub>L</sub> = 600 Ω, f <sub>in</sub> = 1 MHz (square wave) (see Figure 7)	2.3 V	20			mV	
				3 V	35				
				4.5 V	60				
Feedthrough attenuation (switch off)	COM or Y <sub>n</sub>	Y <sub>n</sub> or COM	C <sub>L</sub> = 50 pF, R <sub>L</sub> = 600 Ω, f <sub>in</sub> = 1 MHz (see Note 7 and Figure 8)	2.3 V	-45			dB	
				3 V	-45				
				4.5 V	-45				
Sine-wave distortion	COM or Y <sub>n</sub>	Y <sub>n</sub> or COM	C <sub>L</sub> = 50 pF, R <sub>L</sub> = 10 kΩ, f <sub>in</sub> = 1 kHz (sine wave) (see Figure 9)	V <sub>I</sub> = 2 V <sub>p-p</sub>	2.3 V	0.1			%
				V <sub>I</sub> = 2.5 V <sub>p-p</sub>	3 V	0.1			
				V <sub>I</sub> = 4 V <sub>p-p</sub>	4.5 V	0.1			

NOTES: 6. Adjust f<sub>in</sub> voltage to obtain 0-dBm output. Increase f<sub>in</sub> frequency until dB meter reads -3 dB.  
7. Adjust f<sub>in</sub> voltage to obtain 0-dBm input.

## operating characteristics, V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C

PARAMETER	TEST CONDITIONS	TYP	UNIT
C <sub>pd</sub> Power dissipation capacitance	C <sub>L</sub> = 50 pF, f = 10 MHz	5.9	pF

## PARAMETER MEASUREMENT INFORMATION

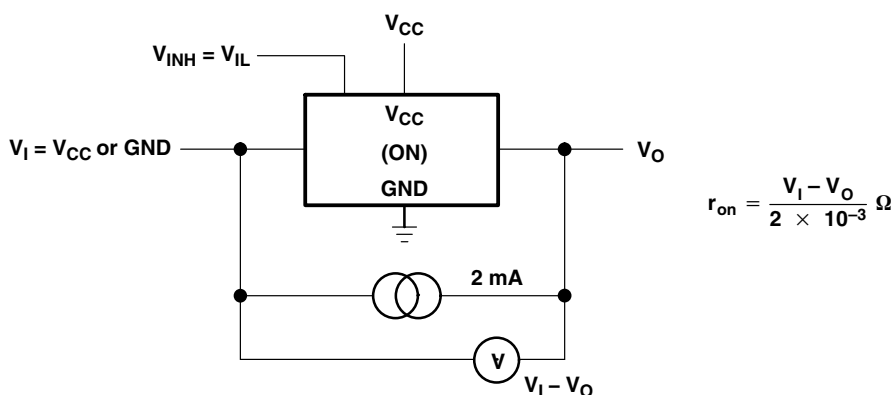
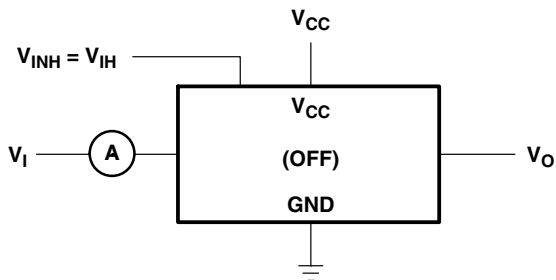


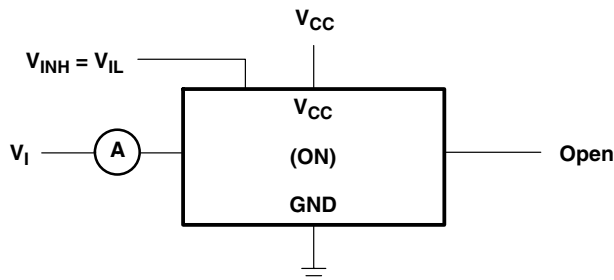
Figure 1. On-State Resistance Test Circuit

PARAMETER MEASUREMENT INFORMATION



Condition 1:  $V_I = 0, V_O = V_{CC}$   
Condition 2:  $V_I = V_{CC}, V_O = 0$

Figure 2. Off-State Switch Leakage-Current Test Circuit



$V_I = V_{CC}$  or  $GND$

Figure 3. On-State Switch Leakage-Current Test Circuit

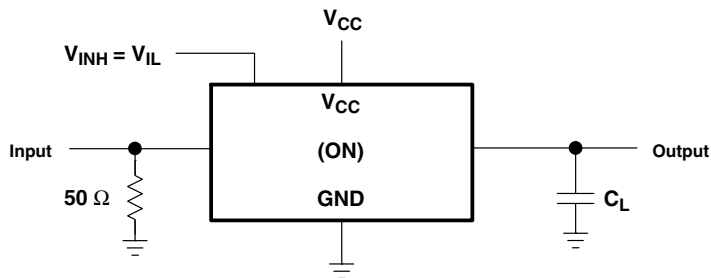
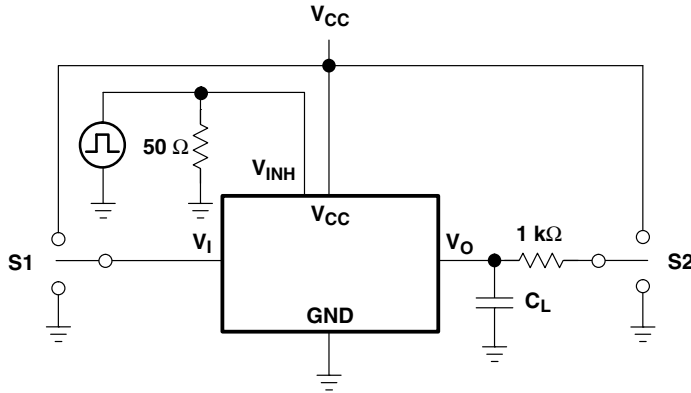


Figure 4. Propagation Delay Time, Signal Input to Signal Output

# SN54LV4051A, SN74LV4051A 8-CHANNEL ANALOG MULTIPLEXERS/DEMULTIPLEXERS

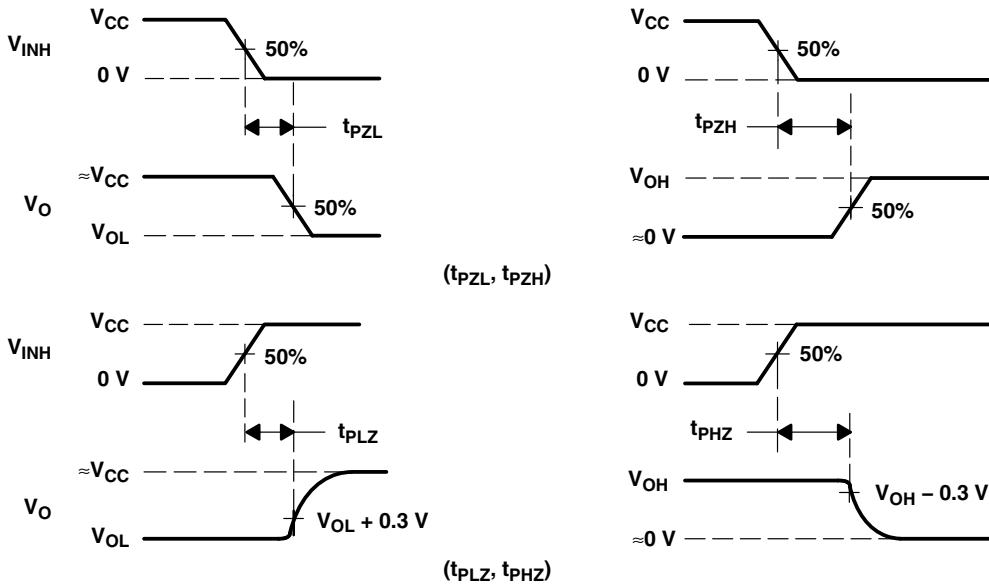
SCLS428H – MAY 1999 – REVISED APRIL 2005

## PARAMETER MEASUREMENT INFORMATION



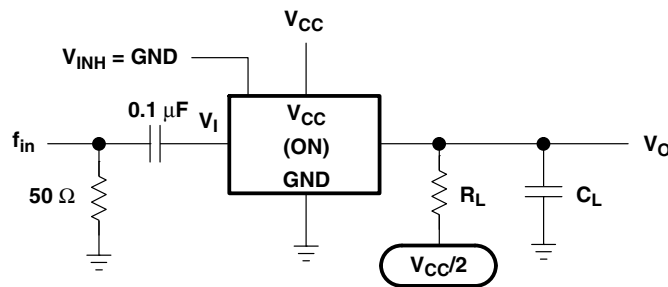
TEST	S1	S2
$t_{PLZ}/t_{PZL}$	GND	$V_{CC}$
$t_{PHZ}/t_{PZH}$	$V_{CC}$	GND

TEST CIRCUIT



VOLTAGE WAVEFORMS

Figure 5. Switching Time ( $t_{PZL}$ ,  $t_{PLZ}$ ,  $t_{PZH}$ ,  $t_{PHZ}$ ), Control to Signal Output



NOTE A:  $f_{in}$  is a sine wave.

Figure 6. Frequency Response (Switch On)



PARAMETER MEASUREMENT INFORMATION

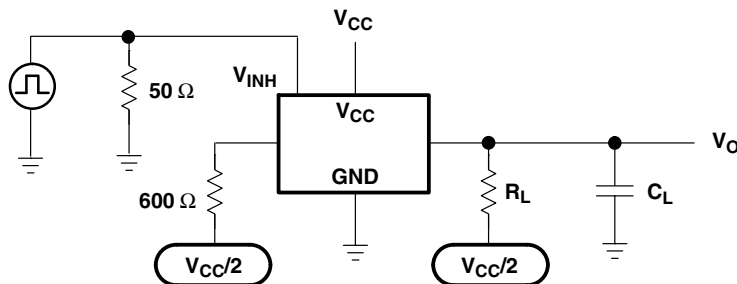


Figure 7. Crosstalk (Control Input, Switch Output)

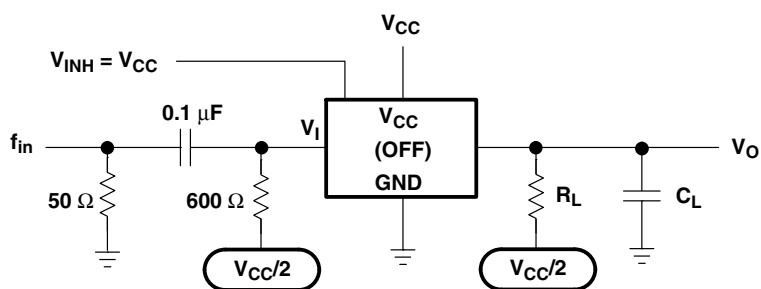


Figure 8. Feedthrough Attenuation (Switch Off)

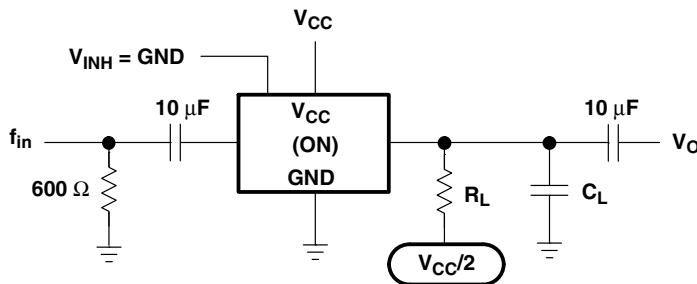


Figure 9. Sine-Wave Distortion

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LV4051AD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV4051A	<a href="#">Samples</a>
SN74LV4051ADBR	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW051A	<a href="#">Samples</a>
SN74LV4051ADBRE4	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW051A	<a href="#">Samples</a>
SN74LV4051ADBRG4	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW051A	<a href="#">Samples</a>
SN74LV4051ADE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV4051A	<a href="#">Samples</a>
SN74LV4051ADG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV4051A	<a href="#">Samples</a>
SN74LV4051ADGVR	ACTIVE	TVSOP	DGV	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW051A	<a href="#">Samples</a>
SN74LV4051ADGVRE4	ACTIVE	TVSOP	DGV	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW051A	<a href="#">Samples</a>
SN74LV4051ADGVRG4	ACTIVE	TVSOP	DGV	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW051A	<a href="#">Samples</a>
SN74LV4051ADR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU   CU SN	Level-1-260C-UNLIM	-40 to 85	LV4051A	<a href="#">Samples</a>
SN74LV4051ADRE4	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	-40 to 85		
SN74LV4051ADRG4	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	-40 to 85	LV4051A	
SN74LV4051AN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	SN74LV4051AN	<a href="#">Samples</a>
SN74LV4051ANE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	SN74LV4051AN	<a href="#">Samples</a>
SN74LV4051ANSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	74LV4051A	<a href="#">Samples</a>
SN74LV4051ANSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	74LV4051A	<a href="#">Samples</a>
SN74LV4051ANSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	74LV4051A	<a href="#">Samples</a>
SN74LV4051APW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW051A	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LV4051APWE4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW051A	<a href="#">Samples</a>
SN74LV4051APWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW051A	<a href="#">Samples</a>
SN74LV4051APWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU   CU SN	Level-1-260C-UNLIM	-40 to 85	LW051A	<a href="#">Samples</a>
SN74LV4051APWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW051A	<a href="#">Samples</a>
SN74LV4051APWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW051A	<a href="#">Samples</a>
SN74LV4051APWT	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW051A	<a href="#">Samples</a>
SN74LV4051APWTE4	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW051A	<a href="#">Samples</a>
SN74LV4051APWTG4	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW051A	<a href="#">Samples</a>
SN74LV4051ARGYR	ACTIVE	VQFN	RGY	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LW051A	<a href="#">Samples</a>
SN74LV4051ARGYRG4	ACTIVE	VQFN	RGY	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LW051A	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

- (3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN74LV4051A :**

- Automotive: [SN74LV4051A-Q1](#)
- Enhanced Product: [SN74LV4051A-EP](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV4051ADBR	SSOP	DB	16	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
SN74LV4051ADGVR	TVSOP	DGV	16	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74LV4051ADR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74LV4051ADR	SOIC	D	16	2500	330.0	16.8	6.5	10.3	2.1	8.0	16.0	Q1
SN74LV4051APWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV4051APWR	TSSOP	PW	16	2000	330.0	12.4	7.0	5.6	1.6	8.0	12.0	Q1
SN74LV4051APWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV4051APWT	TSSOP	PW	16	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV4051ARGYR	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV4051ADBR	SSOP	DB	16	2000	367.0	367.0	38.0
SN74LV4051ADGVR	TVSOP	DGV	16	2000	367.0	367.0	35.0
SN74LV4051ADR	SOIC	D	16	2500	333.2	345.9	28.6
SN74LV4051ADR	SOIC	D	16	2500	364.0	364.0	27.0
SN74LV4051APWR	TSSOP	PW	16	2000	367.0	367.0	35.0
SN74LV4051APWR	TSSOP	PW	16	2000	364.0	364.0	27.0
SN74LV4051APWRG4	TSSOP	PW	16	2000	367.0	367.0	35.0
SN74LV4051APWT	TSSOP	PW	16	250	367.0	367.0	35.0
SN74LV4051ARGYR	VQFN	RGY	16	3000	367.0	367.0	35.0

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

DGV (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN

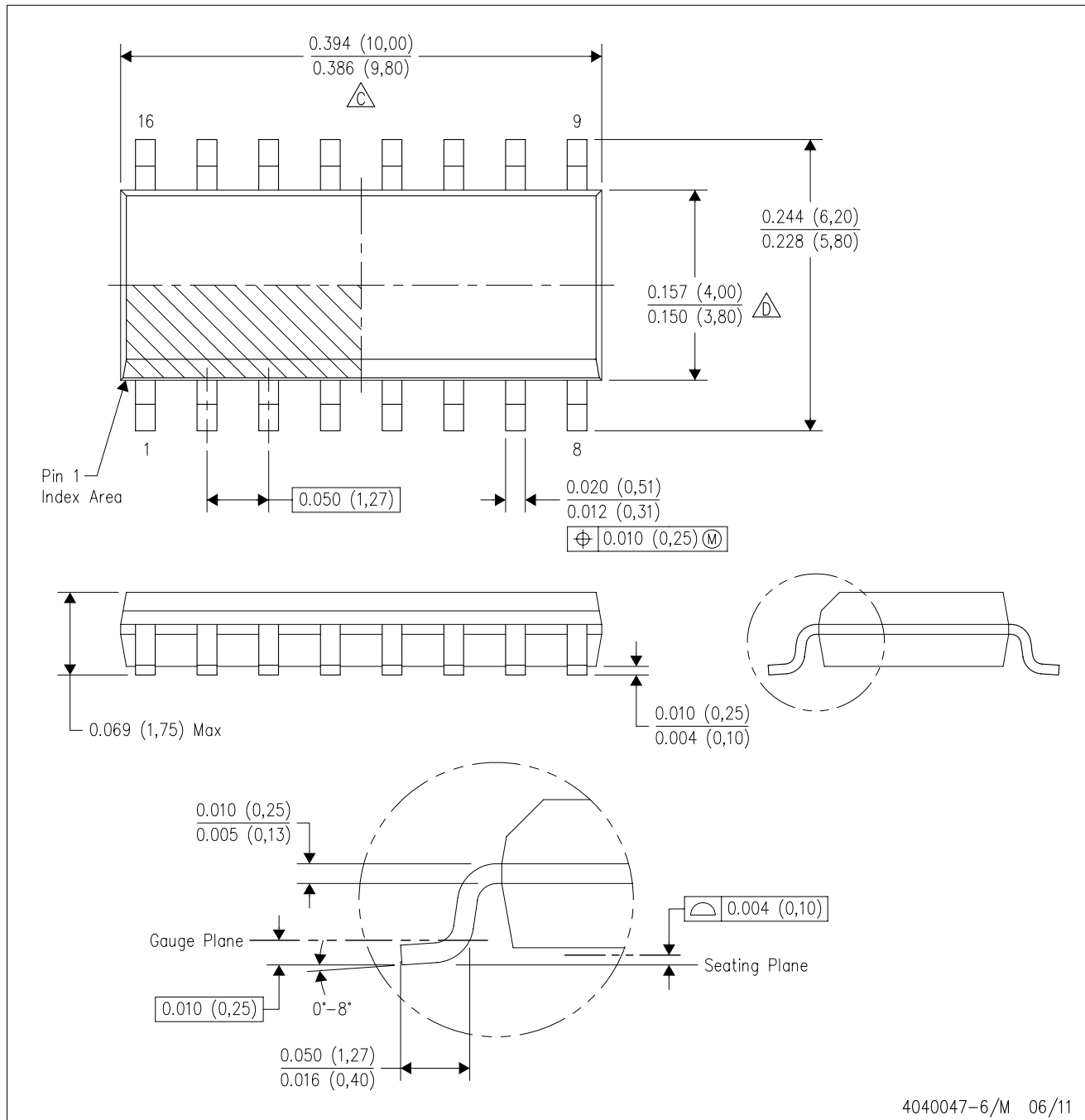


- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194



D (R-PDSO-G16)

PLASTIC SMALL OUTLINE

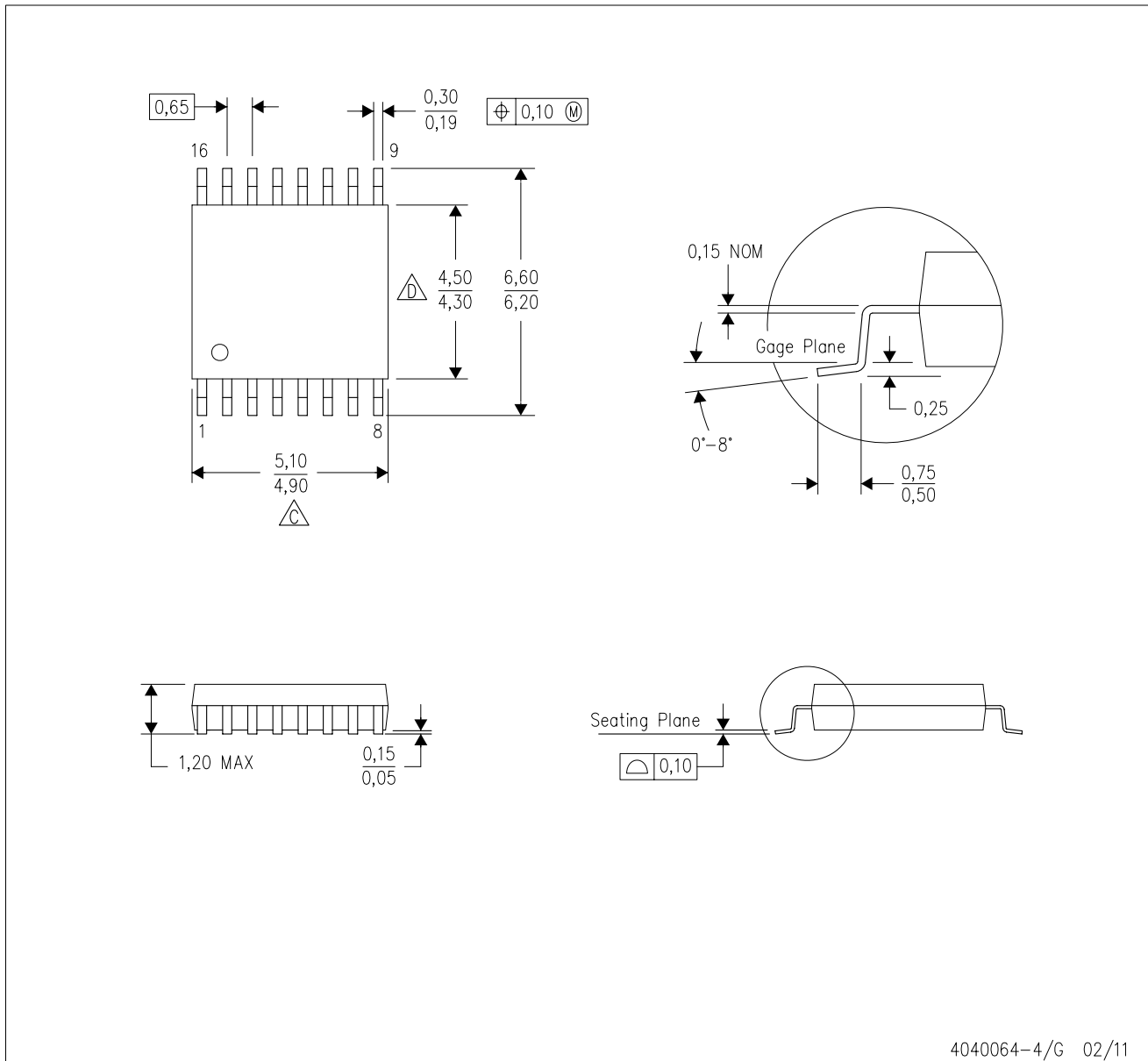


4040047-6/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  -  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040064-4/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DB (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

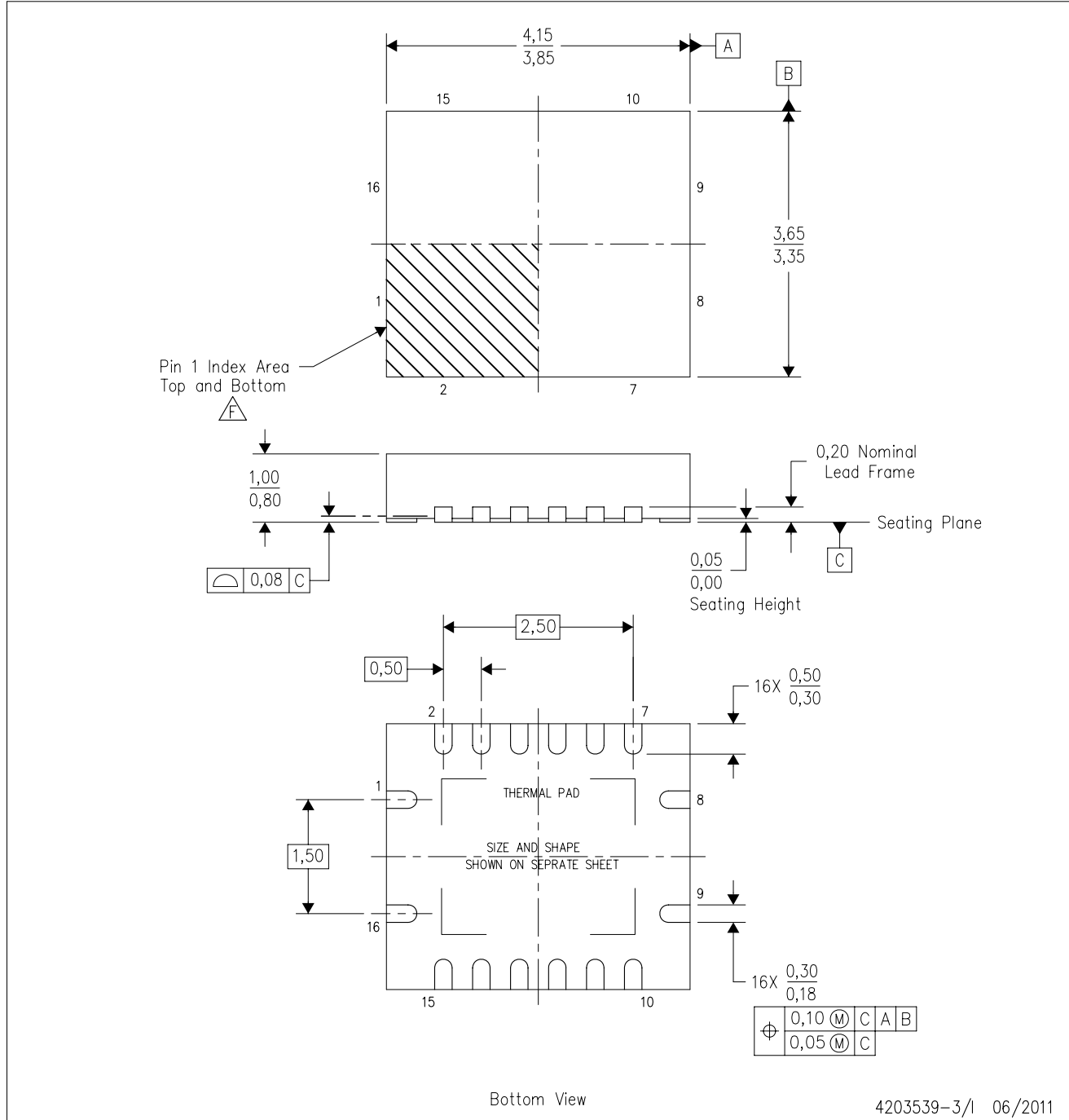
28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

RGY (R-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



4203539-3/1 06/2011

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - QFN (Quad Flatpack No-Lead) package configuration.
  - The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
  - Package complies to JEDEC MO-241 variation BA.

RGY (R-PVQFN-N16)

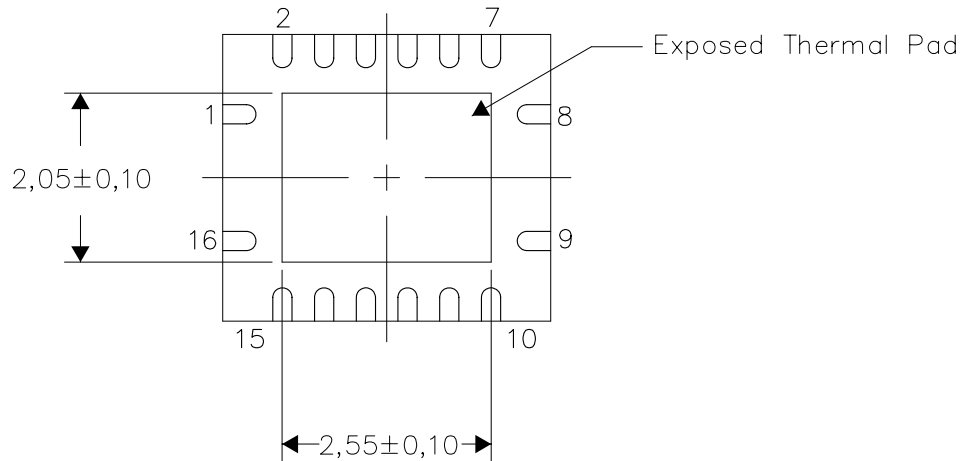
PLASTIC QUAD FLATPACK NO-LEAD

**THERMAL INFORMATION**

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206353-3/0 11/11

NOTE: All linear dimensions are in millimeters

RGY (R-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

## MECHANICAL DATA

**NS (R-PDSO-G\*\*)**

**PLASTIC SMALL-OUTLINE PACKAGE**

**14-PINS SHOWN**



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

### Products

Audio	<a href="http://www.ti.com/audio">www.ti.com/audio</a>
Amplifiers	<a href="http://amplifier.ti.com">amplifier.ti.com</a>
Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>
DLP® Products	<a href="http://www.dlp.com">www.dlp.com</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>
Clocks and Timers	<a href="http://www.ti.com/clocks">www.ti.com/clocks</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>
RFID	<a href="http://www.ti-rfid.com">www.ti-rfid.com</a>
OMAP Applications Processors	<a href="http://www.ti.com/omap">www.ti.com/omap</a>
Wireless Connectivity	<a href="http://www.ti.com/wirelessconnectivity">www.ti.com/wirelessconnectivity</a>

### Applications

Automotive and Transportation	<a href="http://www.ti.com/automotive">www.ti.com/automotive</a>
Communications and Telecom	<a href="http://www.ti.com/communications">www.ti.com/communications</a>
Computers and Peripherals	<a href="http://www.ti.com/computers">www.ti.com/computers</a>
Consumer Electronics	<a href="http://www.ti.com/consumer-apps">www.ti.com/consumer-apps</a>
Energy and Lighting	<a href="http://www.ti.com/energy">www.ti.com/energy</a>
Industrial	<a href="http://www.ti.com/industrial">www.ti.com/industrial</a>
Medical	<a href="http://www.ti.com/medical">www.ti.com/medical</a>
Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
Space, Avionics and Defense	<a href="http://www.ti.com/space-avionics-defense">www.ti.com/space-avionics-defense</a>
Video and Imaging	<a href="http://www.ti.com/video">www.ti.com/video</a>

### TI E2E Community

[e2e.ti.com](http://e2e.ti.com)