

P4C147

ULTRA HIGH SPEED 4K x 1

STATIC CMOS RAM

FEATURES

- Full CMOS, 6T Cell
- High Speed (Equal Access and Cycle Times)
 - 10/12/15/20/25 ns (Commercial)
 - 15/20/25/35 ns (Military)
- Low Power Operation
 - 715 mW Active -10 (Commercial)
 - 550 mW Active -25 (Commercial)
 - 110 mW Standby (TTL Input)
 - 55 mW Standby (CMOS Input)
- Single 5V ± 10% Power Supply
- Separate Input and Output Ports
- Three-State Outputs
- Fully TTL Compatible Inputs and Outputs
- Standard Pinout (JEDEC Approved)
 - 18 Pin 300 mil DIP
 - 18 Pin CERPACK
 - 18 Pin LCC (290 x 430 mils)
 - 18 Pin LCC (295 x 335 mils)

DESCRIPTION

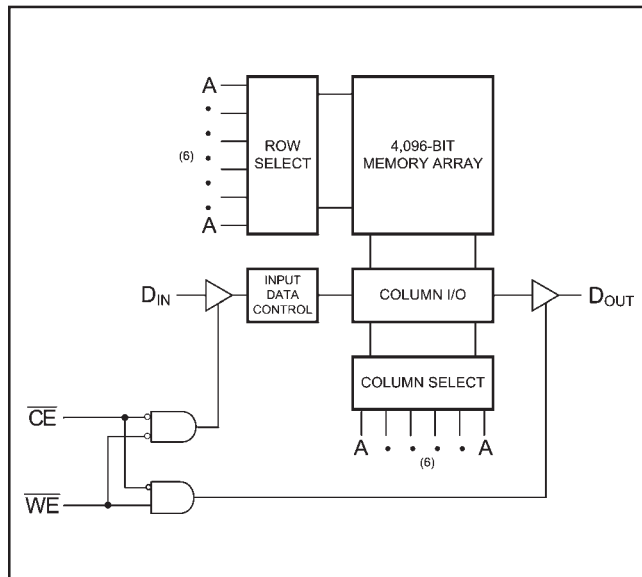
The P4C147 is a 4,096-bit ultra high speed static RAM organized as 4K x 1. The CMOS memory requires no clocks or refreshing, and have equal access and cycle times. Inputs are fully TTL-compatible. The RAM operates from a single 5V ± 10% tolerance power supply.

Access times as fast as 10 nanoseconds are available, permitting greatly enhanced system operating speeds.

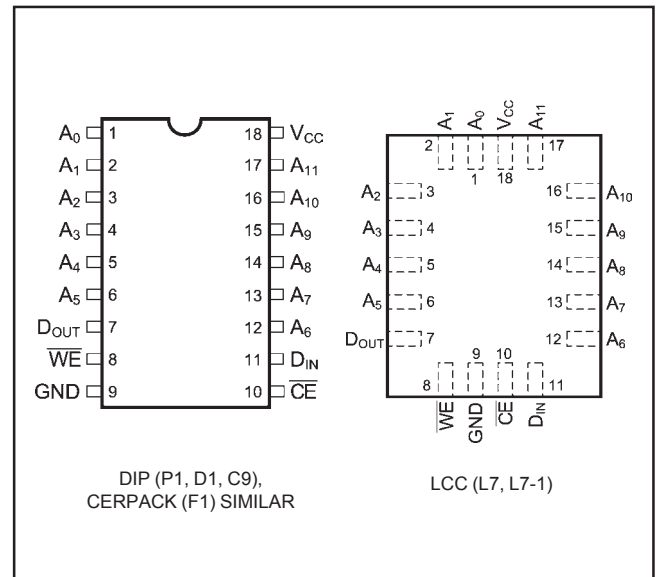
CMOS is utilized to reduce power consumption in both active and standby modes. In addition to very high performance, this device features latch-up protection and single-event-upset protection.

The P4C147 is available in 18 pin 300 mil DIP packages, an 18-pin CERPACK package, and 2 different LCC packages.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



MAXIMUM RATINGS⁽¹⁾

| Symbol | Parameter | Value | Unit |
|------------|---|------------------------|------|
| V_{CC} | Power Supply Pin with Respect to GND | -0.5 to +7 | V |
| V_{TERM} | Terminal Voltage with Respect to GND (up to 7.0V) | -0.5 to $V_{CC} + 0.5$ | V |
| T_A | Operating Temperature | -55 to +125 | °C |

| Symbol | Parameter | Value | Unit |
|------------|------------------------|-------------|------|
| T_{BIAS} | Temperature Under Bias | -55 to +125 | °C |
| T_{STG} | Storage Temperature | -65 to +150 | °C |
| P_T | Power Dissipation | 1.0 | W |
| I_{OUT} | DC Output Current | 50 | mA |

RECOMMENDED OPERATING CONDITIONS

| Grade ⁽²⁾ | Ambient Temp | Gnd | V_{CC} |
|----------------------|-----------------|-----|------------|
| Commercial | 0°C to 70°C | 0V | 5.0V ± 10% |
| Military | -55°C to +125°C | 0V | 5.0V ± 10% |

CAPACITANCES⁽⁴⁾

($V_{CC} = 5.0V$, $T_A = 25^\circ C$, $f = 1.0MHz$)

| Symbol | Parameter | Conditions | Typ. | Unit |
|-----------|--------------------|----------------|------|------|
| C_{IN} | Input Capacitance | $V_{IN} = 0V$ | 5 | pF |
| C_{OUT} | Output Capacitance | $V_{OUT} = 0V$ | 7 | pF |

DC ELECTRICAL CHARACTERISTICS

Over recommended operating temperature and supply voltage (2)

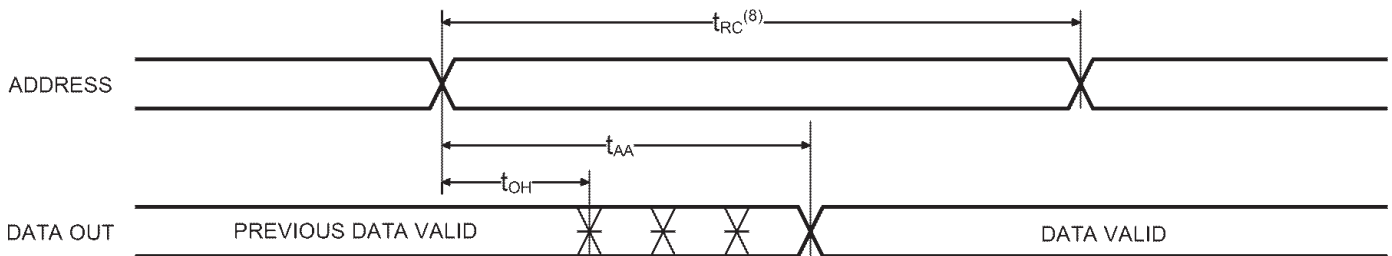
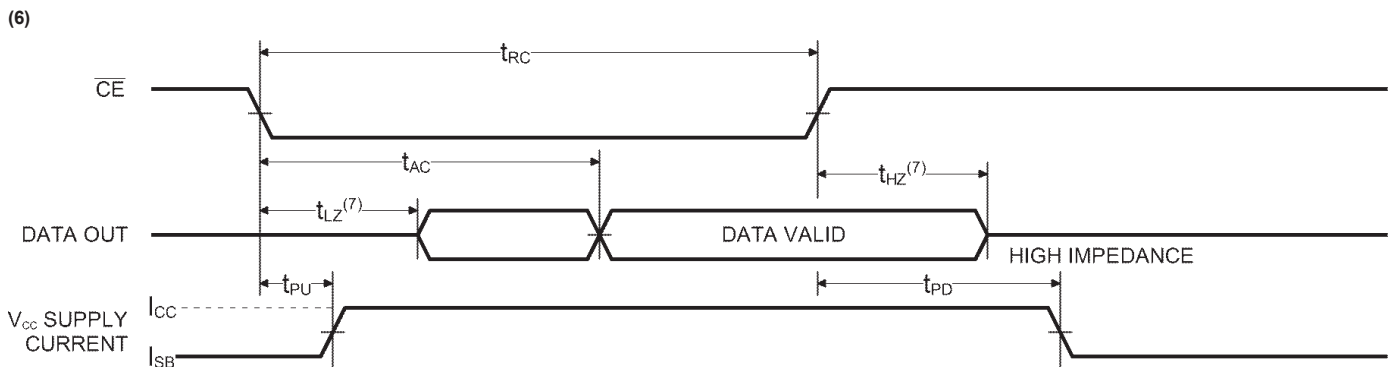
| Symbol | Parameter | Test Conditions | P4C147 | | Unit |
|-----------|--|--|-----------------------------|-----------------|------|
| | | | Min. | Max. | |
| V_{OH} | Output High Voltage (TTL Load) | $I_{OH} = -4 \text{ mA}$, $V_{CC} = \text{Min.}$ | 2.4 | | V |
| V_{OL} | Output Low Voltage (TTL Load) | $I_{OL} = +8 \text{ mA}$, $V_{CC} = \text{Min.}$ | | 0.4 | V |
| V_{IH} | Input High Voltage | | 2.2 | $V_{CC} = +0.5$ | V |
| V_{IL} | Input Low Voltage | | -0.5 ⁽³⁾ | 0.8 | V |
| I_{LI} | Input Leakage Current | $V_{CC} = \text{Max.}$, $V_{IN} = \text{GND to } V_{CC}$ | Mil. -10 Comm'l -5 | +10 +5 | µA |
| I_{LO} | Output Leakage Current | $V_{CC} = \text{Max.}$, $\overline{CE} = V_{IH}$, $V_{OUT} = \text{GND to } V_{CC}$ | Mil. -10 Comm'l -5 | +10 +5 | µA |
| I_{SB} | Standby Power Supply Current (TTL Input Levels) | $\overline{CE} \geq V_{IH}$, $V_{CC} = \text{Max.}$, $f = \text{Max.}$, Output Open | Mil. — Comm'l — | 30 23 | mA |
| I_{SB1} | Standby Power Supply Current (CMOS Input Levels) | $\overline{CE} \geq V_{HC}$, $V_{CC} = \text{Max.}$, $f = 0$, Output Open $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$ | Mil. — Comm'l — | 15 10 | mA |

POWER DISSIPATION CHARACTERISTICS VS. SPEED

| Symbol | Parameter | Temperature Range | -10 | -12 | -15 | -20 | -25 | -35 | Unit |
|----------|---------------------------|------------------------|------------|------------|------------|------------|------------|------------|----------|
| | | | | | | | | | |
| I_{CC} | Dynamic Operating Current | Commercial Military | 130 N/A | 130 N/A | 120 145 | 115 135 | 100 125 | N/A 120 | mA mA |

AC CHARACTERISTICS—READ CYCLE $(V_{CC} = 5V \pm 10\%$, All Temperature Ranges)⁽²⁾

| Sym. | Parameter | -10 | | -12 | | -15 | | -20 | | -25 | | -35 | | Unit |
|----------|----------------------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|------|
| | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| t_{RC} | Read Cycle Time | 10 | | 12 | | 15 | | 20 | | 25 | | 35 | | ns |
| t_{AA} | Address Access Time | | 10 | | 12 | | 15 | | 20 | | 25 | | 35 | ns |
| t_{AC} | Chip Enable Access Time | | 10 | | 12 | | 15 | | 20 | | 25 | | 35 | ns |
| t_{OH} | Output Hold from Address Change | 2 | | 2 | | 2 | | 2 | | 2 | | 2 | | ns |
| t_{LZ} | Chip Enable to Output in Low Z | 2 | | 2 | | 2 | | 2 | | 2 | | 2 | | ns |
| t_{HZ} | Chip Disable to Output in High Z | | 4 | | 5 | | 6 | | 8 | | 10 | | 14 | ns |
| t_{PU} | Chip Enable to Power Up Time | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| t_{PD} | Chip Disable to Power Down Time | | 10 | | 12 | | 15 | | 20 | | 25 | | 35 | ns |

TIMING WAVEFORM OF READ CYCLE NO. 1⁽⁵⁾**TIMING WAVEFORM OF READ CYCLE NO. 2⁽⁶⁾****Notes:**

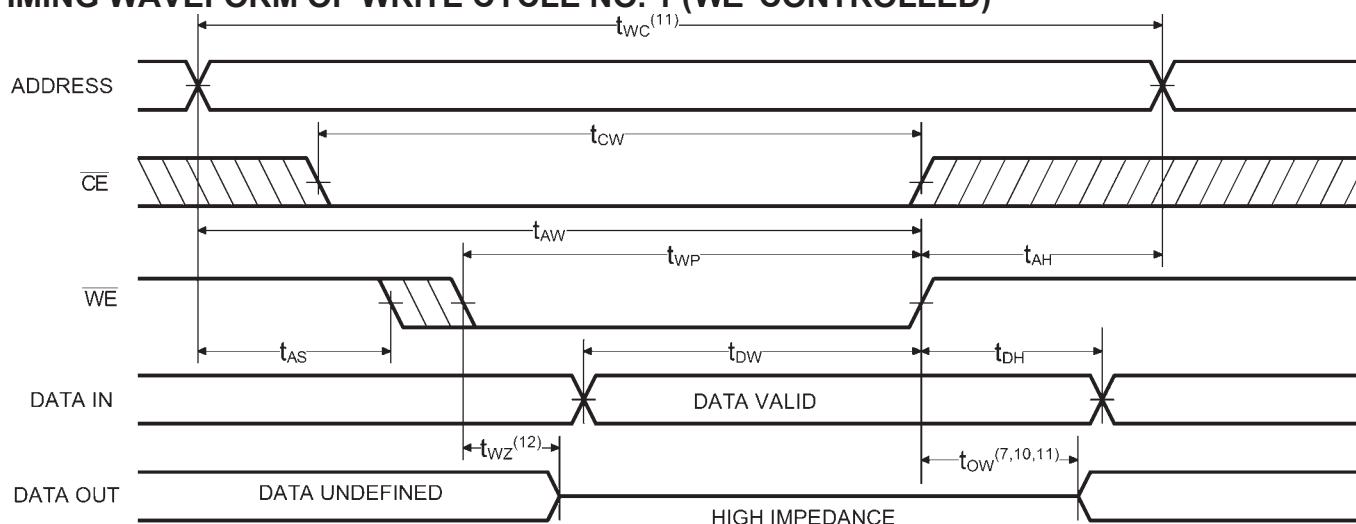
- Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to MAXIMUM rating conditions for extended periods may affect reliability.
- Extended temperature operation guaranteed with 400 linear feet per minute of air flow.
- Transient inputs with V_{IL} and I_{IL} not more negative than $-3.0V$ and $-100mA$, respectively, are permissible for pulse widths up to 20 ns.
- This parameter is sampled and not 100% tested.
- \overline{CE} is LOW and \overline{WE} is HIGH for READ cycle.
- \overline{WE} is HIGH, and address must be valid prior to or coincident with \overline{CE} transition LOW.
- Transition is measured $\pm 200mV$ from steady state voltage prior to change with specified loading in Figure 1. This parameter is sampled and not 100% tested.
- Read Cycle Time is measured from the last valid address to the first transitioning address.

AC CHARACTERISTICS—WRITE CYCLE

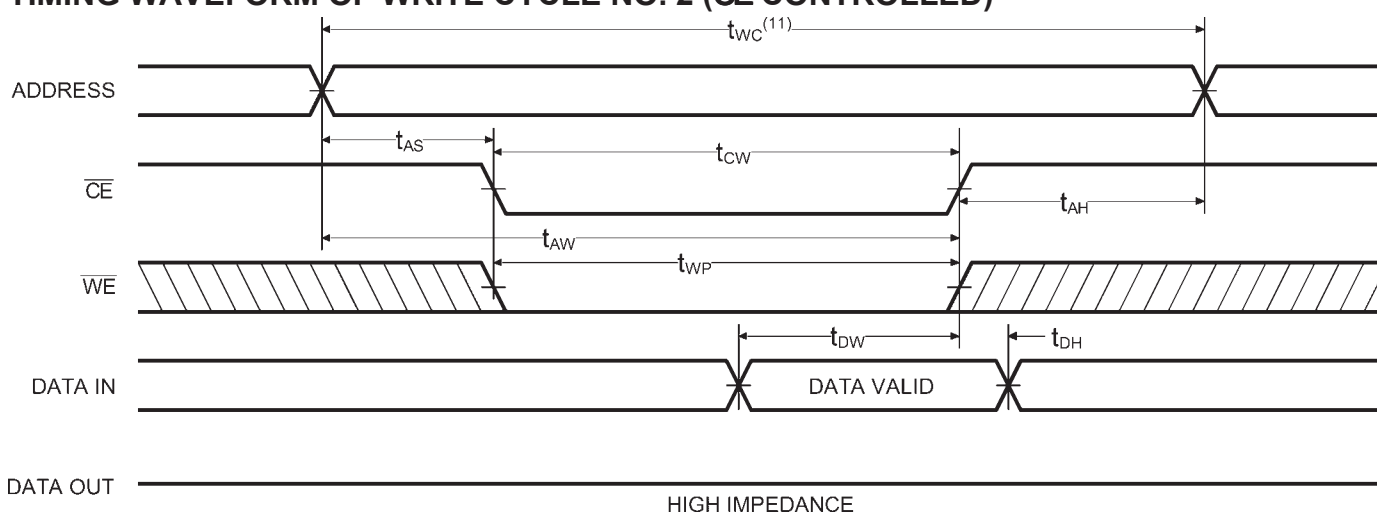
($V_{CC} = 5V \pm 10\%$, All Temperature Ranges)⁽²⁾

| Sym. | Parameter | -10 | | -12 | | -15 | | -20 | | -25 | | -35 | | Unit |
|----------|-------------------------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|------|
| | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| t_{WC} | Write Cycle Time | 10 | | 12 | | 15 | | 20 | | 25 | | 35 | | ns |
| t_{CW} | Chip Enable Time to End of Write | 8 | | 10 | | 12 | | 15 | | 20 | | 25 | | ns |
| t_{AW} | Address Valid to End of Write | 8 | | 10 | | 12 | | 15 | | 20 | | 25 | | ns |
| t_{AS} | Address Set-up Time | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| t_{WP} | Write Pulse Width | 8 | | 10 | | 12 | | 14 | | 15 | | 18 | | ns |
| t_{AH} | Address Hold Time from End of Write | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| t_{DW} | Data Valid to End of Write | 5 | | 6 | | 7 | | 9 | | 12 | | 15 | | ns |
| t_{DH} | Data Hold Time | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| t_{WZ} | Write Enable to Output in High Z | | 5 | | 6 | | 7 | | 9 | | 12 | | 15 | ns |
| t_{OW} | Output Active from End of Write | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns |

TIMING WAVEFORM OF WRITE CYCLE NO. 1 (\overline{WE} CONTROLLED)⁽⁹⁾



TIMING WAVEFORM OF WRITE CYCLE NO. 2 (\overline{CE} CONTROLLED)⁽⁹⁾



Notes:

- 9. \overline{CE} and \overline{WE} must be LOW for WRITE cycle.
- 10. If \overline{CE} goes HIGH simultaneously with \overline{WE} high, the output remains in a high impedance state.
- 11. Write Cycle Time is measured from the last valid address to the first transition address.

AC TEST CONDITIONS

| | |
|-------------------------------|---------------------|
| Input Pulse Levels | GND to 3.0V |
| Input Rise and Fall Times | 3ns |
| Input Timing Reference Level | 1.5V |
| Output Timing Reference Level | 1.5V |
| Output Load | See Figures 1 and 2 |

TRUTH TABLE

| Mode | \overline{CE} | \overline{WE} | Output | Power |
|---------|-----------------|-----------------|------------------|---------|
| Standby | H | X | High Z | Standby |
| Read | L | H | D _{OUT} | Active |
| Write | L | L | High Z | Active |

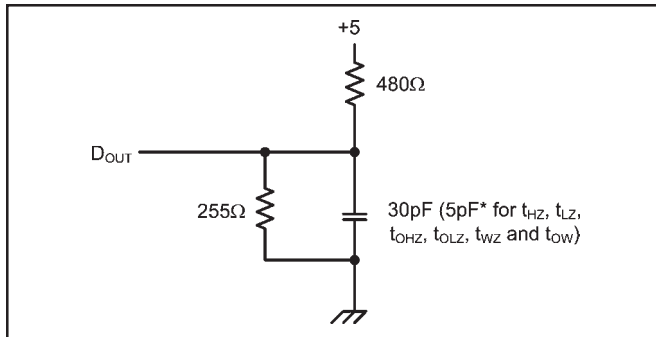


Figure 1. Output Load

* including scope and test fixture.

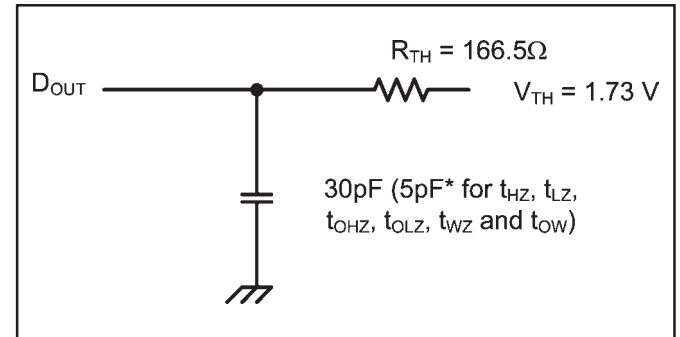


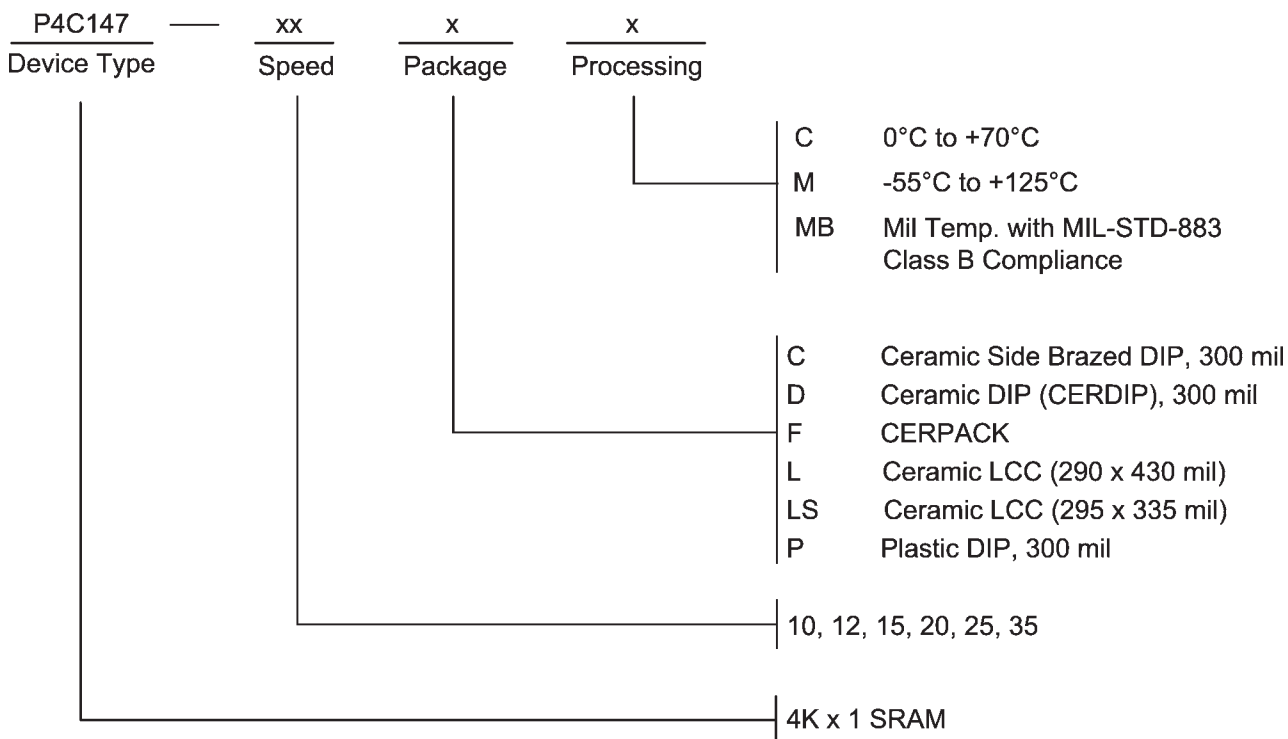
Figure 2. Thevenin Equivalent

Note:

Due to the ultra-high speed of the P4C147, care must be taken when testing this device; an inadequate setup can cause a normal functioning part to be rejected as faulty. Long high-inductance leads that cause supply bounce must be avoided by bringing the V_{CC} and ground planes directly up to the contactor fingers. A 0.01 μF high frequency capacitor

is also required between V_{CC} and ground. To avoid signal reflections, proper termination must be used; for example, a 50Ω test environment should be terminated into a 50Ω load with 1.73V (Thevenin Voltage) at the comparator input, and a 116Ω resistor must be used in series with D_{OUT} to match 166Ω (Thevenin Resistance).

ORDERING INFORMATION



SELECTION GUIDE

The P4C147 is available in the following temperature, speed and package options.

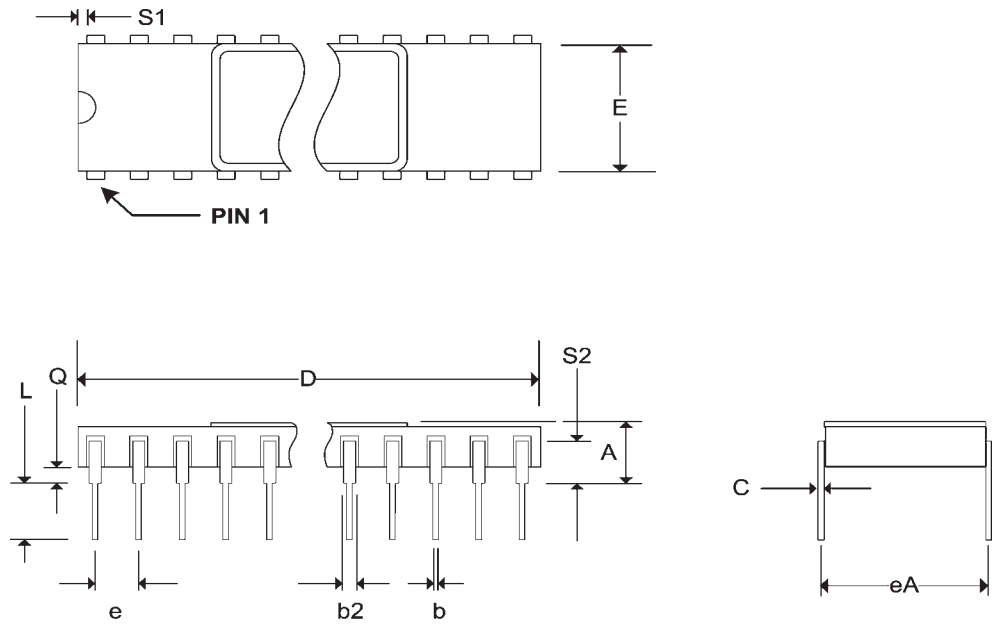
| Temperature Range | Package | Speed (ns) | | | | | |
|------------------------|---------------------|------------|-------|---------|---------|---------|---------|
| | | 10 | 12 | 15 | 20 | 25 | 35 |
| Commercial Temperature | Plastic DIP | -10PC | -12PC | -15PC | -20PC | -25PC | N/A |
| Military Temperature | CERDIP | N/A | N/A | -15DM | -20DM | -25DM | -35DM |
| | Side Brazed DIP | N/A | N/A | -15CM | -20CM | -25CM | -35CM |
| | LCC (290 x 430 mil) | N/A | N/A | -15LM | -20LM | -25LM | -35LM |
| | LCC (295 x 335 mil) | N/A | N/A | -15LSM | -20LSM | -25LSM | -35LSM |
| | CERPACK | N/A | N/A | -15FM | -20FM | -25FM | -35FM |
| Military Processed* | CERDIP | N/A | N/A | -15DMB | -20DMB | -25DMB | -35DMB |
| | Side Brazed DIP | N/A | N/A | -15CMB | -20CMB | -25CMB | -35CMB |
| | LCC (290 x 430 mil) | N/A | N/A | -15LMB | -20LMB | -25LMB | -35LMB |
| | LCC (295 x 335 mil) | N/A | N/A | -15LSMB | -20LSMB | -25LSMB | -35LSMB |
| | CERPACK | N/A | N/A | -15FMB | -20FMB | -25FMB | -35FMB |

* Military temperature range with MIL-STD-883, Class B processing.

N/A = Not Available

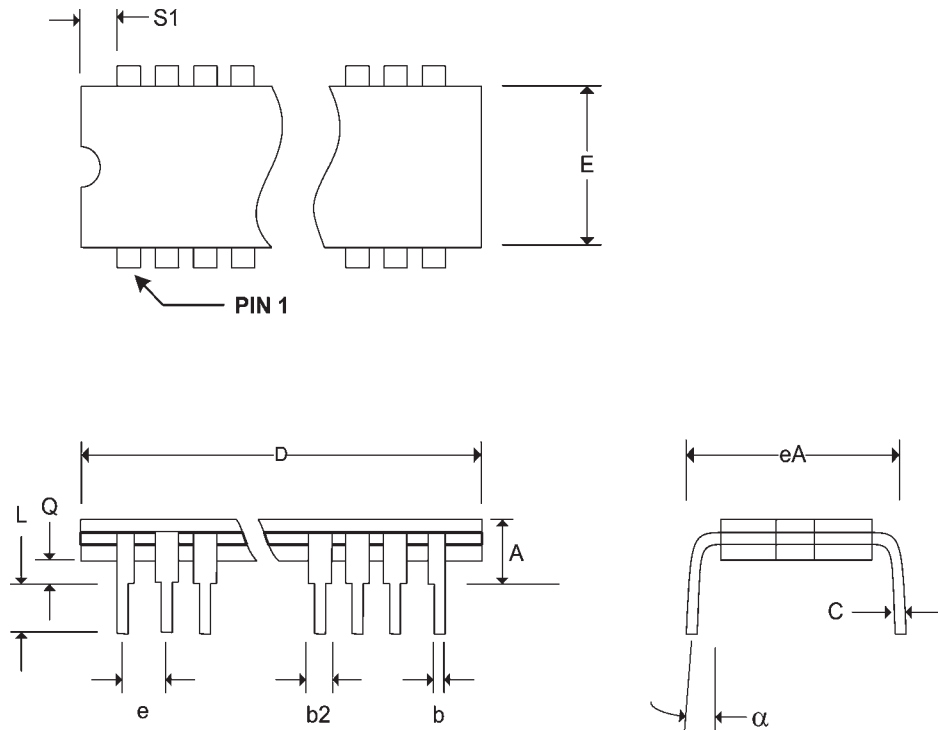
| | | |
|--------|--------------|------------|
| Pkg # | C9 | |
| # Pins | 18 (300 Mil) | |
| Symbol | Min | Max |
| A | - | 0.200 |
| b | 0.014 | 0.026 |
| b2 | 0.030 | 0.065 |
| C | 0.008 | 0.018 |
| D | - | 0.960 |
| E | 0.220 | 0.320 |
| eA | 0.300 BSC | |
| e | 0.100 BSC | |
| L | 0.125 | 0.200 |
| Q | 0.015 | 0.070 |
| S1 | 0.005 | - |
| S2 | 0.005 | - |

SIDE BRAZED DUAL IN-LINE PACKAGE



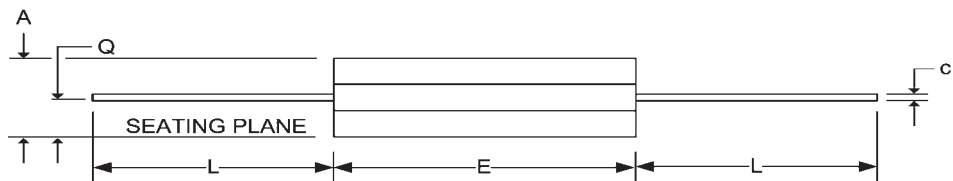
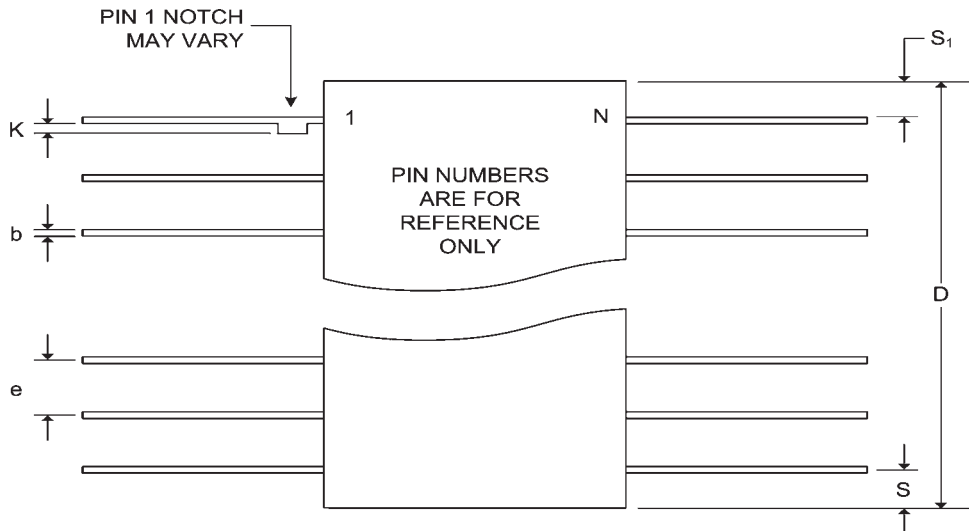
| | | |
|----------|--------------|------------|
| Pkg # | D1 | |
| # Pins | 18 (300 Mil) | |
| Symbol | Min | Max |
| A | - | 0.200 |
| b | 0.014 | 0.026 |
| b2 | 0.045 | 0.065 |
| C | 0.008 | 0.018 |
| D | - | 0.960 |
| E | 0.220 | 0.310 |
| eA | 0.300 BSC | |
| e | 0.100 BSC | |
| L | 0.125 | 0.200 |
| Q | 0.015 | 0.070 |
| S1 | 0.005 | - |
| α | 0° | 15° |

CERDIP DUAL IN-LINE PACKAGE



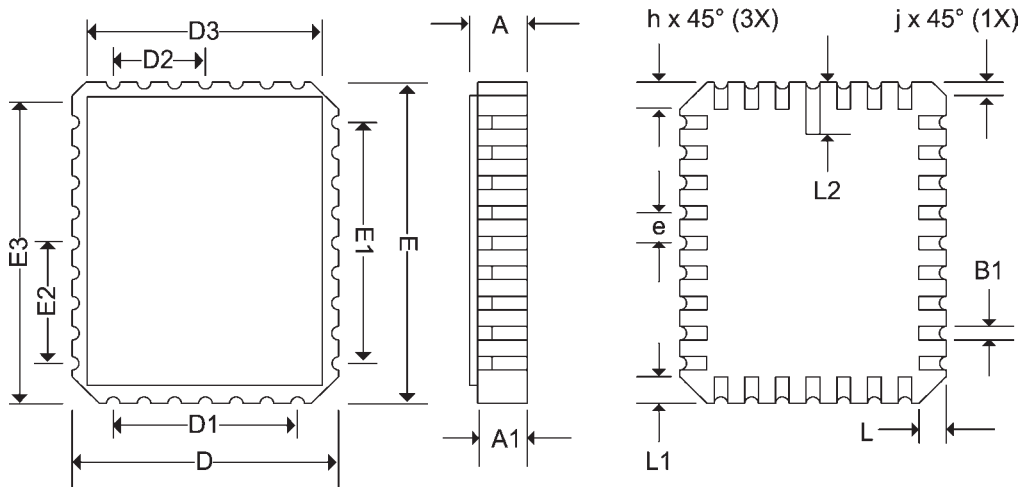
| Pkg # | F1 | |
|--------|-----------|-------|
| # Pins | 18 | |
| Symbol | Min | Max |
| A | 0.045 | 0.092 |
| b | 0.015 | 0.022 |
| c | 0.004 | 0.009 |
| D | - | 0.540 |
| E | 0.245 | 0.370 |
| e | 0.050 BSC | |
| k | 0.005 | 0.018 |
| L | 0.250 | 0.370 |
| Q | 0.026 | 0.045 |
| S | - | 0.085 |
| S1 | 0.005 | - |

CERPACK CERAMIC FLAT PACKAGES



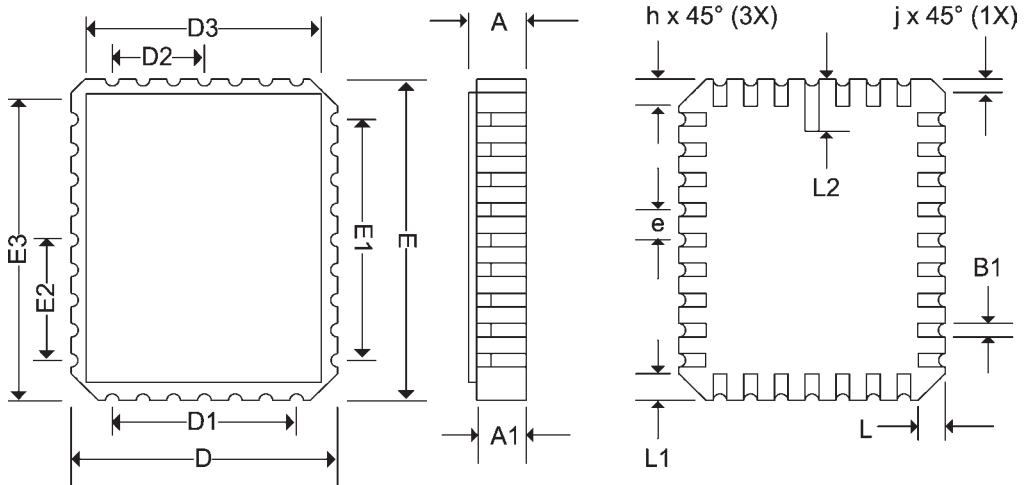
| Pkg # | L7 | |
|--------|-----------|-------|
| # Pins | 18 | |
| Symbol | Min | Max |
| A | 0.060 | 0.075 |
| A1 | 0.050 | 0.065 |
| B1 | 0.022 | 0.028 |
| D | 0.280 | 0.305 |
| D1 | .150 BSC | |
| D2 | .075 BSC | |
| D3 | - | 0.305 |
| E | 0.417 | 0.440 |
| E1 | 0.200 BSC | |
| E2 | 0.100 BSC | |
| E3 | - | 0.440 |
| e | 0.050 BSC | |
| h | 0.040 REF | |
| j | 0.020 REF | |
| L | 0.045 | 0.055 |
| L1 | 0.075 | 0.090 |
| L2 | 0.075 | 0.148 |
| ND | 4 | |
| NE | 5 | |

RECTANGULAR LEADLESS CHIP CARRIER



| | | |
|--------|-------------|------------|
| Pkg # | L7-1 | |
| # Pins | 18 | |
| Symbol | Min | Max |
| A | 0.060 | 0.075 |
| A1 | 0.050 | 0.065 |
| B1 | 0.022 | 0.028 |
| D | 0.280 | 0.305 |
| D1 | .150 BSC | |
| D2 | .075 BSC | |
| D3 | - | 0.305 |
| E | 0.345 | 0.365 |
| E1 | 0.200 BSC | |
| E2 | 0.100 BSC | |
| E3 | - | 0.365 |
| e | 0.050 BSC | |
| h | 0.040 REF | |
| j | 0.020 REF | |
| L | 0.045 | 0.055 |
| L1 | 0.045 | 0.055 |
| L2 | 0.075 | 0.125 |
| ND | 4 | |
| NE | 5 | |

RECTANGULAR LEADLESS CHIP CARRIER



| | | |
|--------|------------|------------|
| Pkg # | P1 | |
| # Pins | 18 | |
| Symbol | Min | Max |
| A | - | 0.210 |
| A1 | 0.015 | - |
| b | 0.014 | 0.022 |
| b2 | 0.045 | 0.070 |
| C | 0.008 | 0.014 |
| D | 0.880 | 0.920 |
| E1 | 0.240 | 0.280 |
| E | 0.300 | 0.325 |
| e | 0.100 BSC | |
| eB | - | 0.430 |
| L | 0.115 | 0.150 |
| α | 0° | 15° |

PLASTIC DUAL IN-LINE PACKAGE

