

74LS113, S113 Flip-Flops

Dual J-K Edge-Triggered Flip-Flop
Product Specification

Logic Products

DESCRIPTION

The '113 is a dual J-K negative edge-triggered flip-flop featuring individual J, K, Set and Clock inputs. The asynchronous Set (\bar{S}_D) input, when LOW, forces the outputs to the steady state levels as shown in the Function Table regardless of the levels at the other inputs.

A HIGH level on the Clock (\bar{CP}) input enables the J and K inputs and data will be accepted. The logic levels at the J and K inputs may be allowed to change while the \bar{CP} is HIGH and the flip-flop will perform according to the Function Table as long as minimum set-up and hold times are observed. Output state changes are initiated by the HIGH-to-LOW transition of \bar{CP} .

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74LS113	45MHz	4mA
74S113	125MHz	15mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74S113N, N74LS113N

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

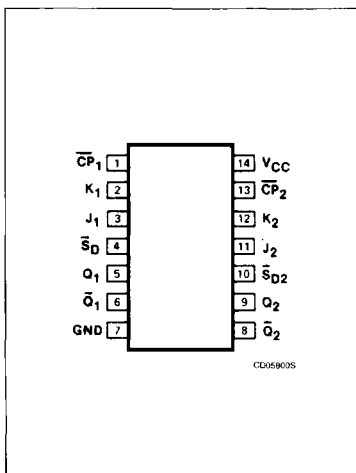
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74S	74LS
\bar{CP}	Clock input	2Sul	4LSul
\bar{S}_D	Set inputs	3.5Sul	3LSul
J, K	Data inputs	1Sul	1LSul
Q, \bar{Q}	Outputs	10Sul	10LSul

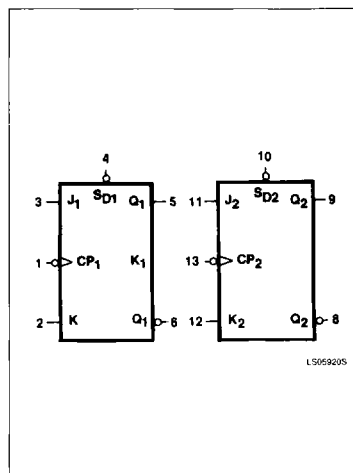
NOTE:

A 74S unit load (Sul) is $50\mu A$ I_{IH} and $-2.0mA$ I_{IL} , and a 74LS unit load (LSul) is $20\mu A$ I_{IH} and $-0.4mA$ I_{IL} .

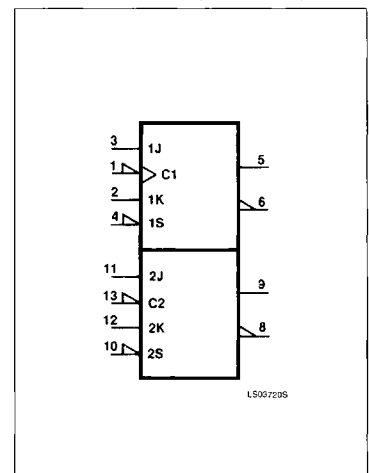
PIN CONFIGURATION



LOGIC SYMBOL



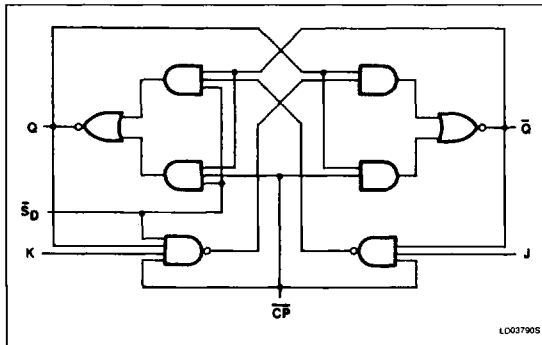
LOGIC SYMBOL (IEEE/IEC)



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LOGIC DIAGRAM



FUNCTION TABLE

OPERATING MODE	INPUTS				OUTPUTS	
	\bar{S}_D	\bar{C}_P	J	K	Q	\bar{Q}
Asynchronous set	L	X	X	X	H	L
Toggle	H	↓	h	h	\bar{q}	q
Load "0" (reset)	H	↓	l	h	L	H
Load "1" (set)	H	↓	h	l	H	L
Hold "no change"	H	↓	l	l	q	\bar{q}

H = HIGH voltage level steady state.
 h = HIGH voltage level one set-up time prior to the HIGH-to-LOW Clock transition.
 L = LOW voltage level steady state.
 l = LOW voltage level one set-up time prior to the HIGH-to-LOW Clock transition.
 q = Lower case letters indicate the state of the referenced output one set-up time prior to the HIGH-to-LOW Clock transition.
 X = Don't care.
 ↓ = HIGH-to-LOW Clock transition.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	74LS	74S	UNIT
V_{CC} Supply voltage	7.0	7.0	V
V_{IN} Input voltage	-0.5 to -7.0	-0.5 to +5.5	V
I_{IN} Input current	-30 to +1	-30 to +5	mA
V_{OUT} Voltage applied to output in HIGH output state	-0.5 to + V_{CC}	-0.5 to + V_{CC}	V
T_A Operating free-air temperature range	0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	74LS			74S			UNIT
	Min	Nom	Max	Min	Nom	Max	
V_{CC} Supply voltage	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH} HIGH-level input voltage	2.0			2.0			V
V_{IL} LOW-level input voltage			+0.8			+0.8	V
I_{IK} Input clamp current			-18			-18	mA
I_{OH} HIGH-level output current			-400			-1000	μA
I_{OL} LOW-level output current			8			20	mA
T_A Operating free-air temperature	0		70	0		70	°C

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DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	74LS113			74S113			UNIT	
		Min	Typ ²	Max	Min	Typ ²	Max		
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	2.7	3.4		2.7	3.4		V	
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX		0.35	0.5		0.5	V	
		I _{OL} = 4mA (74LS)		0.25	0.4			V	
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			-1.5			-1.2	V	
I _I Input current at maximum input voltage	V _{CC} = MAX	V _I = 5.5V					1.0	mA	
		V _I = 7.0V	J, K Inputs		0.1				mA
			\bar{S}_D Inputs		0.3				mA
			$\bar{C}\bar{P}$ Inputs		0.4				mA
I _{IH} HIGH-level input current	V _{CC} = MAX	V _I = 2.7V	J, K Inputs		20		50	μ A	
			\bar{S}_D Inputs		60		100	μ A	
			$\bar{C}\bar{P}$ Inputs		80		100	μ A	
I _{IL} LOW-level input current	V _{CC} = MAX	V _I = 0.4V	J, K Inputs		-0.4			mA	
			\bar{S}_D Inputs		-0.8			mA	
			$\bar{C}\bar{P}$ Inputs		-0.8			mA	
		V _I = 0.5V	J, K Inputs					-1.6	mA
			\bar{S}_D Inputs					-7	mA
			$\bar{C}\bar{P}$ Inputs					-4	mA
I _{OS} Short-circuit output current ³	V _{CC} = MAX	-20		-100	-40		-100	mA	
I _{CC} Supply current ⁴ (total)	V _{CC} = MAX		4	8		15	50	mA	

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- With the Clock input grounded and all outputs open, I_{CC} is measured with the Q and \bar{Q} outputs HIGH in turn.

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	74LS		74S		UNIT
		C _L = 15pF, R _L = 2k Ω		C _L = 15pF, R _L = 280 Ω		
		Min	Max	Min	Max	
f _{MAX} Maximum clock frequency	Waveform 1	30		80		MHz
t _{PLH} Propagation delay	Waveform 1		20		7.0	ns
t _{PHL} Clock to output			30		7.0	
t _{PLH} Propagation delay	Waveform 2		20		7.0	ns
t _{PHL} Set to output			30		7.0	

NOTE:

Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

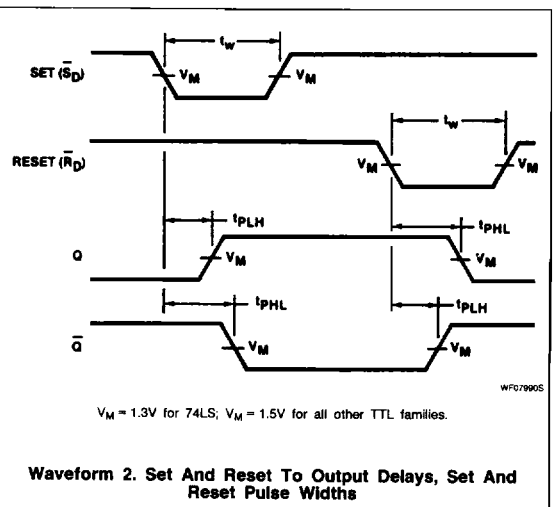
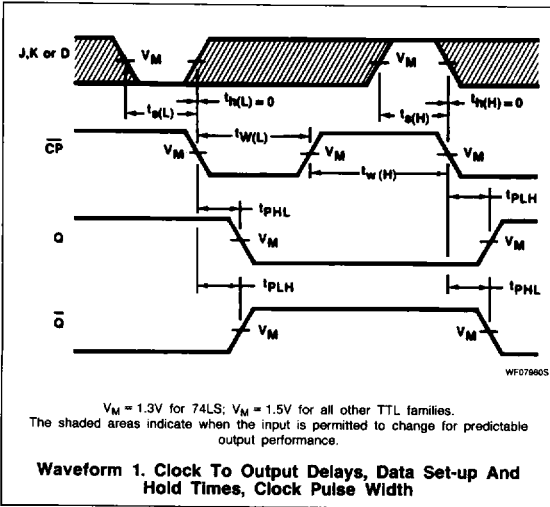
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AC SET-UP REQUIREMENTS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74LS		74S		UNIT
		Min	Max	Min	Max	
$t_{W(H)}$ Clock pulse width (HIGH)	Waveform 1	20		6.0		ns
$t_{W(L)}$ Clock pulse width (LOW)	Waveform 1	13		6.5		ns
$t_{W(L)}$ Set pulse width (LOW)	Waveform 2	25		8.0		ns
t_s Set-up time J or K to clock	Waveform 1	20		3.0		ns
t_h Hold time J or K to clock	Waveform 1	0		0		ns

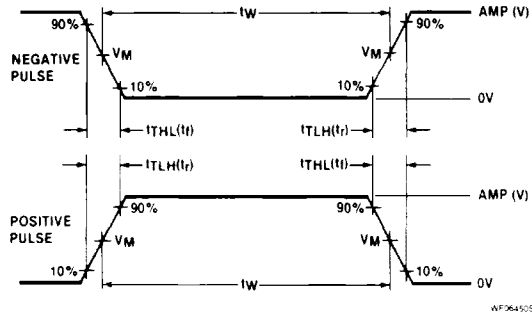
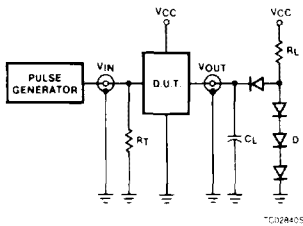
AC WAVEFORMS



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TEST CIRCUITS AND WAVEFORMS



$V_M = 1.3V$ for 74LS; $V_M = 1.5V$ for all other TTL families.

Test Circuit For 74 Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns