54AC/74AC646

Octal Transceiver/Register With 3-State Outputs

Description

The 'AC646 consists of registered bus transceiver circuits, with outputs, D-type flip-flops and control circuitry providing multiplexed transmission of data directly from the input bus or from the internal storage registers. Data on the A or B bus will be loaded into the respective registers on the LOW-to-HIGH transition of the appropriate clock pin (CAB or CBA). The four fundamental data handling functions available are illustrated in the following figures.

Real Time Transfer A-Bus to B-Bus

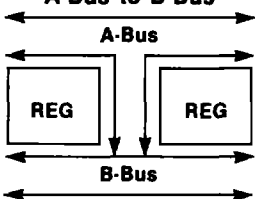


Figure 1

Real Time Transfer B-Bus to A-Bus

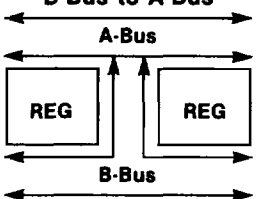


Figure 2

Storage from Bus to Register

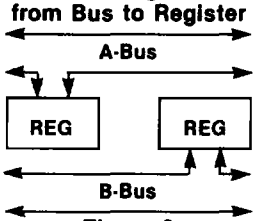


Figure 3

Transfer from Register to Bus

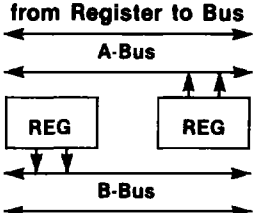
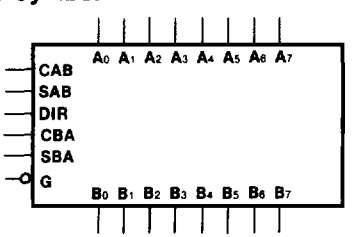


Figure 4

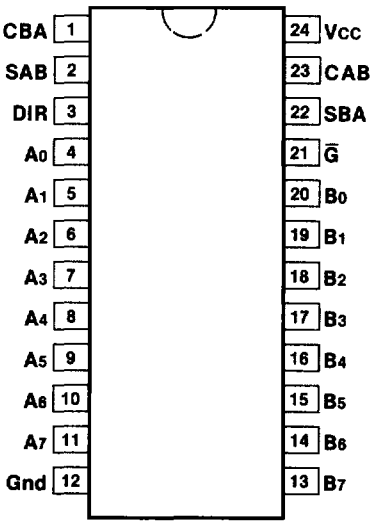
- **Independent Registers for A and B Buses**
- **Multiplexed Real-Time and Stored Data Transfers**
- **Choice of True and Inverting Data Paths**
- **3-State Outputs**
- **300 mil Slim Dual In-Line Package**
- **Outputs Source/Sink 24 mA**

Ordering Code: See Section 6

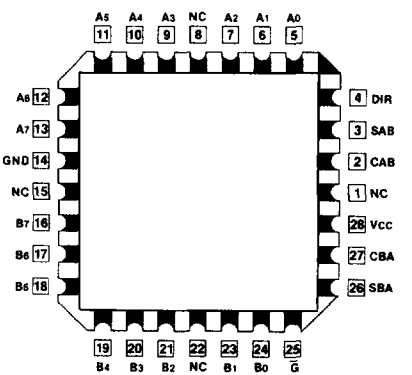
Logic Symbol



Connection Diagrams



Pin Assignment for DIP, Flatpak and SOIC



Pin Assignment for LCC

Pin Names

A_0 - A_7	Data Register Inputs Data Register A Outputs
B_0 - B_7	Data Register B Inputs Data Register B Outputs
CAB, CBA	Clock Pulse Inputs
SAB, SBA	Transmit/Receive Inputs
DIR, $\overline{G}$	Output Enable Inputs

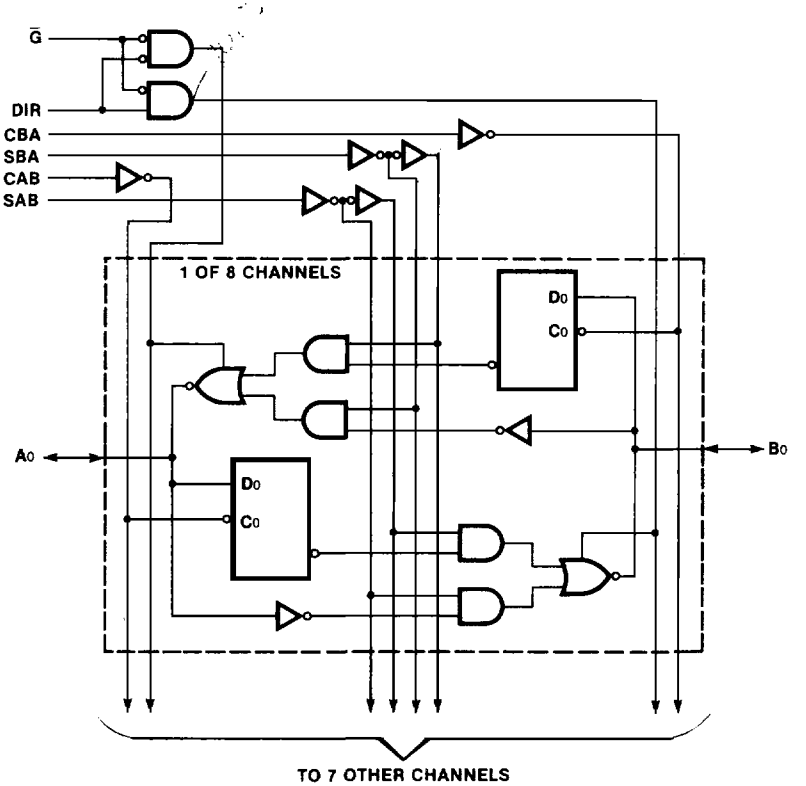
Function Table

Inputs						Data I/O*		Operation or Function
$\overline{G}$	DIR	CAB	CBA	SAB	SBA	A_0 - A_7	B_0 - B_7	
H	X	H or L	H or L	X	X	Input	Input	Isolation
H	X	⌐	⌐	X	X			Store A and B Data
L	L	X	X	X	L	Output	Input	Real Time B Data to A Bus
L	L	X	X	X	H			Stored B Data to A Bus
L	H	X	X	L	X	Input	Output	Real Time A Data to B Bus
L	H	H or L	X	H	X			Stored A Data to B Bus

*The data output functions may be enabled or disabled by various signals at the $\overline{G}$ and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every LOW-to-HIGH transition of the appropriate clock inputs.

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
⌐ = LOW-to-HIGH Transition

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics (unless otherwise specified)

Symbol	Parameter	54AC	74AC	Units	Conditions
I_{CC}	Maximum Quiescent Supply Current	160	80	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	8.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, $T_A = 25°C$

AC Characteristics

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay Clock to Bus	3.3	1.0	10.5	16.5	1.0	21.0	1.0	18.5	ns	3-6
		5.0	1.0	7.5	12.0	1.0	14.5	1.0	13.0		
t_{PHL}	Propagation Delay Clock to Bus	3.3	1.0	9.5	14.5	1.0	18.0	1.0	16.0	ns	3-6
		5.0	1.0	6.5	10.5	1.0	12.5	1.0	11.5		
t_{PLH}	Propagation Delay Bus to Bus	3.3	1.0	7.5	12.0	1.0	15.0	1.0	13.5	ns	3-5
		5.0	1.0	5.0	8.0	1.0	10.0	1.0	9.0		
t_{PHL}	Propagation Delay Bus to Bus	3.3	1.0	7.5	12.5	1.0	15.5	1.0	13.5	ns	3-5
		5.0	1.0	5.0	9.0	1.0	11.0	1.0	9.5		
t_{PLH}	Propagation Delay SBA or SAB to A_n or B_n (w/ A_n or B_n HIGH or LOW)	3.3	1.0	8.5	13.5	1.0	17.0	1.0	15.5	ns	3-6
		5.0	1.0	6.0	10.0	1.0	12.0	1.0	11.0		
t_{PHL}	Propagation Delay SBA or SAB to A_n or B_n (w/ A_n or B_n HIGH or LOW)	3.3	1.0	8.5	13.5	1.0	17.0	1.0	15.0	ns	3-6
		5.0	1.0	6.0	10.0	1.0	12.0	1.0	11.0		
t_{PZH}	Enable Time $\overline{G}$ to A_n or B_n	3.3	1.0	7.0	11.5	1.0	14.0	1.0	12.5	ns	3-7
		5.0	1.0	5.0	8.5	1.0	10.0	1.0	9.0		
t_{PZL}	Enable Time $\overline{G}$ to A_n or B_n	3.3	1.0	7.5	12.5	1.0	15.5	1.0	14.0	ns	3-8
		5.0	1.0	5.5	9.0	1.0	11.0	1.0	10.0		
t_{PHZ}	Disable Time $\overline{G}$ to A_n or B_n	3.3	1.0	8.0	12.5	1.0	14.5	1.0	13.5	ns	3-7
		5.0	1.0	6.5	10.0	1.0	12.0	1.0	11.0		
t_{PLZ}	Disable Time $\overline{G}$ to A_n or B_n	3.3	1.0	7.5	12.0	1.0	15.0	1.0	13.5	ns	3-8
		5.0	1.0	6.0	9.5	1.0	11.5	1.0	10.5		

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table 1 data sheet from your Fairchild sales engineer or account representative.

AC Characteristics, cont'd

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PZH}	Enable Time DIR to A_n or B_n	3.3	1.0	6.5	11.0	1.0	13.5	1.0	12.0	ns	3-7
		5.0	1.0	5.0	7.5	1.0	9.5	1.0	8.5		
t_{PZL}	Enable Time DIR to A_n or B_n	3.3	1.0	7.0	11.5	1.0	14.5	1.0	13.0	ns	3-8
		5.0	1.0	5.0	8.0	1.0	10.0	1.0	9.0		
t_{PHZ}	Disable Time DIR to A_n or B_n	3.3	1.0	7.5	11.5	1.0	13.5	1.0	12.5	ns	3-7
		5.0	1.0	5.5	9.5	1.0	10.5	1.0	10.0		
t_{PLZ}	Disable Time DIR to A_n or B_n	3.3	1.0	7.5	12.0	1.0	15.0	1.0	13.5	ns	3-8
		5.0	1.0	5.5	9.5	1.0	10.5	1.0	10.5		

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF		54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Set-up Time, HIGH or LOW Bus to Clock	3.3	2.0	5.0	6.0	5.5	ns	3-9
		5.0	1.5	4.0	4.5	4.5		
t_h	Hold time, HIGH or LOW Bus to Clock	3.3	−1.5	0	0.5	0	ns	3-9
		5.0	−0.5	0.5	1.0	1.0		
t_w	Clock Pulse Width HIGH or LOW	3.3	2.0	3.5	5.0	4.5	ns	3-6
		5.0	2.0	3.5	5.0	3.5		

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table 1 data sheet from your Fairchild sales engineer or account representative.

Capacitance

Symbol	Parameter	54/74AC Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.5$ V
$C_{I/O}$	Input/Output Capacitance	15.0	pF	$V_{CC} = 5.5$ V
C_{PD}	Power Dissipation Capacitance	60.0	pF	$V_{CC} = 5.5$ V