MOTOROLA

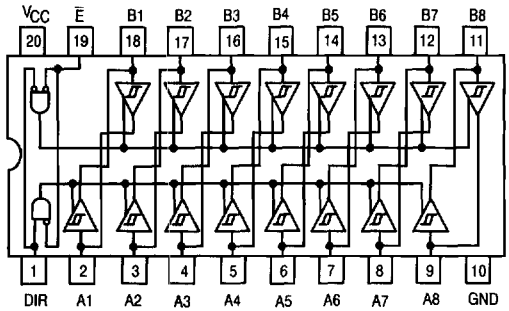
Octal Bus Transceivers With 3-State Outputs

ELECTRICALLY TESTED PER:
MIL-M-38510/32803

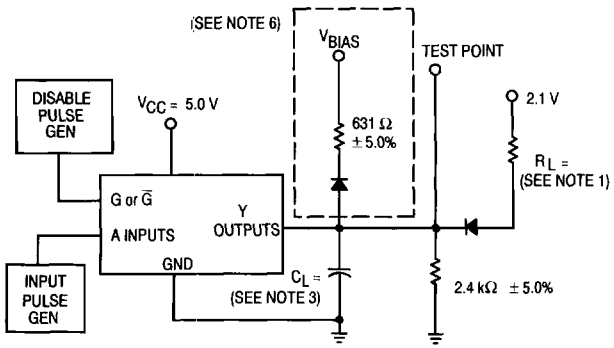
The 54LS245 is an Octal Bus Transmitter/Receiver designed for 8-line asynchronous 2-way data communication between data buses. Direction Input (DIR) controls transmission of Data from bus A to bus B or from bus B to bus A depending upon its logic level. The Enable ($\overline{E}$) can be used to isolate the buses.

- Hysteresis at Inputs to Improve Noise Immunity
- 2-Way Asynchronous Data Bus Communication
- Input Clamp Diodes Limit High-Speed Termination Effects

LOGIC DIAGRAM



AC TEST CIRCUIT



TRUTH TABLE

Inputs		Output
$\overline{E}$	DIR	
L	L	Bus B Data to Bus A
L	L	Bus A Data to Bus B
H	X	Isolation

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

REFERENCE NOTES ON PAGE 5-315

Military 54LS245

MPO

AVAILABLE AS:

1) JAN: JM38510/32803BXA
2) SMD: 8002101
3) 883: 54LS245/BXAJC

X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: R
CERFLAT: S
LCC: 2

THE LETTER "M" APPEARS BEFORE THE / ON LCC.

PIN ASSIGNMENTS

FUNCT.	DIL 732-03	FLATS 737-02	LCC 756A-02	BURN-IN (COND. A)
DIR	1	1	1	GND
A1	2	2	2	V_{CC}
A2	3	3	3	V_{CC}
A3	4	4	4	V_{CC}
A4	5	5	5	V_{CC}
A5	6	6	6	V_{CC}
A6	7	7	7	V_{CC}
A7	8	8	8	V_{CC}
A8	9	9	9	V_{CC}
GND	10	10	10	GND
B8	11	11	11	V_{CC}
B7	12	12	12	V_{CC}
B6	13	13	13	V_{CC}
B5	14	14	14	V_{CC}
B4	15	15	15	V_{CC}
B3	16	16	16	V_{CC}
B2	17	17	17	V_{CC}
B1	18	18	18	V_{CC}
$\overline{E}$	19	19	19	GND
V_{CC}	20	20	20	V_{CC}

BURN-IN CONDITIONS:
V_{CC} = 5.0 V MIN/6.0 V MAX

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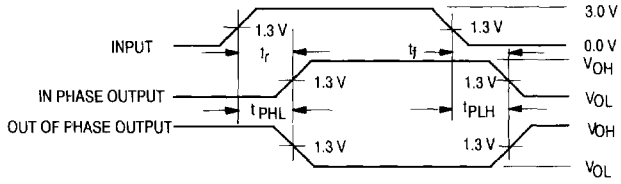
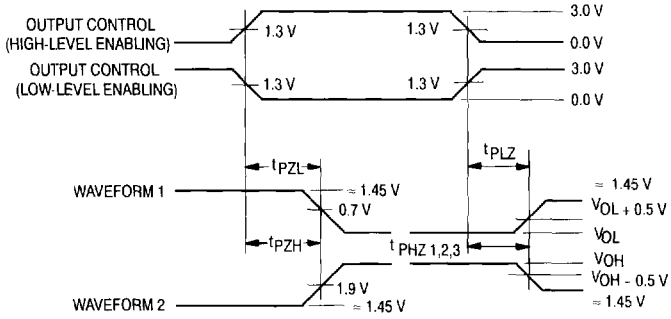
VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS



NOTES:

1. R_L = 110 Ω ± 5.0%.
2. All diodes are 1N3064 or equivalent.
3. C_L = 50 pF ± 10%, including scope probe, wiring and stray capacitance without package in text fixture.
4. The pulse generators have the following characteristics: V_{gen} = 3.0 V, PRR ≤ 1.0 MHZ, t_r ≤ 15 ns, t_f ≤ 6.0 ns, Z_{OUT}≈ 50 Ω.
5. Clock pulse characteristics: $t_{p(CLK)}$ = 20 ns, t_{setup} = 20 ns.
6. The diode and resistor shown within the dotted area are optional. When the diode and resistor are used, V_{BIAS} shall be 5.5 V for all tests except for t_{PHZ}; for t_{PHZ} tests, V_{BIAS} shall be − 0.6 V.
7. Voltage measurements are to be made with respect to network ground terminal.
8. Terminal conditions (pins not designated may be high ≥ 2.0 V, low ≤ 0.7 V, or open).

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Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
		+ 25°C		+ 125°C		− 55°C			
	Static Parameters:	Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V_{OH}	Logical "1" Output Voltage	2.4		2.4		2.4		V	V_{CC} = 4.5 V, I_{OH} = − 3.0 mA, V_{IH} = 2.0 V (other inputs are open), DIR = 2.0 V or 0.7 V, $\overline{E}$ = 0.7 V.
V_{OL}	Logical "0" Output Voltage		0.4		0.4		0.4	V	V_{CC} = 4.5 V, I_{OH} = 12 mA, V_{IL} = 0.7 V (other inputs are open), DIR = 2.0 V or 0.7 V, $\overline{E}$ = 0.7 V.
V_{OH1}	Logical "1" Output Voltage	2.0		2.0		2.0		V	V_{CC} = 4.5 V, I_{OH} = − 12 mA, V_{IH} = 2.0 V (other inputs are open), DIR = 2.0 V or 0.7 V, $\overline{E}$ = 0.7 V.
V_{IC}	Input Clamping Voltage		− 1.5					V	V_{CC} = 4.5 V, I_{IN} = −18 mA, $\overline{E}$ = open, 5.5 V or (−18 mA), all other inputs are open.
I_{IH}	Logical "1" Input Current		20		20		20	µA	V_{CC} = 5.5 V, V_{IH}= 2.7 V, $\overline{E}$ = GND or (2.7 V), other inputs are open.
I_{IHH}	Logical "1" Input Current		100		100		100	µA	V_{CC} = 5.5 V, V_{IHH} = 5.5 V, $\overline{E}$ = GND or (5.5 V), other inputs are open.
I_{IL}	Logical "0" Input Current	− 5.0	− 240	− 5.0	240	− 5.0	− 240	µA	V_{CC} = 5.5 V, $\overline{E}$ = GND or (0.4 V), DIR = 0.4 V, 4.5 V or GND, other inputs are open.
I_{OSH}	Output Short Circuit Current	− 40	− 225	− 40	− 225	− 40	− 225	mA	V_{CC} = 5.5 V, V_{IN} = 5.5 V (other inputs are GND), V_{OUT} = GND, $\overline{E}$ = GND.
I_{IOZH}	Output Off Current High		20		20		20	µA	V_{CC} = 5.5 V, V_{IH} = 2.7 V, other inputs are open, $\overline{E}$ = 2.0 V, DIR = open.
I_{IOZL}	Output Off Current Low		− 200		− 200		− 200	mA	V_{CC} = 5.5 V, V_{IL} = 0.4 V, $\overline{E}$ = 2.0 V, other inputs are open.
I_{CCH}	Power Supply Current		70		70		70	mA	V_{CC} = 5.5 V, V_{IN} = 5.5 V (all inputs), DIR = GND.
I_{CCL}	Power Supply Current		90		90		90	mA	V_{CC} = 5.5 V, V_{IN} = GND (all inputs)
I_{CCZ}	Power Supply Current Off		95		95		95	mA	V_{CC} = 5.5 V, all inputs are open, $\overline{E}$ = 5.5 V.
V_{IH}	Logical "1" Input Voltage	2.0		2.0		2.0		V	V_{CC} = 4.5 V.
V_{IL}	Logical "0" Input Voltage		0.7		0.7		0.7	V	V_{CC} = 4.5 V.
	Functional Tests	Subgroup 7		Subgroup 8A		Subgroup 8B			per Truth Table with V_{CC} = 5.0 V, V_{INL} = 0.4 V, and V_{INH} = 2.5 V.

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Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Switching Parameters:	+ 25°C		+ 125°C		− 55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t_{PHL} t_{PHL}	Propagation Delay Data to Output	2.0 —	17 12	2.0 —	22 17	2.0 —	22 17	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 110 Ω. V_{CC} = 5.0 V, C_L = 45 pF, R_L = 667 Ω.
t_{PLH} t_{PLH}	Propagation Delay Data to Output	2.0 —	17 12	2.0 —	22 17	2.0 —	22 17	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 110 Ω. V_{CC} = 5.0 V, C_L = 45 pF, R_L = 667 Ω.
t_{PLZ} t_{PLZ}	Propagation Delay Output Disable Time from LOW Level	2.0 —	30 25	2.0 —	39 34	2.0 —	39 34	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 110 Ω. V_{CC} = 5.0 V, C_L = 45 pF, R_L = 667 Ω.
t_{PHZ} t_{PHZ}	Propagation Delay Output Disable Time from HIGH Level	2.0 —	30 25	2.0 —	39 34	2.0 —	39 34	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 110 Ω. V_{CC} = 5.0 V, C_L = 45 pF, R_L = 667 Ω.
t_{PZL} t_{PZL}	Propagation Delay Output Enable Time from LOW Level	2.0 —	45 40	2.0 —	58 53	2.0 —	58 53	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 110 Ω. V_{CC} = 5.0 V, C_L = 45 pF, R_L = 667 Ω.
t_{PZH} t_{PZH}	Propagation Delay Output Enable Time from HIGH Level	2.0 —	45 40	2.0 —	58 53	2.0 —	58 53	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 110 Ω. V_{CC} = 5.0 V, C_L = 45 pF, R_L = 667 Ω.