Integrated Device Technology, Inc.

MULTILEVEL PIPELINE REGISTERS

PRELIMINARY
IDT 29FCT520A/B
IDT 29FCT521A/B

FEATURES:

- Equivalent to AMD's Am29520/21 bipolar Multilevel Pipeline Registers in pinout/function, speeds and output drive over full temperature and voltage supply extremes
- Four 8-bit high-speed registers
- Dual two-level or single four-level push-only stack operation
- All registers available at multiplexed output
- Hold, transfer and load instructions
- Provides temporary address or data storage
- I_{OL} = 48mA (commercial), 32mA (military)
- CMOS power levels (5μW typ. static)
- Substantially lower input current levels than AMD's bipolar (5μA typ.)
- TTL input and output level compatible
- CMOS output level compatible
- Manufactured using advanced CEMOS™ processing
- Available in 300 mil plastic and hermetic DIP, as well as LCC, SOIC and CERPACK
- Product available in Radiation Tolerant and Enhanced versions
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

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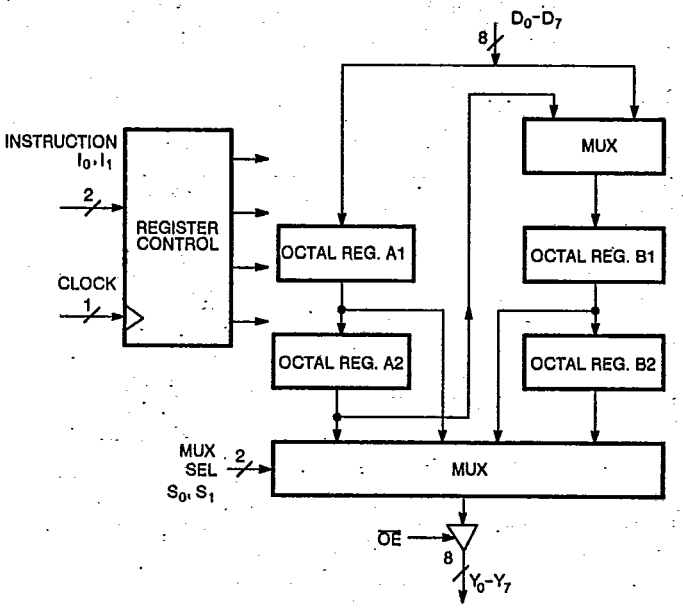
The IDT29FCT520A/B and IDT29FCT521A/B each contain four 8-bit positive edge-triggered registers. These may be operated as a dual 2-level or as a single 4-level pipeline. A single 8-bit input is provided and any of the four registers is available at the 8-bit, 3-state output.

These devices differ only in the way data is loaded into and between the registers in 2-level operation. The difference is illustrated in Figure 1. In the IDT29FCT520A/B when data is entered into the first level (I = 2 or I = 1), the existing data in the first level is moved to the second level. In the IDT29FCT521A/B, these instructions simply cause the data in the first level to be overwritten. Transfer of data to the second level is achieved using the 4-level shift instruction (I = 0). Transfer also causes the first level to change. In either part I = 3 is for hold.

FUNCTIONAL BLOCK DIAGRAM



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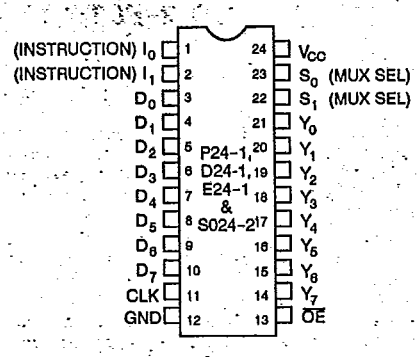
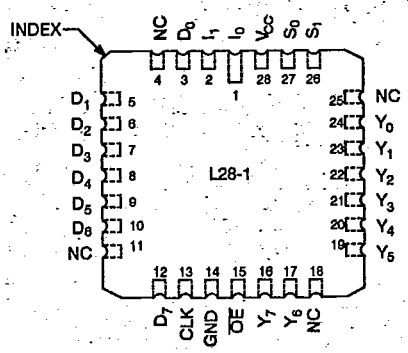
PIN CONFIGURATIONS



DIP/CERPACK/SOIC
TOP VIEW



LCC
TOP VIEW

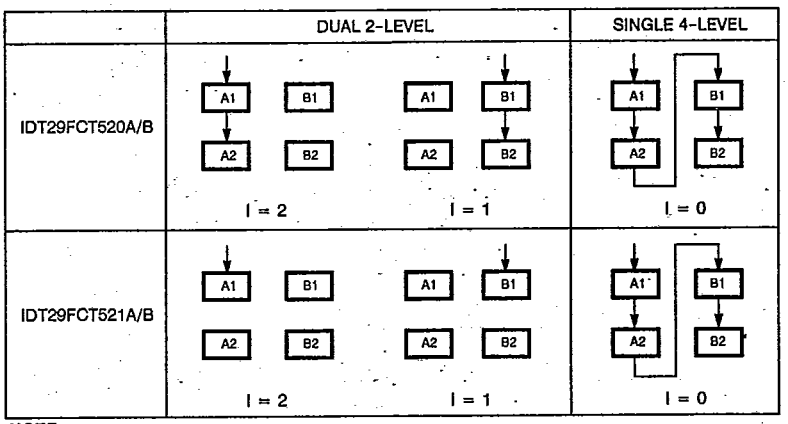
PIN DESCRIPTION

PIN NO.(1)	NAME	I/O	DESCRIPTION
3-10	D_0 - D_7	I	Register input port.
11	CLK	I	Clock input. Enter data into registers on LOW-to-HIGH transitions.
1, 2	I_0, I_1	I	Instruction inputs. See Figure 1 and Instruction Control Tables.
23, 22	S_0, S_1	I	Multiplexer select. Inputs either register A_1, A_2, B_1 or B_2 data to be available at the output port.
13	$\overline{OE}$	I	Output enable for 3-state output port.
14-21	Y_7 - Y_0	O	Register output port

NOTE:
1. DIP configuration.

REGISTER SELECTION

S_1	S_0	Register
0	0	B_2
0	1	B_1
1	0	A_2
1	1	A_1



NOTE:
1. I = 3 for hold.

Figure 1. Data Loading in 2-Level Operation

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ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	100	100	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V
Commercial: T_A = 0°C to +70°C; V_{CC} = 5.0V±5%
Military: T_A = -55°C to +125°C; V_{CC} = 5.0V±10%

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		–	–	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = V_{CC}	–	–	5	µA
			V_I = 2.7V	–	–	5(4)	
I_{IL}	Input LOW Current		V_I = 0.5V	–	–	-5(4)	
			V_I = GND	–	–	-5	
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = V_{CC}	–	–	10	µA
			V_O = 2.7V	–	–	10(4)	
			V_O = 0.5V	–	–	-10(4)	
			V_O = GND	–	–	-10	
I_{OS}	Short Circuit Current	V_{CC} = Max.(3), V_O = GND		-60	-120	–	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	–	
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	–	V
			I_{OH} = -12mA MIL.	2.4	4.3	–	
			I_{OH} = -15mA COM'L.	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		–	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	–	GND	V_{LC}	
			I_{OL} = 32mA MIL.	–	0.3	0.5	
			I_{OL} = 48mA COM'L.	–	0.3	0.5	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

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POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} – 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS (1)		MIN.	TYP.(2)	MAX.	UNIT
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ $f_{CP} = f_i = 0$		–	0.001	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V(3)		–	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current(4)	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	–	0.15	0.25	mA/MHz
I_C	Total Power Supply Current (6)	V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{OE}$ = GND One Bit Toggling at f_i = 5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	2.3	4	mA
			V_{IN} = 3.4V or V_{IN} = GND	–	2.8	6	
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{OE}$ = GND Eight Bits and Four Controls Toggling at f_i = 5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	9.8	17.8(5)	
			V_{IN} = 3.4V or V_{IN} = GND	–	13.0	30.8(5)	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

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SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITIONS[1]	IDT29FCT520A/21A					IDT29FCT520B/21B[4]					UNIT
			TYP[3]	COM'L.		MIL.		TYP[3]	COM'L.		MIL.		
				MIN.[2]	MAX.	MIN.[2]	MAX.		MIN.[2]	MAX.	MIN.[2]	MAX.	
t_{PHL} t_{PLH}	Clock to Data Output	R_L = 500Ω C_L = 50pF	7.0	2.0	14.0	2.0	16.0	–	2.0	7.5	2.0	8.0	ns
t_{PHL} t_{PLH}	S_0, S_1 to Data Output		7.0	2.0	13.0	2.0	15.0	–	2.0	7.5	2.0	8.0	ns
t_{SU}	Set-up Time Input Data to Clock		–	5.0	–	6.0	–	–	2.5	–	2.5	–	ns
t_H	Hold Time Input Data to Clock		–	2.0	–	2.0	–	–	2.0	–	2.0	–	ns
t_{SU}	Set-up Time Instruction to Clock		–	5.0	–	6.0	–	–	4.0	–	4.5	–	ns
t_H	Hold Time Instruction to Clock		–	2.0	–	2.0	–	–	2.0	–	2.0	–	ns
t_{PHZ} t_{PLZ}	Output Disable Time		6.0	1.5	12.0	1.5	13.0	–	1.5	7.0	1.5	7.5	ns
t_{PZH} t_{PZL}	Output Enable Time		9.0	1.5	15.0	1.5	16.0	–	1.5	7.5	1.5	8.0	ns
t_W	Clock Pulse Width HIGH or LOW	–	4.0	7.0	–	8.0	–	–	5.5	–	6.0	–	ns

NOTES:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
4. Preliminary information only.

As companies like IDT continue to integrate more onto each device and put each device into smaller packages such as surface mount devices, the board level testing becomes more complex for the designer and the manufacturing divisions of companies. To help this situation, serial diagnostics was invented. This allows for observation of critical signals deep within the system. During system test, when an error is observed, these signals may be modified in order to zero in on the fault in the system.

Serial diagnostics is primarily a scheme utilizing only a few pins (4) to examine and alter the internal state of a system for the purpose of monitoring and diagnosing system faults. It can be used at many points in the life of a product: design debug and verification, manufacturing test and field service. This document describes a serial diagnostic scheme which was developed at IDT and will be used in future VLSI logic devices designed by IDT.

CMOS TESTING CONSIDERATIONS

Special test board considerations must be taken into account when applying high-speed CMOS products to the automatic test environment. Large output currents are being switched in very short periods and proper testing demands that test set-ups have minimized inductance and guaranteed zero voltage grounds. The techniques listed below will assist the user in obtaining accurate testing results:

1) All input pins should be connected to a voltage potential during testing. If left floating, the device may oscillate, causing improper device operation and possible latchup.
2) Placement and value of decoupling capacitors is critical. Each physical set-up has different electrical characteristics and it is recommended that various decoupling capacitor sizes be experimented with. Capacitors should be positioned using the minimum lead lengths. They should also be distributed to decouple power supply lines and be placed as close as possible to the DUT power pins.
3) Device grounding is extremely critical for proper device testing. The use of multi-layer performance boards with radial decoupling between power and ground planes is necessary. The ground plane must be sustained from the performance board to the DUT interface board and wiring unused interconnect pins to the ground plane is recommended. Heavy gauge stranded wire should be used for power wiring, with twisted pairs being recommended for minimized inductance.
4) To guarantee data sheet compliance, the input thresholds should be tested per input pin in a static environment. To allow for testing and hardware-induced noise, it may be necessary to use $V_{IL} \leq 0V$ and $V_{IH} \geq 3V$ for ATE testing purposes.

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ORDERING INFORMATION