Hex "D" Master-Slave Flip-Flop with Reset

ELECTRICALLY TESTED PER: 5962-8756301

The 10H586 is a hex D type flip-flop with common reset and clock lines. This MECL 10H part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in clock toggle frequency and propagation delay and no increase in power supply current.

- Propagation Delay, 1.7 ns Typical
- 660 mW Max/Pkg (No Load)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

	PIN ASSIGNMENTS			
FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V_{CC1}	1	5	2	GND
Q_0	2	6	3	51 Ω to V_{TT}
Q_1	3	7	4	51 Ω to V_{TT}
Q_2	4	8	5	51 Ω to V_{TT}
D0	5	9	7	GND
D_1	6	10	8	GND
D_2	7	11	9	GND
V_{EE}	8	12	10	V_{EE}
Clock	9	13	12	CP1
D_3	10	14	13	GND
D_4	11	15	14	GND
D_5	12	16	15	GND
Q_3	13	1	17	51 Ω to V_{TT}
Q_4	14	2	18	51 Ω to V_{TT}
Q_5	15	3	19	51 Ω to V_{TT}
V_{CC2}	16	4	20	GND

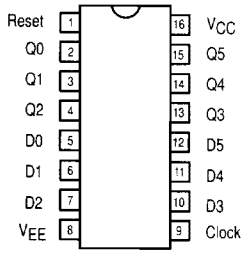
BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN

AVAILABLE AS

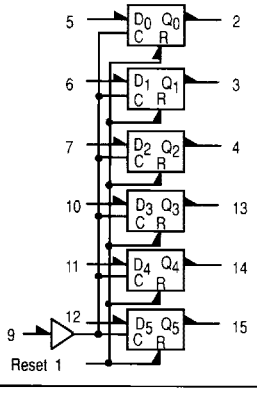
1) JAN: N/A
2) SMD: 5962-8756301
3) 883: 10H586/BXAJC
X = CASE OUTLINE AS FOLLOWS:

PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.

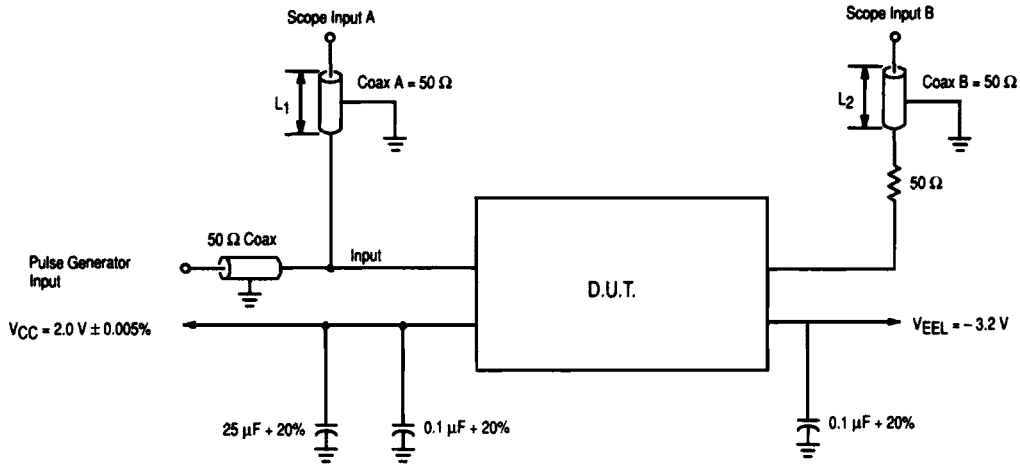


LOGIC DIAGRAM

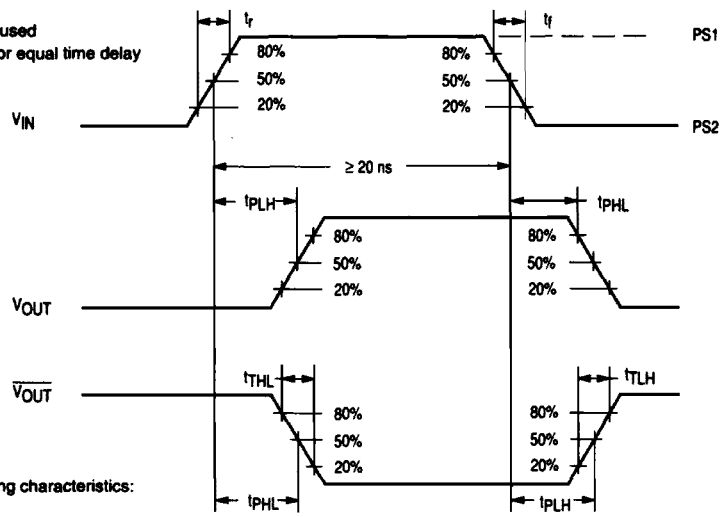


CLOCKED TRUTH TABLE			
R	C	Q	$Q_n + 1$
L	L	Ø	Q_n
L	H*	L	L
L	H*	H	H
H	L	Ø	L

Ø = Don't Care
* A clock H is a clock transition from a low to a high state



NOTES
1. Pulse generator must be capable of rise and fall time of 1.0 ns ± 0.1 ns
2. Unused outputs connected to 100 Ω resistor to ground
3. 2:1 divider may be used
4. L1 = L2: matched for equal time delay



NOTES
1. V_{IN} has the following characteristics:
   a) PW ≥ 20 ns
   b) f = 1.0 MHz

Figure 1. Switching Test Circuit and Waveforms

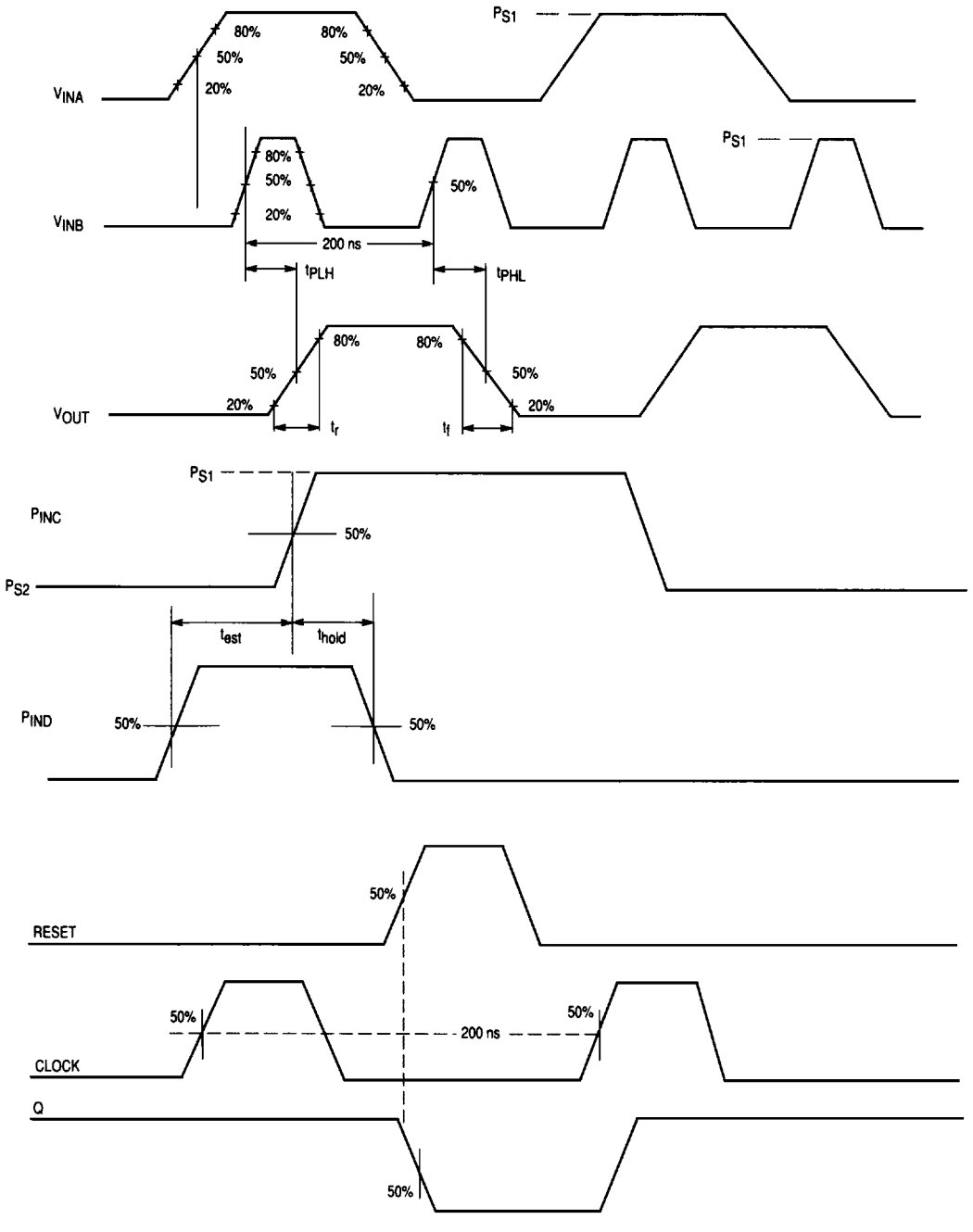


Figure 2. Switching Test Circuit and Waveforms

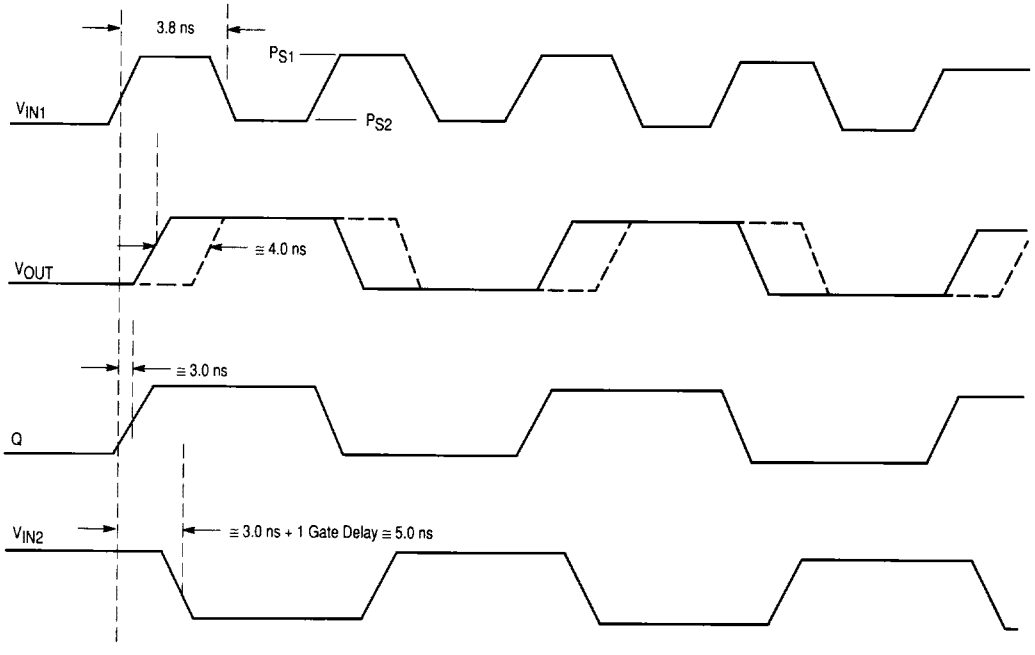


Figure 3. t_{TOGGLE} Waveforms

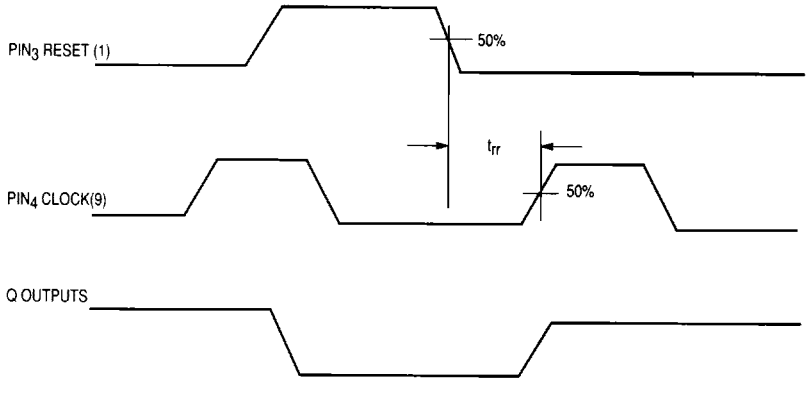


Figure 4. t_{rr} Waveforms

10H586
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)								
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	P_{S1}	P_{S2}	V_{EE1}	V_{EE2}	V_{EEL}
T_A = 25 °C	-0.78	-1.95	-1.11	-1.480	+1.11	+0.31	-5.46	-4.94	-2.94
T_A = 125 °C	-0.65	-1.95	-0.96	-1.465	+1.24	+0.36	-5.46	-4.94	-2.94
T_A = -55 °C	-0.84	-1.95	-1.16	-1.510	+1.01	+0.28	-5.46	-4.94	-2.94

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW							
	Functional Parameters:	+ 25 °C		+ 125 °C		– 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to – 2.0 V							
		Subgroup 1		Subgroup 2		Subgroup 3										
		Min	Max	Min	Max	Min	Max		V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	V_{EE1}	V_{EE2}	V_{CC}	P. U. T.
V_{OH}	High Output Voltage	– 1.01	– 0.78	– 0.86	– 0.65	– 1.06	– 0.84	V	5 - 7 9 - 12	5 - 7 9 - 12			8		16	2 - 4, 13 - 15
V_{OL}	Low Output Voltage	– 1.95	– 1.58	– 1.95	– 1.565	– 1.95	– 1.61	V	5 - 7 9 - 12	5 - 7 9 - 12			8		16	2 - 4, 13 - 15
V_{OH1}	High Output Voltage	– 1.01	– 0.78	– 0.86	– 0.65	– 1.06	– 0.84	V	5 - 7 9 - 12	1, 5 - 7 10 - 12	5 - 7, 10 - 12	1	8	8	16	2 - 4, 13 - 15
V_{OL1}	Low Output Voltage	– 1.95	– 1.58	– 1.95	– 1.565	– 1.95	– 1.61	V	5 - 7 10 - 12	1, 5 - 7 9 - 12	1	5 - 7, 10 - 12	8	8	16	2 - 4, 13 - 15
I_{EE}	Power Supply Current	– 110		– 121		– 121		mA					8		16	8
I_{IH}	Input Current High		420		670		670	µA	9				8		16	9
I_{IH1}	Input Current High		265		430		430	µA	5 - 7 10 - 12				8		16	5 - 7, 10 - 12
I_{IH2}	Input Current High		1200		1900		1900	µA	1				8		16	1
I_{IL}	Input Current Low	0.5		0.3		0.5		µA		1, 5 - 7 9 - 12				8	16	1, 5 - 7, 9 - 12

NOTES

1. Hold power during all V_{OH} and V_{OL} tests.
2. P1) V_{IH}, V_{IL} P2) V_{IH}, V_{IH2} P3) V_{IH}, V_{IL2}

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	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	P_{S1}	P_{S2}	V_{EE1}	V_{EE2}	V_{EEL}
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Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW					
	Functional Parameters:	+ 25 °C		+ 125 °C		– 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND					
		Subgroup 9		Subgroup 10		Subgroup 11								
		Min	Max	Min	Max	Min	Max		P_{S1}	V_{IN}	V_{OUT}	V_{CC}	V_{EEL}	P. U. T.
t_{TLH}	Rise Time	0.7	2.4	0.7	2.6	0.7	2.6	ns		5 - 7, 9 - 12	2 - 4, 13 - 15	16	8	2 - 4, 13 - 15
t_{THL}	Fall Time	0.7	2.4	0.7	2.6	0.7	2.6	ns		5 - 7, 9 - 12	2 - 4, 13 - 15	16	8	2 - 4, 13 - 15
t_{PLH}	Propagation Delay Clk or Reset to Q	0.7	2.7	0.7	3.0	0.7	3.0	ns	5 - 7 10 - 12	5 - 7, 9 - 12	2 - 4, 13 - 15	16	8	2 - 4, 13 - 15
t_{PLH}	Propagation Delay Clk or Reset to Q	0.7	2.7	0.7	3.0	0.7	3.0	ns	5 - 7 10 - 12	5 - 7, 9 - 12	2 - 4, 13 - 15	16	8	2 - 4, 13 - 15
t_{SET}	Setup Time	1.5		1.5		1.5		ns		5 - 7, 9 - 12	2 - 4, 13 - 15	16	8	2 - 4, 13 - 15
t_{HOLD}	Hold Time	1.0		1.0		1.0		ns		5 - 7, 9 - 12	2 - 4, 13 - 15	16	8	2 - 4, 13 - 15
t_{RR}	Reset Recovery Time	3.0		3.0		3.0		ns	5 - 7 10 - 12	9	2 - 4, 13 - 15	16	8	2 - 4, 13 - 15
f_{TOGGLE}	Toggle Frequency	250		250		250		MHz		5 - 7, 9 - 12	2 - 4, 13 - 15	16	8	2 - 4, 13 - 15