UM621024B Series

128K X 8 CMOS SRAM

Features

- Single +5V power supply
- Access times: 55/70 ns (max.)
- Current:
  - Low power version: Operating: 70mA (max.)
    Standby: 100 μA (max.)
  - Very low power version: Operating: 70mA (max.)
    Standby: 25 μA (max.)
- Full static operation, no clock or refreshing required
- Directly TTL compatible: All inputs and outputs
- Common I/O using three-state output
- Output enable and two chip enable inputs for easy application
- Data retention voltage: 2V (min.)
- Available in 32-pin DIP, SOP or TSOP packages

General Description

The UM621024B is a low operating current 1,048,576-bit static random access memory organized as 131,072 words by 8 bits and operates on a single 5V power supply. It is built using UMC's high performance CMOS process.

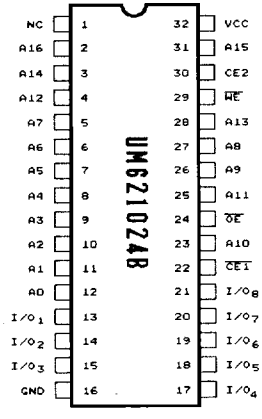
Inputs and three-state outputs are TTL compatible and allow for direct interfacing with common system bus structures.

Two chip enable inputs are provided for power down and device enable and an output enable input is included for easy interfacing.

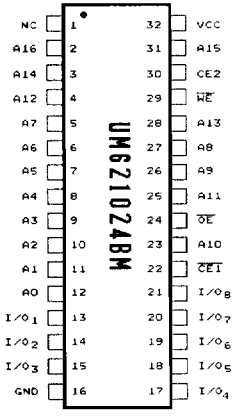
Data retention is guaranteed at a power supply voltage as low as 2V.

Pin Configurations

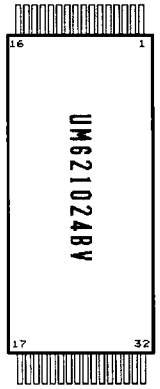
■ DIP



■ SOP



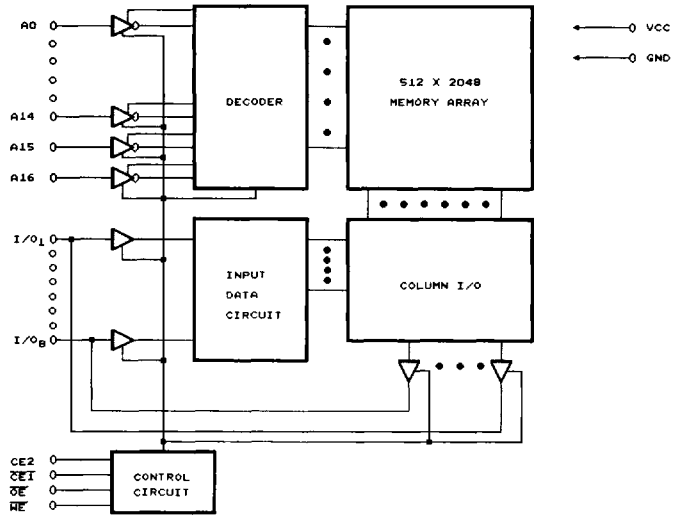
■ TSOP (forward type)



(reverse type)

Pin No.	1	2	3	4	5	6	7	8	9	10	11
Pin Name	A11	A9	A8	A13	$\overline{WE}$	CE2	A15	VCC	NC	A16	A14
Pin No.	12	13	14	15	16	17	18	19	20	21	22
Pin Name	A12	A7	A6	A5	A4	A3	A2	A1	A0	I/O1	I/O2
Pin No.	23	24	25	26	27	28	29	30	31	32	
Pin Name	I/O3	GND	I/O4	I/O5	I/O6	I/O7	I/O8	$\overline{CE1}$	A10	$\overline{OE}$	

Block Diagram



Pin Descriptions — DIP/SOP

Pin No.	Symbol	Description
2 - 12, 23, 25 - 28, 31	A0 - A16	Address Input
29	$\overline{WE}$	Write Enable
24	$\overline{OE}$	Output Enable
22	$\overline{CE1}$	Chip Enable
30	CE2	Chip Enable
1	NC	No Connection
13-15, 17-21	I/O1 - I/O8	Data Input/Output
32	VCC	Power Supply (+5V)
16	GND	Ground

Pin Description — TSOP

Pin No.	Symbol	Description
1 - 4, 7, 10 - 20, 31	A0 - A16	Address Input
5	$\overline{WE}$	Write Enable
32	$\overline{OE}$	Output Enable
30	$\overline{CE1}$	Chip Enable
6	CE2	Chip Enable
9	NC	No Connection
21-23, 25-29	I/O1 - I/O8	Data Input/Output
8	VCC	Power Supply
24	GND	Ground

Recommended DC Operating Conditions

(T_A = 0°C to + 70°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	4.5	5.0	5.5	V
GND	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.2	3.5	VCC + 0.3	V
V_{IL}	Input Low Voltage	-0.3	0	+0.8	V
C_L	Output Load	-	-	30	pF
TTL	Output Load	-	-	1	-

Absolute Maximum Ratings*

VCC to GND . . . . . -0.5V to +7.0V
IN, IN/OUT Volt to GND . . . . . -0.5V to VCC + 0.5V
Operating Temperature, Topr . . . . . 0°C to +70°C
Storage Temperature, Tstg . . . . . -55°C to +125°C
Temperature Under Bias, Tbias . . . . . -10°C to +85°C
Power Dissipation, P_T 0.7W
Soldering Temp. & Time . . . . . 260°C, 10 sec

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (T_A = 0°C to + 70°C, VCC = 5V ± 10%, GND = 0V)

Symbol	Parameter	UM621024B-55L/70L		UM621024B-55LL/70LL		Unit	Conditions
		Min.	Max.	Min.	Max.		
$\|I_{LI}\|$	Input Leakage Current	–	1	–	1	μA	V_{IN} = GND to VCC
$\|I_{LO}\|$	Output Leakage Current	–	1	–	1	μA	$\overline{CE1}$ = V_{IH} or CE2 = V_{IL} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL} $V_{I/O}$ = GND to VCC
I_{CC}	Active Power Supply Current	–	15	–	15	mA	$\overline{CE1}$ = V_{IL}, CE2 = V_{IH} $I_{I/O}$ = 0 mA

DC Electrical Characteristics (continued)

Symbol	Parameter	UM621024B-55L/70L		UM621024B-55LL/70LL		Unit	Conditions
		Min.	Max.	Min.	Max.		
I_{CC1}	Dynamic Operating Current	–	70	–	70	mA	Min. Cycle, Duty = 100% $\overline{CE1}$ = V_{IL}, CE2 = V_{IH} $I_{I/O}$ = 0 mA
I_{CC2}		–	15	–	15	mA	$\overline{CE1}$ = V_{IL}, CE2 = V_{IH} V_{IH} = VCC, V_{IL} = 0V f = 1 MHz, $I_{I/O}$ = 0 mA
I_{SB}	Standby Power Supply Current	–	3	–	2	mA	$\overline{CE1}$ = V_{IH} or CE2 = V_{IL}
I_{SB1}		–	100	–	25	μA	$\overline{CE1}$ ≥ VCC - 0.2V CE2 ≥ VCC - 0.2V V_{IN} ≥ 0V
I_{SB2}		–	100	–	25	μA	CE2 ≤ 0.2V V_{IN} ≥ 0V
V_{OL}	Output Low Voltage	–	0.4	–	0.4	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage	2.4	–	2.4	–	V	I_{OH} = -1.0 mA

Truth Table

Mode	$\overline{CE1}$	CE2	$\overline{OE}$	$\overline{WE}$	I/O Operation	Supply Current
Standby	H	X	X	X	High Z	I_{SB}, I_{SB1}
	X	L	X	X	High Z	I_{SB}, I_{SB2}
Output Disabled	L	H	H	H	High Z	I_{CC}, I_{CC1}, I_{CC2}
Read	L	H	L	H	D_{OUT}	I_{CC}, I_{CC1}, I_{CC2}
Write	L	H	X	L	D_{IN}	I_{CC}, I_{CC1}, I_{CC2}

Note: X: H or L

Capacitance (T_A = 25°C, f = 1.0 MHz)

Symbol	Parameter	Min.	Max.	Unit	Conditions
C_{IN}*	Input Capacitance		6	pF	V_{IN} = 0V
$C_{I/O}$*	Input/Output Capacitance		8	pF	$V_{I/O}$ = 0V

* These parameters are sampled and not 100% tested.

AC Characteristics (TA = 0°C to +70°C, VCC = 5V ± 10%)

Symbol	Parameter		UM621024B-55L/LL		UM621024B-70L/LL		Unit
			Min.	Max.	Min.	Max.	
Read Cycle							
t_{RC}	Read Cycle Time		55	–	70	–	ns
t_{AA}	Address Access Time		–	55	–	70	ns
t_{ACE1}	Chip Enable Access Time	$\overline{CE1}$	–	55	–	70	ns
t_{ACE2}		CE2	–	55	–	70	ns
t_{OE}	Output Enable to Output Valid		–	30	–	35	ns
t_{CLZ1}	Chip Enable to Output in Low Z	$\overline{CE1}$	10	–	10	–	ns
t_{CLZ2}		CE2	10	–	10	–	ns
t_{OLZ}	Output Enable to Output in Low Z		5	–	5	–	ns
t_{CHZ1}	Chip Disable to Output in High Z	$\overline{CE1}$	0	20	0	25	ns
t_{CHZ2}		CE2	0	20	0	25	ns
t_{OHZ}	Output Disable to Output in High Z		0	20	0	25	ns
t_{OH}	Output Hold from Address Change		5	–	5	–	ns
Write Cycle							
t_{WC}	Write Cycle Time		55	–	70	–	ns
t_{CW}	Chip Enable to End of Write		50	–	60	–	ns
t_{AS}	Address Setup Time		0	–	0	–	ns
t_{AW}	Address Valid to End of Write		50	–	60	–	ns

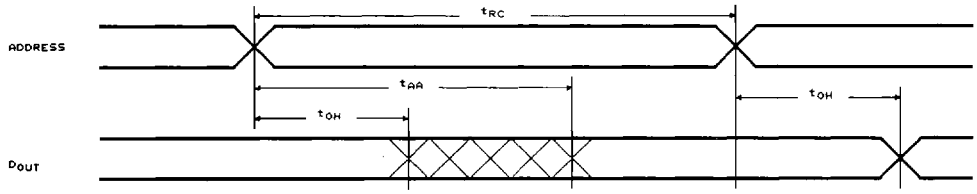
AC Characteristics (continued)

Symbol	Parameter	UM621024B-55L/LL		UM621024B-70L/LL		Unit
		Min.	Max.	Min.	Max.	
t_{WP}	Write Pulse Width	40	–	50	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	ns
t_{WHZ}	Write to Output in High Z	0	25	0	30	ns
t_{DW}	Data to Write Time Overlap	25	–	30	–	ns
t_{DH}	Data Hold from Write Time	0	–	0	–	ns
t_{OW}	Output Active from End of Write	5	–	5	–	ns

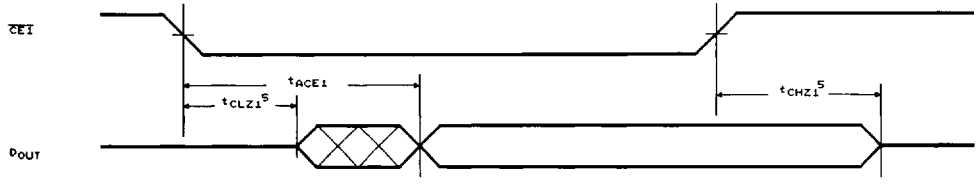
Notes: t_{CHZ1}, t_{CHZ2} and t_{OHZ} and t_{WHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.

Timing Waveforms

Read Cycle 1 (1, 2, 4)

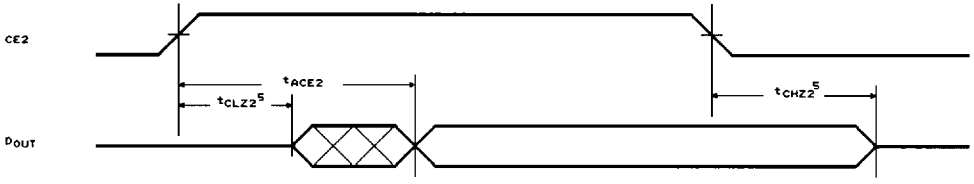


Read Cycle 2 (1, 3, 4, 6)

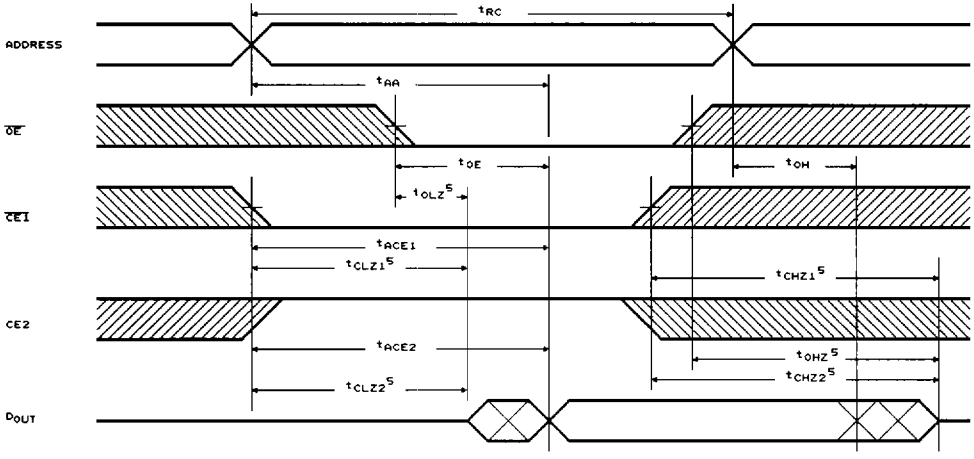


Timing Waveforms (continued)

Read Cycle 3 (1, 4, 7, 8)



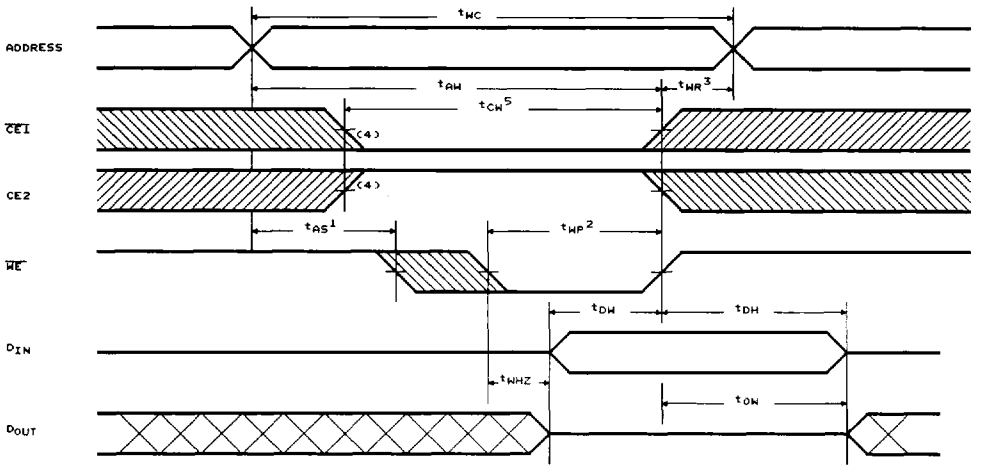
Read Cycle 4 (1)



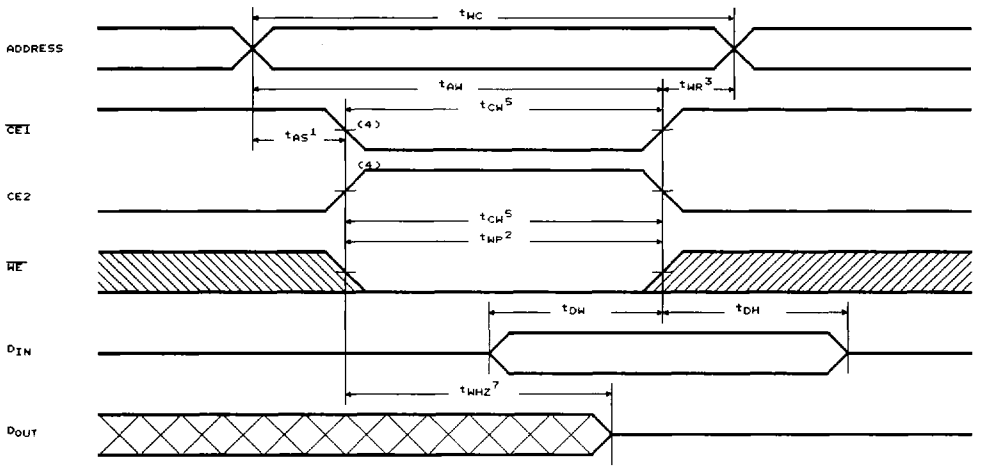
Notes: 1. $\overline{WE}$ is high for Read Cycle.
2. Device is continuously enabled $\overline{CE1}$ = VIL and CE2 = VIH.
3. Address valid prior to or coincident with $\overline{CE1}$ transition low.
4. $\overline{OE}$ = VIL.
5. Transition is measured ±500mV from steady state. This parameter is sampled and not 100% tested.
6. CE2 is high.
7. $\overline{CE1}$ is low.
8. Address valid prior to or coincident with CE2 transition high.

Timing Waveforms (continued)

Write Cycle 1 [6]
(Write Enable Controlled)



Write Cycle 2
(Chip Enable Controlled)



Notes: 1. t_{AS} is measured from the address valid to the beginning of Write.
2. A Write occurs during the overlap (t_{WP}) of a low $\overline{CE1}$, a high CE2 and a low $\overline{WE}$.
3. t_{WR} is measured from the earliest of $\overline{CE1}$ or $\overline{WE}$ going high or CE2 going low to the end of the Write cycle.
4. If the $\overline{CE1}$ low transition or the CE2 high transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
5. t_{CW} is measured from the later of $\overline{CE1}$ going low or CE2 going high to the end of Write.
6. $\overline{OE}$ is continuously low. ($\overline{OE}$ = V_{IL})
7. Transition is measured ±500mV from steady state. This parameter is sampled and not 100% tested.

AC Test Conditions

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Time	5 ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Fig. 1, 2

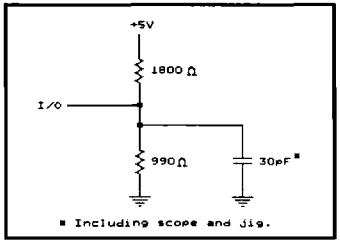


Figure 1. Output Load

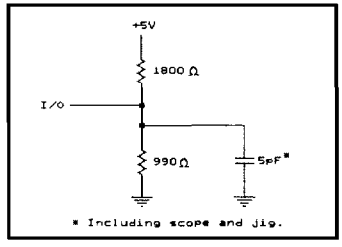


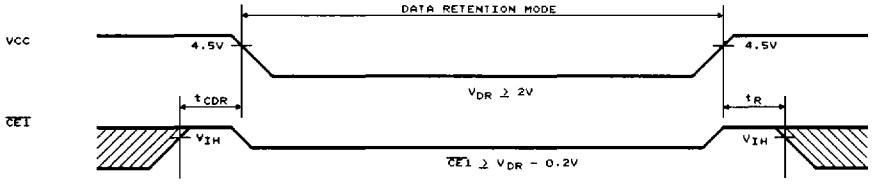
Figure 2. Output Load for t_{CLZ1}, t_{CLZ2}, t_{OLZ}, t_{CHZ1}, t_{CHZ2}, t_{OHZ}, t_{WHZ}, and t_{OW}

Data Retention Characteristics (TA = 0°C to 70°C)

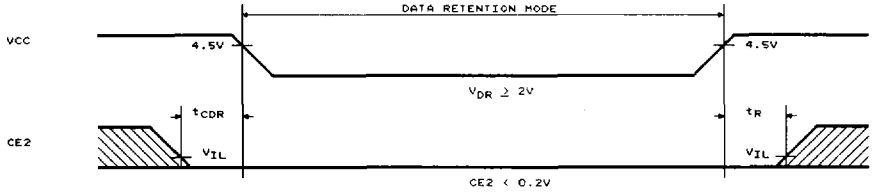
Symbol	Parameter		Min.	Max.	Unit	Conditions
V_{DR1}	VCC for Data Retention		2.0	5.5	V	$\overline{CE1}$ ≥ VCC - 0.2V
V_{DR2}			2.0	5.5	V	CE2 ≤ 0.2V $\overline{CE1}$ ≥ VCC - 0.2C or $\overline{CE1}$ ≤ 0.2V
I_{CCDR1}	Data Retention Current	L-Version	–	50*	μA	VCC = 3.0V $\overline{CE1}$ ≥ VCC - 0.2V CE2 ≥ VCC - 0.2V V_{IN} ≥ 0V
		LL-Version	–	10**		
I_{CCDR2}		L-Version	–	50*	μA	VCC = 3.0V CE2 ≤ 0.2V V_{IN} ≥ 0V
		LL-Version	–	10**		
t_{CDR}	Chip Disable to Data Retention Time		0	–	ns	See Retention Waveform
t_R	Operation Recovery Time		5	–	ms	

** UM621024B-70LL/10LL I_{CCDR}: Max. 3 μA at TA = 0°C to + 40°C
* UM621024B-70L/10L I_{CCDR}: Max. 20 μA at TA = 0°C to + 40°C

Low VCC Data Retention Waveform (1) ($\overline{CE1}$ Controlled)



Low VCC Data Retention Waveform (2) (CE2 Controlled)



Ordering Information

Part No.	Access Time (ns)	Operating Current Max. (mA)	Standby Current Max. (μA)	Package
UM621024B-70L	70	70	100	32L DIP
UM621024B-70LL		70	25	32L DIP
UM621024BM-70L		70	100	32L SOP
UM621024BM-70LL		70	25	32L SOP
UM621024BV-70L		70	100	32L TSOP
UM621024BV-70LL		70	25	32L TSOP
UM621024BVR-70L		70	100	32L TSOP
UM621024BVR-70LL		70	25	32L TSOP
UM621024B-10L	100	70	100	32L DIP
UM621024B-10LL		70	25	32L DIP
UM621024BM-10L		70	100	32L SOP
UM621024BM-10LL		70	25	32L SOP
UM621024BV-10L		70	100	32L TSOP
UM621024BV-10LL		70	25	32L TSOP
UM621024BVR-10L		70	100	32L TSOP
UM621024BVR-10LL		70	25	32L TSOP