M5M28F101P,FP,J,VP,RV-10,-12,-15

1048576-BIT(131072-WORD BY 8-BIT)CMOS FLASH MEMORY

DESCRIPTION

The Mitsubishi M5M28F101P, FP, J, VP, RV are high-speed 1048576-bit CMOS Flash Memories. They are suitable for the applications with micro-processor or micro-controller where on-board reprogramming is required. The M5M 28F101P, FP, J, VP, RV are fabricated by N-channel double polysilicon gate for memory and CMOS technology for peripheral circuits, and are available in 32pin plastic molded packages.

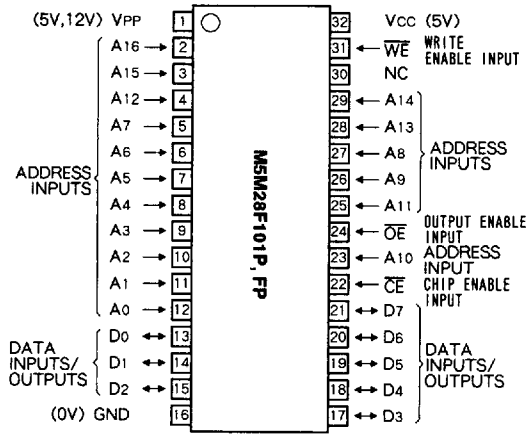
FEATURES

- 131072-word by 8-bit organization
- Access Time
  - M5M28F101P, FP, J, VP, RV-10 ..... 100ns (max.)
  - M5M28F101P, FP, J, VP, RV-12 ..... 120ns (max.)
  - M5M28F101P, FP, J, VP, RV-15 ..... 150ns (max.)
- Low power consumption — Active ..... 165mW (max.); Stand-by ..... 5.5mW (max.)
- Power supply voltage — V_{CC} = 5V ± 0.5V; V_{PP} = 12V ± 0.6V
- Byte program and Chip erase
- Program/erase operation controlled by software command
- Program/erase pulses controlled by an embedded timer
- 10000 program/erase cycles
- Tri-state output buffer
- TTL-compatible input and output in read and write mode
- Contained device-identifier code
- Incorporated data-protection
- Package: 32pin DIP (P)
  - 32pin SOP (FP)
  - 32pin PLCC (J)
  - 32pin TSOP (VP/RV)

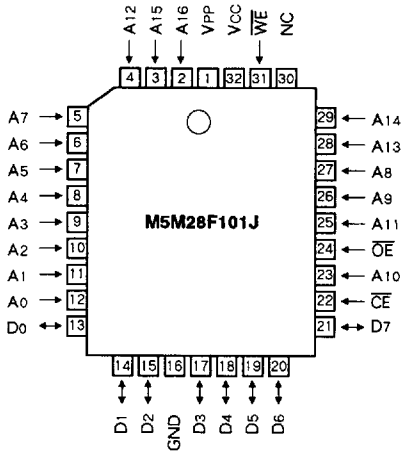
APPLICATION

Micro-computer systems and peripheral equipments

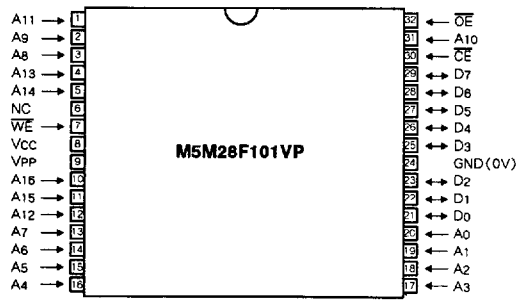
PIN CONFIGURATION (TOP VIEW)



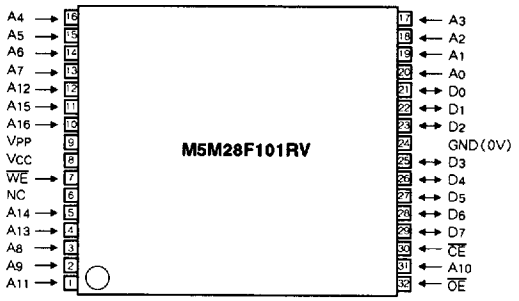
Outline 32P4 (DIP : P)
32P2M-A (SOP : FP)



Outline 32P0 (PLCC : J)



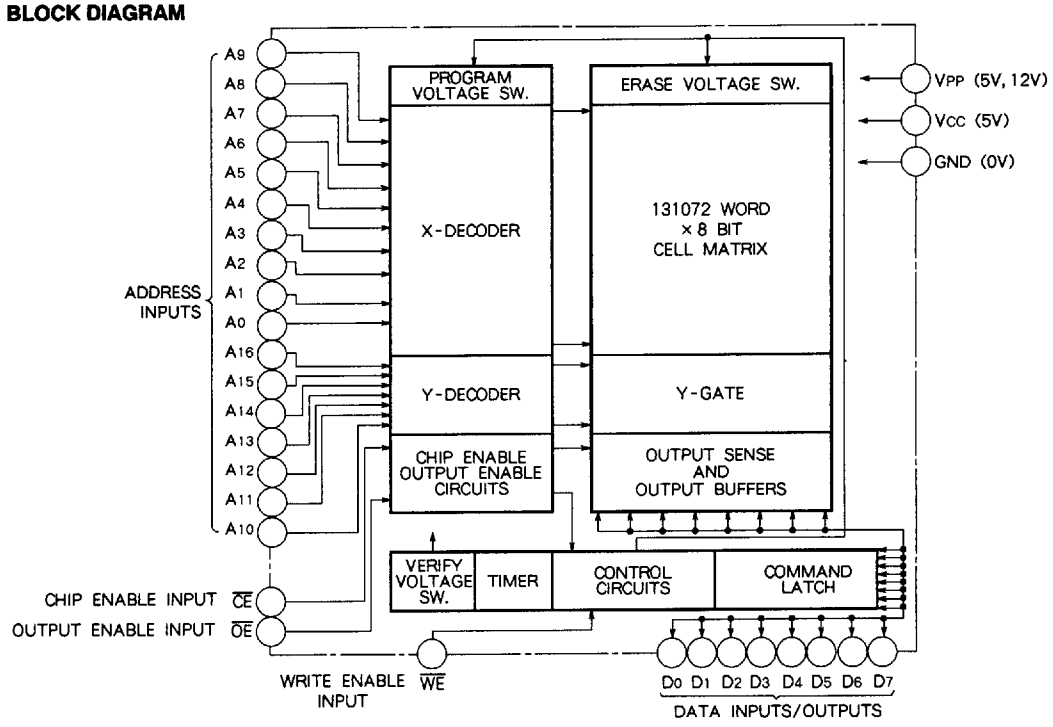
Outline 32P3H-E (TSOP : VP)



Outline 32P3H-F (TSOP : RV)

NC : NO CONNECTION

BLOCK DIAGRAM



FUNCTION

M5M28F101P, FP, J, VP, RV are set to the Read-only mode or Read-write mode by applying the voltage of V_{PPL} or V_{PPH}, respectively, to V_{PP} pin. In Read-only mode, three operation modes, Read, Out-put disable and Stand-by are accessible. While, in Read-Write mode, four operation modes, Read, Output disable, Stand-by and Write are functional.

Read

Set $\overline{CE}$ and $\overline{OE}$ terminals to the read mode (low level). Low level input to $\overline{CE}$ and $\overline{OE}$, and address signals to the address inputs (A_0~A_{16}) make the data contents of the designated address location available at data input/output (D_0~D_7).

Output Disable

When $\overline{OE}$ is at high level, output from the devices is disabled. Data input/output are in a high-impedance (High-Z) state.

Stand-by

When $\overline{CE}$ is at high level, the devices is in the stand-by mode and its power consumption is substantially reduced. Data input/output are in a high-impedance (High-Z) state.

Write

Software command accomplishes program and erase operations via the command latch in the device, when high voltage is supplied to V_{PP}. The contents of the latch serve as input to the internal controller. The controller output dictates the function of device. The command latch is written by bringing $\overline{WE}$ to low level, while $\overline{CE}$ is at low level and $\overline{OE}$ is at high level. Addresses are latched on the falling edge of $\overline{WE}$, while data is latched on the rising edge of $\overline{WE}$. Standard micro-processor write timings are used.

DATA PROTECTION

1. Power Supply Voltage
   When the power supply voltage (V_{CC}) is less than 2.5V, the device ignores $\overline{WE}$ signal.
2. Write Inhibit
   In the cases, as below, write mode is not set.
   1) When $\overline{CE}$ and $\overline{OE}$ are terminated to the low level.
   2) From 100ns through 5 µs after 2nd rising edge of $\overline{WE}$ for program.
   3) From 100ns through 5ms after 2nd rising edge of $\overline{WE}$ for erase.
3. Over-erase Protection
   Just after powering up, if erase command is inputted, erase operation is not executed. Once byte-program is performed or verified data is not FFH in the erase-verify mode, successive command input for erase will be accepted. Because of this, it is applicable to the case of multi-chip erasing simultaneously.

SOFTWARE COMMAND

When V_{PP} is low ($V_{PP} = V_{PPL}$), the contents of the command latch are fixed to 00H, and the device is in read-only mode. When V_{PP} is high ($V_{PP} = V_{PPH}$), the device enters read/write mode. The device operations are selected by writing specific software command into the command latch.

Read Command

The device is in read mode after writing Read Command (00H) to the command latch. The device continues to be in read mode until the other commands are written. When V_{PP} powers-up to high voltage ($V_{PP} = V_{PPH}$), the default contents of the command latch is 00H. So it is ensured that the false alteration of memory data does not occur during V_{PP} power transition.

Program Command

Program Command is the command for byte-program, and program is initiated by twice of write cycles. Program Command (40H) is written to the command latch in first write cycle, and the address and data to be programmed are latched in second write cycle. Then the address and data are latched on the falling edge and the rising edge of $\overline{WE}$ pulse, respectively. The byte-program operation is initiated at the rising edge of $\overline{WE}$ in second write cycle, and terminates in 10 µs, controlled by the internal timer.

Program Verify Command

Following byte program, the programmed byte must be verified. The program-verify is initiated by writing Program Verify Command (C0H) to the command latch. After writing Program Verify Command, programmed data is verified in read mode. Then the address information is not needed.

Erase Command

Erase Command is the command for chip-erase, and chip-erase is initiated by writing twice of the Erase Command (20H) consecutively to the command latch. The erase operation is initiated with the rising edge of the $\overline{WE}$ pulse and terminates in 9.5ms, controlled by the internal timer. This two-step sequence for chip-erase prevents from erasing accidentally.

Erase Verify Command

Following each erase, all bytes must be verified. The erase verify is initiated by writing Erase Verify Command (A0H) to the command latch, while the address to be verified is latched on the falling edge of the $\overline{WE}$ pulse. The erase verify command must be written to the command latch and each address is latched before each byte is verified. The operation continues for each byte until a byte is not erased, or the last address is accessed.

Reset Command

Reset Command is the command to safely abort the erase or program sequences. Following erase or program command in first write cycle, the operation is aborted safely by writing the two consecutive Reset Commands (FFH). Then the device enters read mode without altering memory contents.

Read Device Identifier Code

The device identifier mode allows the reading of a binary code from the device that identifies the manufacturer and device type. The PROM programmers read the manufacturer code and device code by raising A_9 to high voltage, and automatically select the corresponding programming algorithm.

Though PROM programmers can normally read device identifier codes by raising A_9 to high voltage, multiplexing high voltage onto address lines is not desired for micro-processor system. It is another means to read device identifier codes that Read Device Identifier Code Command (90H) is written to the command latch. Following the command write, the manufacturer code (1CH) and the device code (D0H) can be read from address 00000H and 00001H, respectively.

MODE SELECTION

Mode	Pins	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	V_{PP}	Data I/O
Read-Only	Read	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	Data out
	Output disable	V_{IL}	V_{IH}	V_{IH}	V_{PPL}	Hi-Z
	Stand by	V_{IH}	X	X	V_{PPL}	Hi-Z
Read/Write	Read	V_{IL}	V_{IL}	V_{IH}	V_{PPH}	Data out
	Output disable	V_{IL}	V_{IH}	V_{IH}	V_{PPH}	Hi-Z
	Stand by	V_{IH}	X	X	V_{PPH}	Hi-Z
	Write	V_{IL}	V_{IH}	V_{IL}	V_{PPH}	Data in

Note 1 : X can be V_{IL} or V_{IH}

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{I1}	All input or output voltage except V_{PP}/A_9	With respect to Ground	−0.6~7	V
V_{I2}	V_{PP} supply voltage		−0.6~14.0	V
V_{I3}	A_9 supply voltage		−0.6~13.5	V
T_{opr}	Operating temperature		−10~80	℃
T_{stg}	Storage temperature		−65~125	℃

SOFTWARE COMMAND DEFINITION

Command	First bus cycle			Second bus cycle		
	Mode	Address	Data I/O	Mode	Address	Data I/O
Read	Write	X	00H	———	———	———
Program (Byte Program)	Write	X	40H	Write	Program Address	Program Data
Program verify	Write	X	C0H	Read	X	Verify Data
Erase (Chip Erase)	Write	X	20H	Write	X	20H
Erase verify	Write	Verify address	A0H	Read	X	Verify Data
Reset	Write	X	FFH	Write	X	FFH
Read device identifier code	Write	X	90H	Read	ADI	DDI

Note 2 : Write and read mode are defined in mode selection table.
ADI = Address of Device Identifier : 00000H for manufacturer code, 00001H for device code.
DDI = Data of Device Identifier : 1CH for manufacturer code, D0H for device code.

DEVICE IDENTIFIER CODE

Code \ Pins	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Hex. Data
Manufacturer Code	V_{IL}	0	0	0	1	1	1	0	0	1CH
Device Code	V_{IH}	1	1	0	1	0	0	0	0	D0H

Note 3 : A_9 = 11.5V~13.0V
A_1~A_8, A_{10}~A_{16}, $\overline{CE}$, $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
V_{CC} = V_{PP} = 5V ± 10%

CAPACITANCE

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
C_{IN}	Input capacitance (Address, $\overline{CE}$, $\overline{OE}$, $\overline{WE}$)	Ta = 25℃, f = 1MHz, V_{in} = V_{out} = 0V			8	pF
C_{OUT}	Output capacitance				12	pF

DC ELECTRICAL CHARACTERISTICS (T_a = 0~70℃, V_{CC} = 5V ± 0.5V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{LI}	Input leakage current	$0 \leqq V_{IN} \leqq V_{CC}$			10	μA
I_{LO}	Output leakage current	$0 \leqq V_{OUT} \leqq V_{CC}$			10	μA
I_{SB1}	V_{CC} stand by current	V_{CC} = 5.5V, $\overline{CE}$ = V_{IH}			1	mA
I_{SB2}		V_{CC} = 5.5V, $\overline{CE}$ = V_{CC} ± 0.2V			100	μA
I_{CC1}	V_{CC} active read current	V_{CC}=5.5V, $\overline{CE}$=V_{IL}, f=10MHz, I_{OUT}=0mA			30	mA
I_{CC2}	V_{CC} program current	V_{PP} = V_{PPH}			30	mA
I_{CC3}	V_{CC} erase current	V_{PP} = V_{PPH}			30	mA
I_{PP1}	V_{PP} read current	$0 \leqq V_{PP} \leqq V_{CC}$			10	μA
		$V_{CC} < V_{PP} \leqq V_{CC}$ + 1.0V			100	
		V_{PP} = V_{PPH}			100	
I_{PP2}	V_{PP} program current	V_{PP} = V_{PPH}			30	mA
I_{PP3}	V_{PP} erase current	V_{PP} = V_{PPH}			30	mA
V_{IL}	Input low voltage		−0.5		0.8	V
V_{IH}	Input high voltage		2.0		V_{CC}+0.5	V
V_{OL}	Output low voltage	I_{OL} = 2.1mA			0.45	V
V_{OH1}	Output high voltage	I_{OH} = −400 μA	2.4			V
V_{OH2}		I_{OH} = −100 μA	V_{CC}−0.4			V
V_{PPL}	V_{PP} during read-only mode		0		V_{CC}+1.0	V
V_{PPH}	V_{PP} during read/write mode		11.4	12.0	12.6	V

AC ELECTRICAL CHARACTERISTICS (T_a = 0~70℃, V_{CC} = 5V ± 0.5V, unless otherwise noted)
Read-Only Mode

Symbol	Parameter	Limits						Unit
		M5M28F101-10		M5M28F101-12		M5M28F101-15		
		Min	Max	Min	Max	Min	Max	
t_{RC}	Read cycle time	100		120		150		ns
$t_{a\ (AD)}$	Address access time		100		120		150	ns
$t_{a\ (CE)}$	Chip enable access time		100		120		150	ns
$t_{a\ (OE)}$	Output enable access time		50		50		55	ns
t_{CLZ}	Chip enable to output in low Z	0		0		0		ns
t_{OLZ}	Output enable to output in low Z	0		0		0		ns
t_{DF}	Output enable high to output in high Z		25		30		35	ns
t_{OH}	Output hold from $\overline{CE}$, $\overline{OE}$, addresses	0		0		0		ns
t_{WRR}	Write recovery time before read	6		6		6		μs

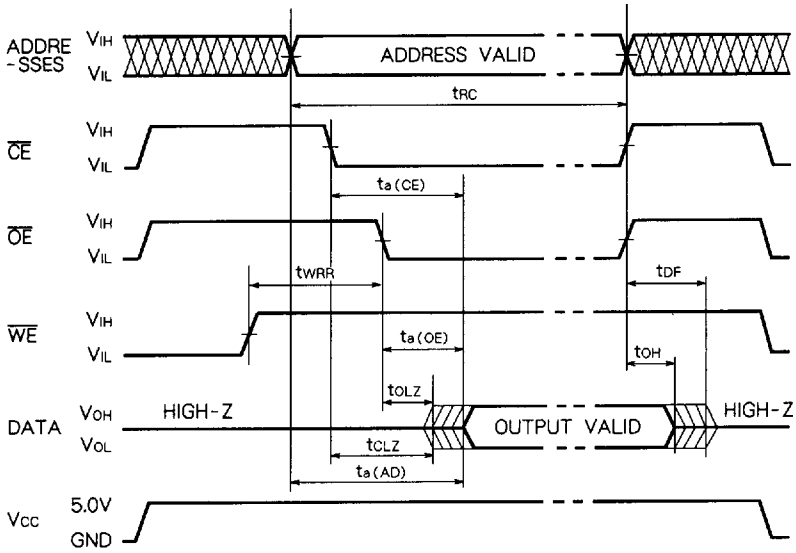
Note 4 : V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

Read/Write Mode

Symbol	Parameter	Limits						Unit
		M5M28F101-10		M5M28F101-12		M5M28F101-15		
		Min	Max	Min	Max	Min	Max	
t_{WC}	Write cycle time	100		120		150		ns
t_{AS}	Address set-up time	0		0		0		ns
t_{AH}	Address hold time	60		60		60		ns
t_{DS}	Data set-up time	50		50		50		ns
t_{DH}	Data hold time	10		10		10		ns
t_{WRR}	Write recovery time before read	6		6		6		μs
t_{RRW}	Read recovery time before write	0		0		0		μs
t_{CS}	Chip enable set-up time before write	20		20		20		ns
t_{CH}	Chip enable hold time	0		0		0		ns
t_{WP}	Write pulse width	60		60		60		ns
t_{OWP}	Optional write pulse width	70		70		70		ns
t_{WPH}	Write pulse width high	20		20		20		ns
t_{DP}	Duration of programming operation	10		10		10		μs
t_{DE}	Duration of erase operation	9.5		9.5		9.5		ms
t_{VSC}	V_{PP} set-up time to chip enable low	1		1		1		μs

Note 5 : Read timing parameters during read/write mode are the same as during read-only mode.
V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

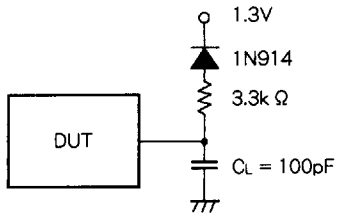
AC WAVEFORMS FOR READ OPERATIONS



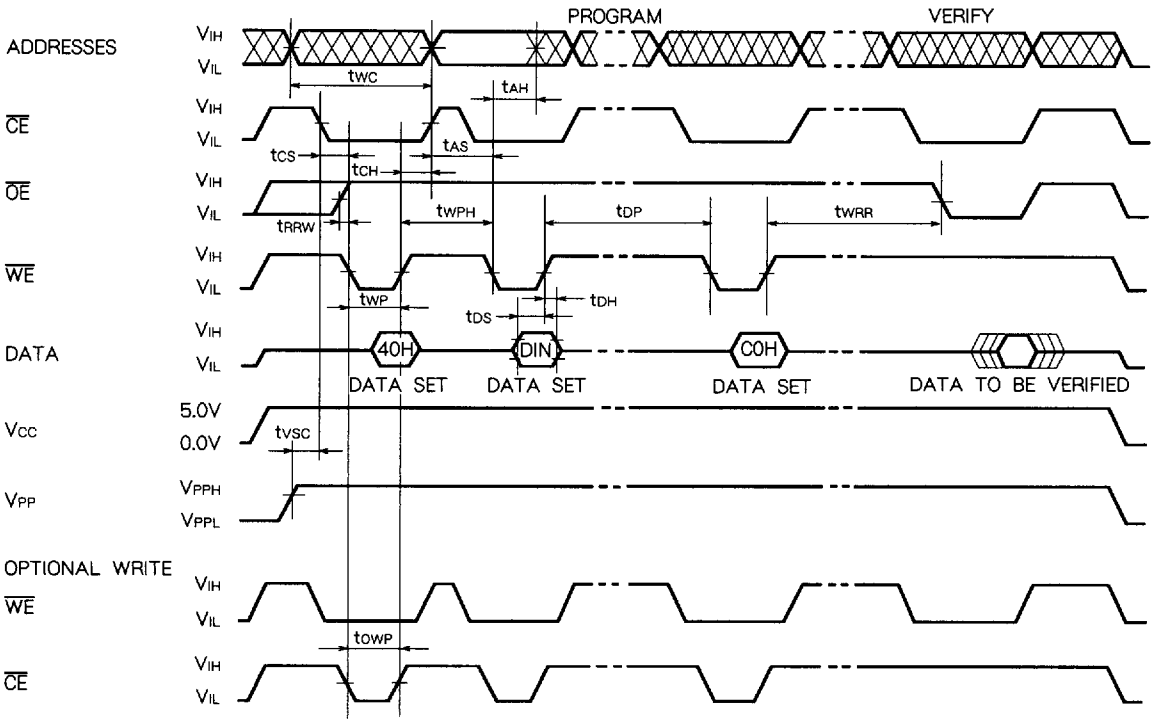
TEST CONDITIONS
FOR AC CHARACTERISTICS

Input voltage : V_{IL} = 0.45V, V_{IH} = 2.4V
Input rise and fall times : ≦ 10ns
Reference voltage
at timing measurement : 1.5V
Output load : 1TTL gate + C_L
(= 100pF)

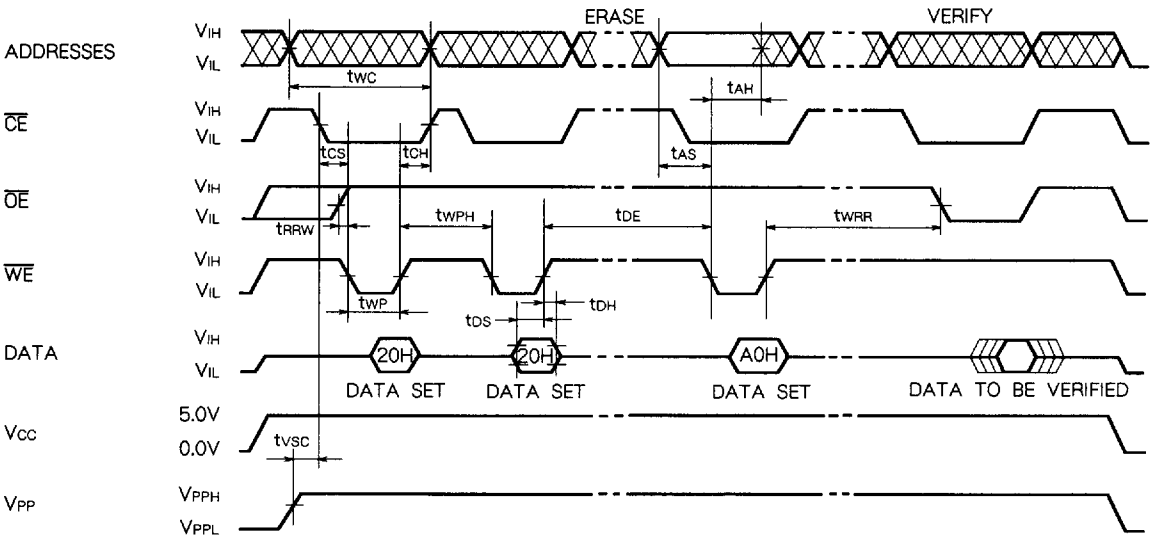
or



AC WAVEFORMS FOR PROGRAM OPERATIONS

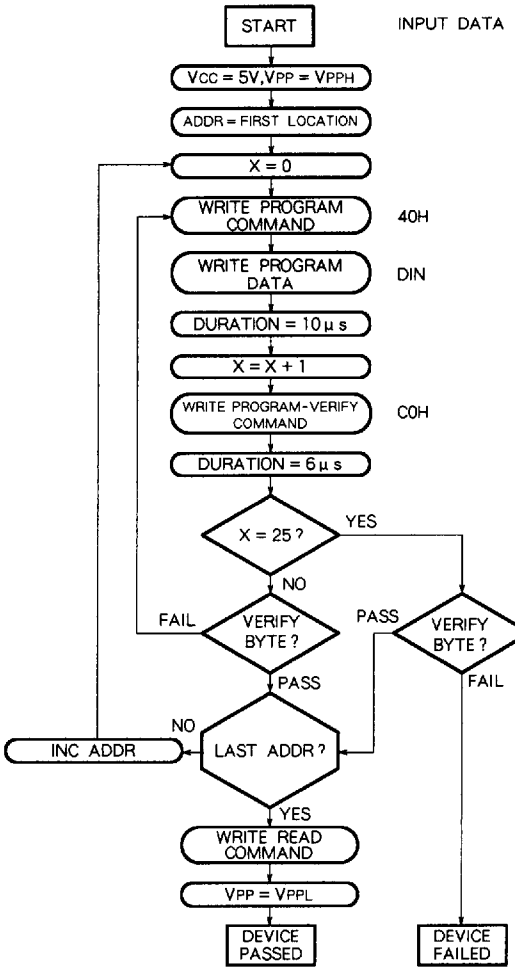


AC WAVEFORMS FOR ERASE OPERATIONS



PROGRAMMING AND ERASE ALGORITHM FLOW CHART

PROGRAM :



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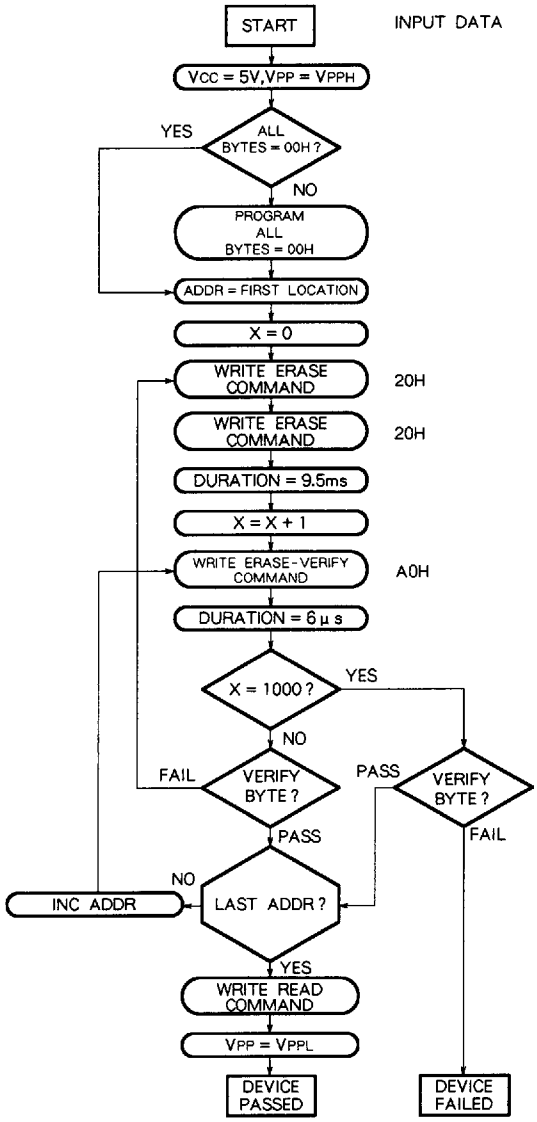

(Erase Complete)